AN1156
APPLICATION NOTE
Connecting the MC68331 Microcontroller to M29 Series Flash Memories

CONTENTS

INTRODUCTION

This application note describes a method of to connecting an M29F800A Flash memory to an MC68331 microcontroller. The application note can be used as a reference for other Flash memory devices from STMicroelectronics.

The M29F800A is an 8 Mbit Flash memory from STMicroelectronics, which can be configured as a 1M byte-wide memory, or 512K word-wide memory. Other Flash parts that can be used in place of the M29F800A, with only minor circuit changes, include the M29F400B, M29F200B and M29F100B. The TSOP48 package of these memories is pin-compatible with the M29F800A, the only difference in the SO44 package is the Ready/Busy Output pin.

The MC68331 is a member of Motorola's 68300 family of integrated microprocessors. It is a general purpose 32-bit microcontroller with a wide variety of application areas including telecommunications and automotive.

ADVANTAGES OF FLASH

Flash memories can be used to store both code and data for the MC68331 microcontroller. Unlike EPROMs the data in Flash memories can be changed by the microcontroller. This enables non-volatile user data to be stored in the Flash. Field upgrades of the application code can be performed without any disassembly, unlike EPROM solutions.

It is usual to write separate boot and application programs so that the application program can be upgraded without changing the boot program. If the upgrade fails then the processor will still boot and it will be possible to reattempt to upgrade the application. The boot code should be programmed into the Flash before the Flash is fitted to the circuit board, otherwise it may not be possible to boot the microprocessor. Often the block containing the boot program is protected so it cannot become corrupt.

FLASH BUS ARCHITECTURE

Take a look at the bus on the M29F800A, Figure 1 shows the Logic Diagram. The memory has separate Address and Data Buses that can connect directly to the Address and Data Buses on the MC68331. The control lines are Chip Enable ($\overline{E}$), Output Enable ($\overline{G}$) and Write Enable ($\overline{W}$). Also, Ready/Busy Output (R/$\overline{B}$) and Reset/Block Temporary Unprotect ($\overline{RP}$) are present. Finally there is the $\overline{BYTE}$ pin that selects 8-bit or 16-bit mode.

Figure 1. M29F800B Logic Diagram
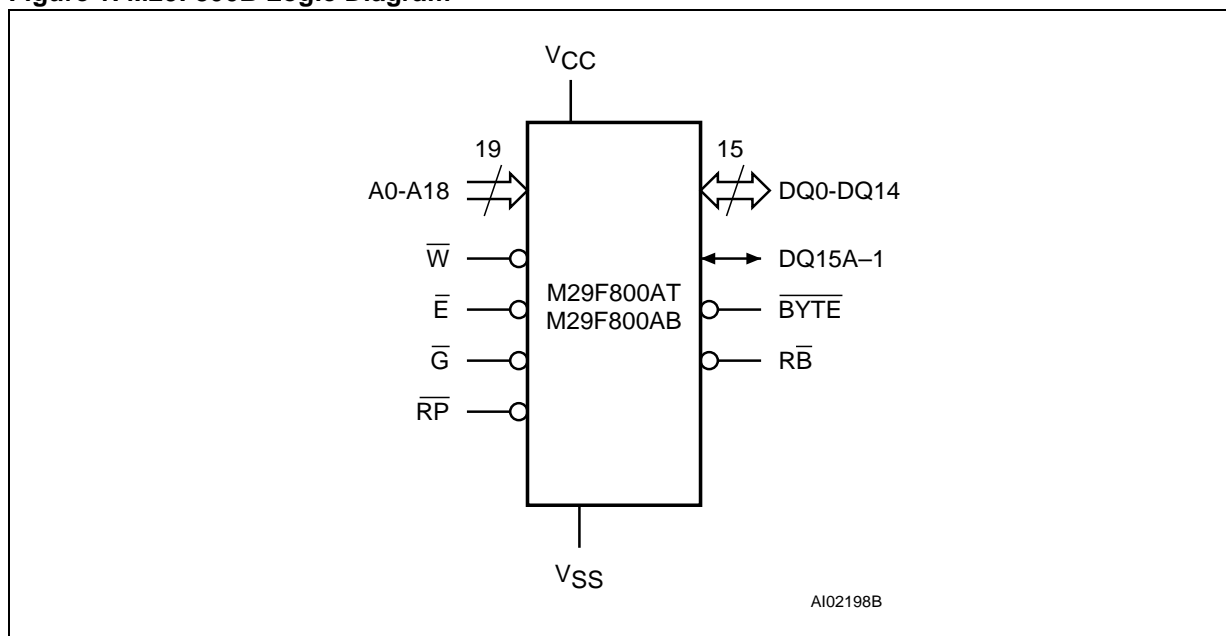

The M29F800A has been designed to allow $\overline{BYTE}$ to change between accesses, so 8-bit accesses and 16-bit accesses can be achieved in the same design. In practice it is far simpler to always use the memory in one mode; in order to swap modes additional logic is required to decode the DQ15A-1 pin, this would complicate the design, add cost and probably increase the wait-states required to access the memory.

In the example here 16-bit mode has been chosen. Care should be taken to make sure that all write accesses will write 16-bits at a time. In order to change one byte in the memory it will be necessary to write a word. Programming words and bytes takes the M29F800A the same amount of time; the internal charge pumps required for the program operation are word-wide, not byte-wide. Once the choice has been made to keep $\overline{BYTE}$ high, the special pin, DQ15A–1, can be treated like any other Data Input/Output pin. It forms part of the Data Bus, DQ0-DQ15. Note that the A0 address pin on the M29F800B specifies the address of a word, not of a byte; the address bus of the MC68331 will need to be shifted compared to the address bus of the M29F800A in order to address the Flash correctly.

The Reset/Block Temporary Unprotect pin ($\overline{RP}$) accepts three states: Reset (V_{IL}), Not Reset (V_{IH}) and Block Temporary Unprotect (V_{ID}). Reset and Not Reset are the usual signals for a Reset line. The MC68331 provides these signals on its $\overline{RESET}$ pin. The third state, Block Temporary Unprotect is used to temporarily unprotect blocks that have been specifically protected in the memory. Many applications do not protect any blocks and therefore connect the $\overline{RP}$ pin directly to the system Reset signal.

Figure 2 gives an example of how the connection between the MC68331's $\overline{RESET}$ pin and the M29F800A's $\overline{RP}$ pin can be made. The circuit makes use of a jumper to enable Block Temporary Unprotect. Many applications will provide the 12V from an external source, in which case the jumper can be replaced by a connector. The advantage with the circuit, as it stands, is that a reset from the MC68331 will override Block Temporary Unprotect and cause the Flash to reset. Only four additional components are required.

Figure 2. Reset/Block Temporary Unprotect Circuit

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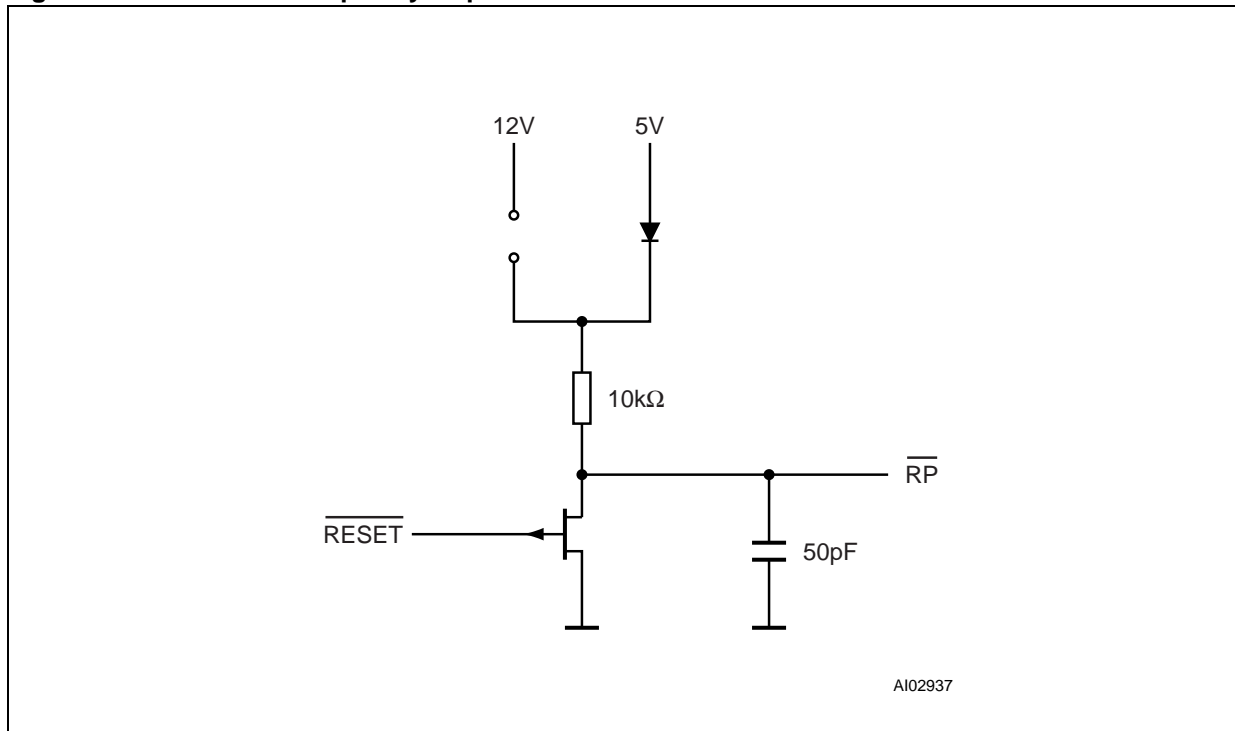
Before the jumper is inserted, and when $\overline{RESET}$ is High, V_{IH}, $\overline{RP}$ is connected to 5V through the 10kΩ resistor and the diode. The current required by $\overline{RP}$ is very low, in the order of 1μA at 5V. The voltage drop in the resistor and the diode at these currents will keep $\overline{RP}$ very close to 5V. When the jumper is fitted the diode ceases to conduct and $\overline{RP}$ rises to 12V as the capacitor charges. The time-constant of a 10kΩ resistor and a 50pF capacitor is 500ns, satisfying the t_{PHPHH} rise-time requirements of the M29F800A. During a Reset, $\overline{RESET}$ is Low, V_{IL}, and the JFET is switched on, bringing $\overline{RP}$ close to ground. The current consumption during a Reset rises due to the current through the 10kΩ resistor.

Although the use of a jumper may not be the most elegant solution, it is a practical one because it maintains the security level offered by the Block Protection. There is little point in having the Block Temporary Unprotect pin under software control. The whole point of the Block Protection feature is to protect against software failure. Allowing the Block Temporary Unprotect feature to be under the control of software is nearly equivalent to not protecting the blocks in the first place.

MC68331 BUS ARCHITECTURE

The MC68331's bus architecture can be daunting on first appearance. There are many control lines to allow for 8-bit accesses, 16-bit accesses, bus arbitration, memory protection (user/supervisor memory spaces) and other complicated controls. Many applications do not need to make use of these features. Only a simple connection is considered here.

The MC68331 uses the $\overline{CSBOOT}$ pin to select the boot memory. This memory is mapped to 000000h at boot time, and 13 wait states are selected. There are eleven other chip selects available to control the Flash if the Flash is not used to boot the microcontroller. The MC68331 does not provide separate read and write control lines, instead there is only one R/$\overline{W}$ output pin. It is possible to configure the chip selects to act as Chip Enable, Write Enable and Output Enable for the Flash memory without using any external logic.

One interesting point that should be considered is the use of the M29F800A's chip select. The M29F800A can be connected to the MC68331 as the boot device without any glue logic if the M29F800A's Chip Enable is tied to ground. The $\overline{\text{CSBOOT}}$ pin can then be used to control Output Enable and $\overline{\text{CS1}}$ can be used to control Write Enable. On boot $\overline{\text{CSBOOT}}$ can be used to access the Flash, $\overline{\text{CS1}}$ can be configured in the boot code to allow write accesses to the Flash. However, tying Chip Enable low never allows the Flash to enter its Standby state and the Read Supply Current will be consumed unless Automatic Standby is entered. (Automatic Standby will still be entered if the Address Bus stops changing, e.g. if the Microprocessor executes a Low Power STOP operation).

The circuit shown here makes use of an inverter to provide the correct Output Enable signal.

**Figure 3. Connection between the MC68331 and the M29F800A**

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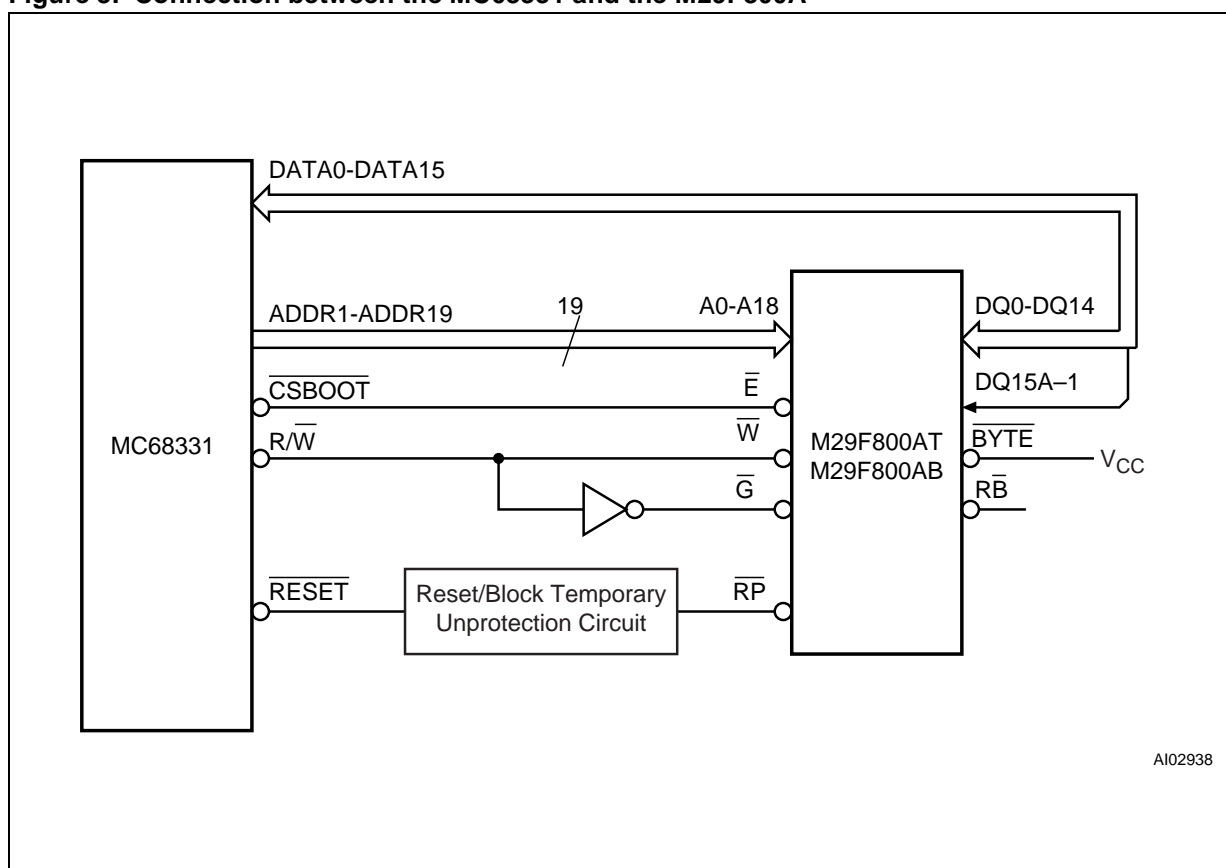
TIMING REQUIREMENTS

The MC68331 has a zero wait-state external access time of about 140ns when running with a 20.97MHz clock. Additional wait-states can be inserted for slower external peripherals. The timings in Table 1 and Figure 4 examine the Read cycles timing requirements, Table 2 and Figure 5 examine the Write Cycle timing requirements; both are from the Flash's perspective. A 10ns delay has been included in the MC68331 timings that affect $\overline{\text{G}}$ to account for the delay in the inverter.

Table 1. Read Timing Requirements

M29F800A				MC68331	
Symbol	55	70	90	F1 = 16.78 MHz $\overline{\text{DSACK}}$ = 0	F1 = 20.97 MHz $\overline{\text{DSACK}}$ = 0
t_{AVAV}	55	70	90	150	120
t_{AVQV}	55	70	90	116	91
t_{ELQV}	55	70	90	80	57
t_{GLQV}	30	30	35	106	81
t_{EHQZ}	18	20	20	55	48
t_{OH}	0	0	0	0	0

Figure 4. Principal Read Timing Waveforms
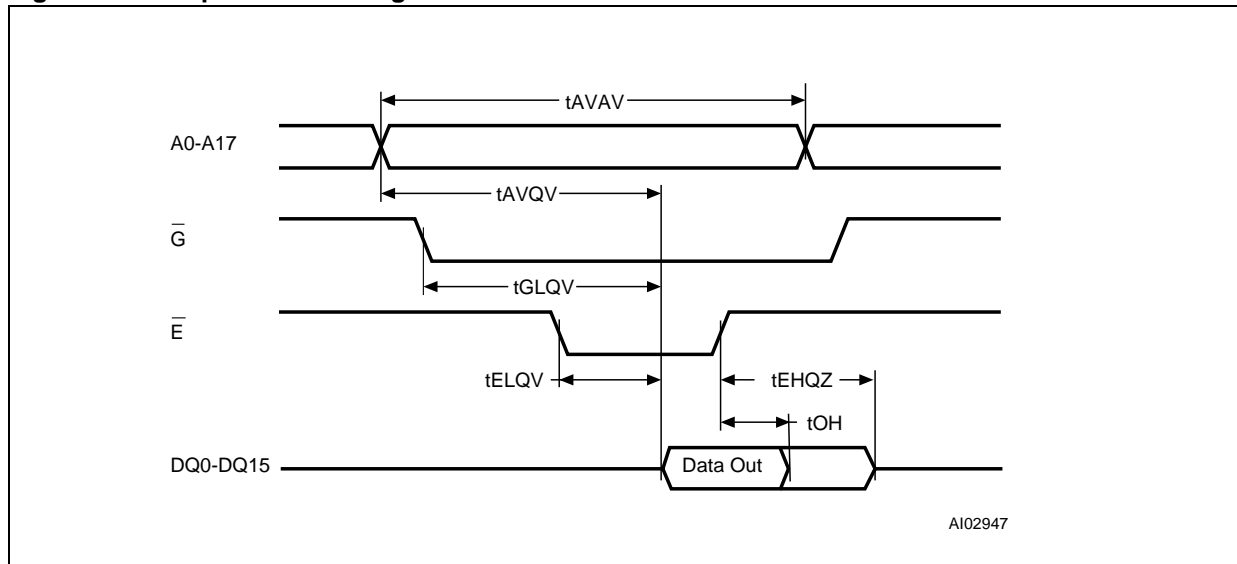
From the timings it can be seen that the 55ns part is required to meet all of the timings of the 20MHz MC68331. The 70ns part is sufficient for the 16MHz MC68331.

The MC68331 always leaves its Chip Select signal until last in any read or write cycle. The M29F800A on the other hand uses Chip Enable to enter the Standby mode. Flash access times using Chip Enable are always longer than the access times using Output Enable or Write Enable. The solution that ties the Flash's Chip Enable to ground and controls accesses using Output Enable and Write Enable will allow Flash memories with slower access times to meet zero wait state timing requirements. However, it will also cause the supply current to rise.

Table 2. Write Timing Requirements, Chip Enable Controlled

	M29F800A			MC68331	
Symbol	55	70	90	F1 = 16.78 MHz $\overline{\text{DSACK}}$ = 0	F1 = 20.97 MHz $\overline{\text{DSACK}}$ = 0
t_{AVAV}	55	70	90	150	120
t_{ELEH}	40	45	45	100	80
t_{DVEH}	25	30	45	43	33
t_{EHEL}	20	20	20	40	32
t_{ELAX}	40	45	45	117	92

Figure 5. Principal Write Timing Waveforms, Chip Enable Controlled
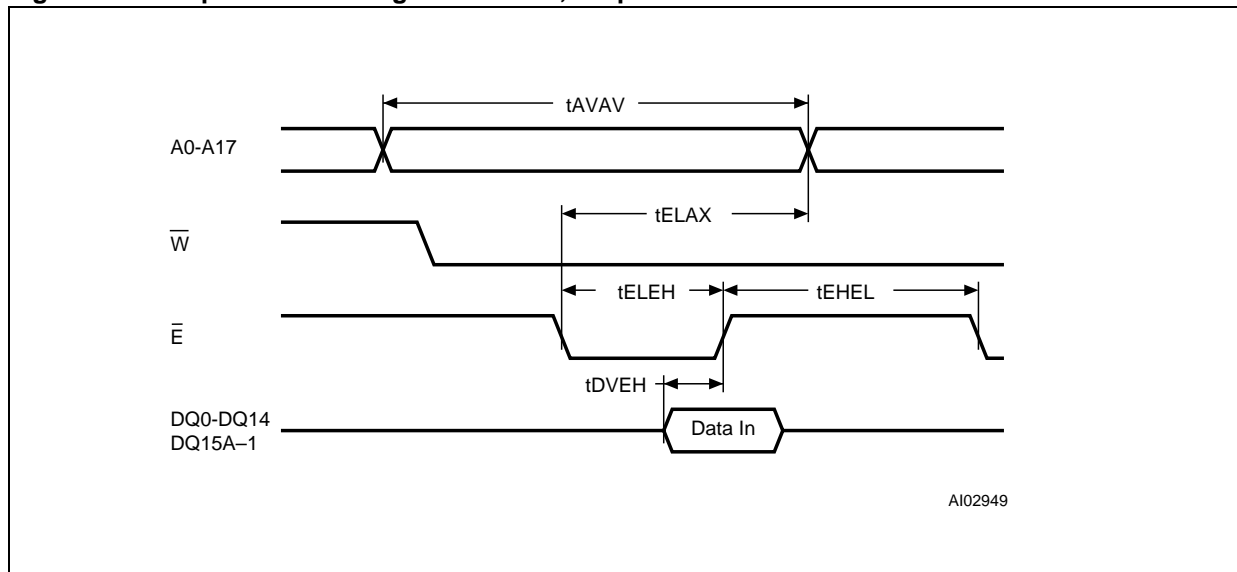
CONCLUSION

The M29F800A and other STMicroelectronics Flash can be connected to the MC68331 in glueless con-figurations, or with a simple inverter. The Flash can be used to boot the MC68331 and provides a solution that allows field upgrades to the application software without the need to disassemble the product.

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com   (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.