REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02; editorial changes throughout. Redrawn.	93-06-23	M. A. Frye
B	Update boilerplate. Add device types 03 and 04. Add case outline M. Editorial changes throughout.	94-06-30	M. A. Frye
C	Add 05 device. Removed some parameters from table IIB. Updated boilerplate. ksr	98-04-06	Raymond Monnin
D	Added equation to footnote 2/, made corrections to table IB. Changed sample size in paragraph 4.4.1. Removed (Dose Rate Induced latchup testing) and (Dose Rate Upset testing) paragraphs. Updated boilerplate. ksr	98-07-10	Raymond Monnin
E	Change 1.3 Maximum junction temperature from 175°C to 150°C. Added footnote 2/ to Figure 2 for the T and M case outlines. Add die information per Appendix A. ksr	98-09-21	Raymond Monnin

REV																			
SHEET																			
REV	E	E	E	E	E	E	E	E	E										
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
KENNETH RICE

APPROVED BY
TIM H. NOH

DRAWING APPROVAL DATE
92-06-23

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316

MICROCIRCUIT, MEMORY, DIGITAL, , CMOS,
FIELD PROGRAMMABLE GATE ARRAY,
2000 GATES,MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-90965**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E526-98

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	90965	01	V	X	X
Federal stock class designator	RHA designator (See 1.2.1)		Device type (See 1.2.2)	Device class designator (See 1.2.3)	Case outline (See 1.2.4)	Lead finish (See 1.2.5)
\ Drawing number /						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	1020A	2000 gate, field programmable gate array	186 ns
02	1020A-1	2000 gate, field programmable gate array	158 ns
03	1020B	2000 gate, field programmable gate array	168.2 ns
04	1020B-1	2000 gate, field programmable gate array	142.9 ns
05	RH1020	2000 gate, field programmable gate array	168.2 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC2 - J44	44	J-lead chip carrier
Y	CQCC2 - J68	68	J-lead chip carrier
Z	CQCC2 - J84	84	J-lead chip carrier
U	CMGA15 - P85	84	Pin grid array 1/
T	CQCC1 - F84	84	Unformed lead chip carrier
M	See figure 1	84	Unformed lead chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Actual number of pins is 85 including one index or orientation pin (C3).

1.3 Absolute maximum ratings. 2/

DC supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range (V_I)	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage range (V_O)	-0.5 V dc to V_{DD} + 0.5 V dc
I/O source sink current I_{IO})	±20 mA
Storage temperature range (T_{STG})	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	300° C
Thermal resistance, junction-to-case (Θ_{JC})	
Case outline X, Y, Z, U, T	See MIL-STD-1835
Case outline M	10° C/W 3/
Maximum junction temperature (T_J)	+150° C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55° C to +125° C

1.5 Radiation features.

Total Dose	300K rads (maximum) 4/

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Device electrical characteristics are verified for post irradiation levels at 25° C per MIL-STD-883, Test method 1019, condition A and post 168 hours, 100° C, biased anneal.
5/ 100 percent test coverage of blank programmable logic devices.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standard Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-95 - Standard Guide for the Measurement of Single Event Procedures from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 of MIL-STD-883 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

Table IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage	V_{OL}	test one output at a time, V_{DD} = 4.5 V, I_{OL} = 4.0 mA	1,2,3	All		0.4	V
Output high voltage	V_{OH}	test one output at a time, V_{DD} = 4.5 V, I_{OH} = -3.2 mA	1,2,3	All	3.7		V
Input low voltage	V_{IL}		1,2,3	All		0.8	V
Input high voltage	V_{IH}		1,2,3	01-04	2.0		V
				05	2.2	VDD+ 0.3	
Standby supply current	I_{DD}	outputs unloaded, V_{DD} = 5.5 V, $V_{IN} = V_{DD}$ or GND	1,2,3	All		25	mA
Input leakage current	I_{IL}	V_{DD} = 5.5 V, $V_{IN} = V_{DD}$ or GND	1,2,3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{DD} = 5.5 V, $V_{OUT} = V_{DD}$ or GND	1,2,3	All	-10	10	µA
Output short circuit current	I_{OS}	2/ V_{OUT} = VDD	1,2,3	01,02	20	140	mA
				05	0	160	
		V_{OUT} = GND	1,2,3	01,02	-100	-10	
				05	-100	0	
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f = 1.0 Mhz, V_{OUT} = 0 V	4	All		20	pF
Functional tests	FT 3/	V_{DD} = 4.5 V , See 4.4.1e and f	7,8A,8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, V_{IL} = 0 V, V_{IH} = 3.0 V, V_{DD} = 4.5 V, V_{OUT} = 1.5 V 4/	9,10,11	01		186	ns
				02		158	
				03		168.2	
				04		142.9	
				05		168.2	

1/ All tests shall be performed under the worst case condition unless otherwise specified. Devices supplied to this drawing will meet levels M, D, L, R, and F, of irradiation. However, this device is only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ V_{DD} = 4.5 V for minimum limits and V_{DD} = 5.5 V for maximum limits. Test one output at a time, duration of short circuit condition shall not exceed one second. This test for devices 01, 02, and 05 only.

3/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA and PRB pins. These tests form a part of the manufacturer's test tape and shall be maintained by the approved source(s) of supply and shall be made available upon request by the preparing or acquiring activity.

4/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit shall be programmed into all device prior to screening. The binning circuit consists of one input buffer plus 28 logic modules plus one output buffer. The logic modules are distributed along two sides of the device. These modules are configured as inverting and non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

TABLE IB. SEP test limits. 1/ 3/

Symbol	Characteristics	Upset Mode	Conditions	Bias V_{DD} =	Effective LET no upset (MeV-cm^2/mg)	Saturated X-section
SEL	Single event latchup	all	-55°C≤T_C≤125°C	5.5 V	>84	N/A
SEU	Single event upset	C-Latch	-55°C≤T_C≤125°C	4.5 V	>8 3/	1.5 x 10^{-6} cm^2/bit
		1 Mhz Clock 2/	T_A = +25°C	5.0 V	18.8	2.5 x 10^{-7} cm^2/device
SEDR 4/	Single event dielectric (antifuse) rupture	all	-55°C≤T_C≤125°C	5.5 V	>40	N/A

Notes:
1/. Verification test per TRB approved test plan.
2/. Clock upset causes upset in the clocked flip-flops, its rate is proportional to the clock frequency and can be computed using the following; $f \times \frac{3\times10^{-8} \text{ upset/device-day}}{1 \text{ MHz}}$;
Where f is the clock frequency of interest and 3 x 10^{-8} (upset/device-day) is the computed rate from the SEU testing data.

3/. Threshold LET at 1% saturated X-section is 13, and at 10%, saturated X-section is 25.
4/. Tested at worst case that ions have perpendicular incidence.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

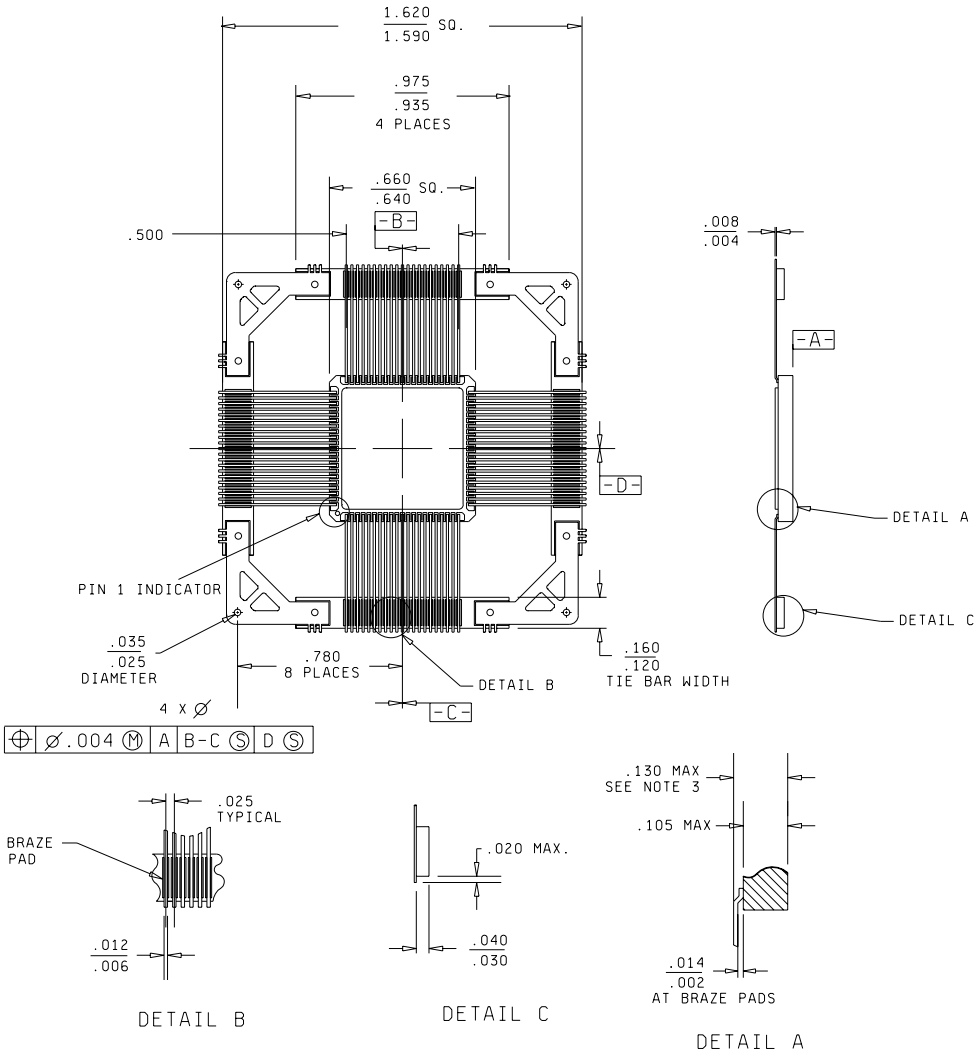
a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. A sample size of 5 devices with no failures, and all input and output terminals shall be required.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

Case M



Inches	mm	Inches	mm	Inches	mm	Inches	mm
.002	.050	.020	2.67	.120	3.05	.935	23.75
.004	.100	.025	3.05	.130	3.30	.975	24.77
.006	.150	.030	3.30	.160	4.06	1.590	40.39
.008	.200	.035	4.06	.500	12.70	1.620	41.15
.012	.300	.040	12.70	.640	16.26		
.014	.360	.105	16.26	.660	16.76		

NOTES:
1. Dimensions are in inches.
2. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
3. For detail A: Includes lead attach dogleg height and lid height, whichever is greater.

FIGURE 1. Case outline.

Device type	All 1/				
Case outlines	X	Y	Case outlines	X	Y
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	I/O	I/O	35	VDD	I/O
2	I/O	I/O	36	SDI or I/O	I/O
3	VDD	I/O	37	DCLK or I/O	I/O
4	I/O	VDD	38 1/	PRA or I/O	VDD
5	I/O	I/O	39 1/	PRB or I/O	I/O
6	I/O	I/O	40	I/O	I/O
7	I/O	I/O	41	I/O	I/O
8	I/O	I/O	42	I/O	I/O
9	I/O	I/O	43	GND	I/O
10	GND	I/O	44	I/O	I/O
11	I/O	I/O	45	- - -	I/O
12	I/O	I/O	46	- - -	I/O
13	I/O	I/O	47	- - -	I/O
14	VDD	GND	48	- - -	I/O
15	I/O	GND	49	- - -	GND
16	VPP	I/O	50	- - -	I/O
17	I/O	I/O	51	- - -	I/O
18	I/O	I/O	52	- - -	CLK or I/O
19	I/O	I/O	53	- - -	I/O
20	I/O	I/O	54	- - -	MODE
21	GND	VDD	55	- - -	VDD
22	I/O	I/O	56	- - -	SDI or I/O
23	I/O	I/O	57	- - -	DCLK or I/O
24	I/O	I/O	58 1/	- - -	PRA or I/O
25	VDD	VPP	59 1/	- - -	PRB or I/O
26	I/O	I/O	60	- - -	I/O
27	I/O	I/O	61	- - -	I/O
28	I/O	I/O	62	- - -	I/O
29	I/O	I/O	63	- - -	I/O
30	I/O	I/O	64	- - -	I/O
31	I/O	I/O	65	- - -	I/O
32	GND	GND	66	- - -	GND
33	CLK or I/O	I/O	67	- - -	I/O
34	MODE	I/O	68	- - -	I/O

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03, 04, and 05. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections.

Device type	All 1/	Device type	All 1/
Case outlines	Z	Case outlines	Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O	43	I/O
2	I/O	44	I/O
3	I/O	45	I/O
4	VDD	46	VDD
5	I/O	47	I/O
6	I/O	48	I/O
7	I/O	49	I/O
8	I/O	50	I/O
9	I/O	51	I/O
10	I/O	52	I/O
11	I/O	53	I/O
12	NC	54	I/O
13	I/O	55	I/O
14	I/O	56	I/O
15	I/O	57	I/O
16	I/O	58	I/O
17	I/O	59	I/O
18	GND	60	GND
19	GND	61	GND
20	I/O	62	I/O
21	I/O	63	I/O
22	I/O	64	CLK or I/O
23	I/O	65	I/O
24	I/O	66	MODE
25	VDD	67	VDD
26	VDD	68	VDD
27	I/O	69	I/O
28	I/O	70	I/O
29	I/O	71	I/O
30	I/O	72	SDI or I/O
31	I/O	73	DCLK or I/O
32	I/O	74 1/	PRA or I/O
33	VPP	75 1/	PRB or I/O
34	I/O	76	I/O
35	I/O	77	I/O
36	I/O	78	I/O
37	I/O	79	I/O
38	I/O	80	I/O
39	I/O	81	I/O
40	GND	82	GND
41	I/O	83	I/O
42	I/O	84	I/O

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03, 04, and 05. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections - Continued.

Device type	All 1/	Device type	All 1/
Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	I/O	F9	CLK or I/O
A2	I/O	F10	GND
A3	I/O	F11	I/O
A4	I/O	G1	I/O
A5	I/O	G2	VDD
A6	I/O	G3	I/O
A7	I/O	G9	I/O
A8	I/O	G10	GND
A9	I/O	G11	I/O
A10	I/O	H1	I/O
A11 1/	PRA or I/O	H2	I/O
B1	I/O	H10	I/O
B2	NC	H11	I/O
B3	I/O	J1	I/O
B4	I/O	J2	I/O
B5	VDD	J5	I/O
B6	I/O	J6	I/O
B7	GND	J7	I/O
B8	I/O	J10	I/O
B9	I/O	J11	I/O
B10 1/	PRB or I/O	K1	I/O
B11	SDI or I/O	K2	VPP
C1	I/O	K3	I/O
C2	I/O	K4	I/O
C3	Keying pin	K5	GND
C5	I/O	K6	I/O
C6	I/O	K7	VDD
C7	I/O	K8	I/O
C10	DCLK or I/O	K9	I/O
C11	I/O	K10	I/O
D1	I/O	K11	I/O
D2	I/O	L1	I/O
D10	I/O	L2	I/O
D11	I/O	L3	I/O
E1	I/O	L4	I/O
E2	GND	L5	I/O
E3	GND	L6	I/O
E9	VDD	L7	I/O
E10	VDD	L8	I/O
E11	MODE	L9	I/O
F1	VDD	L10	I/O
F2	I/O	L11	I/O
F3	I/O		

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03, 04, and 05. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

FIGURE 2. Terminal connections - Continued.

Device type	All 1/	Device type	All 1/
Case outline	T, M	Case outline	T, M
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	43	I/O
2	I/O	44	I/O
3	I/O	45	I/O
4	I/O	46	I/O
5	I/O	47	I/O
6	I/O	48	I/O
7	GND	49	GND
8	GND	50	GND
9	I/O	51	I/O
10	I/O	52	I/O
11	I/O	53	CLK/I/O
12	I/O	54	I/O
13	I/O	55	MODE
14	VDD	56	VDD
15	VDD	57	VDD
16	I/O	58	I/O
17	I/O	59	I/O
18	I/O	60	I/O
19	I/O	61 2/	SDI/I/O
20	I/O	62 2/	DCLK/I/O
21	I/O	63 1/	PRA/I/O
22	VPP	64 1/	PRB/I/O
23	I/O	65	I/O
24	I/O	66	I/O
25	I/O	67	I/O
26	I/O	68	I/O
27	I/O	69	I/O
28	I/O	70	I/O
29	GND	71	GND
30	I/O	72	I/O
31	I/O	73	I/O
32	I/O	74	I/O
33	I/O	75	I/O
34	I/O	76	I/O
35	VDD	77	VDD
36	I/O	78	I/O
37	I/O	79	I/O
38	I/O	80	I/O
39	I/O	81	I/O
40	I/O	82	I/O
41	I/O	83	I/O
42	I/O	84	I/O

NC = No connection

1/ PRA and PRB are inverting signals for device types 01 and 02, and non-inverting signals for device types 03, 04, and 05. PRA and PRB are used only for device testing or debugging. In normal operation, all device types exhibit identical logic on these pins.

2/ For device type 05 only. The special function pins 61(SDI_I/O) and 62 (DCLK_I/O) have shown anomalous operation when configured as outputs. Designers should ensure that these pins are unused as I/Os or, if necessary, they can be used as inputs only. Please contact vendor for complete details on product advisory.

FIGURE 2. Terminal connections - Continued.

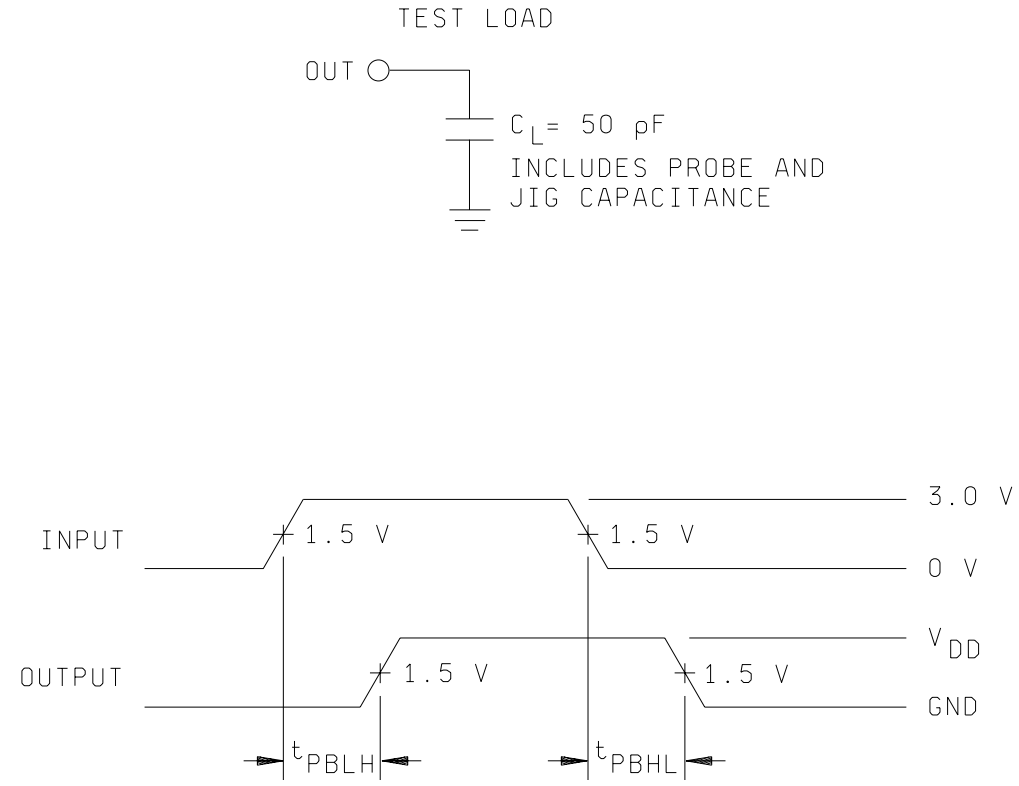
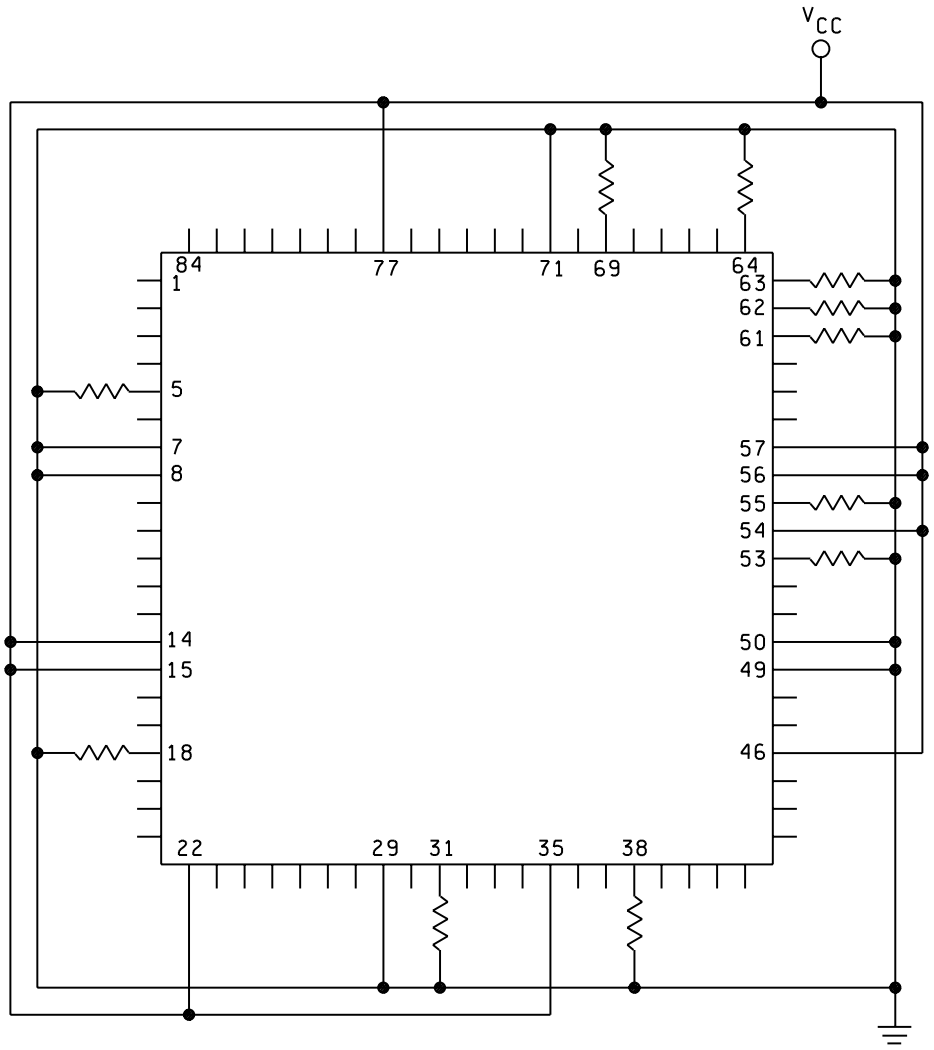


FIGURE 3. Switching test circuit and waveforms.



Note: Resistors are 1kΩ resistors.

FIGURE 4. Radiation exposure circuit.

4.4.1 Continued.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.6 herein).

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The package lid of the DUT is removed so as to provide an unobstructed path to the die for the ion beam.

b. The DUT is biased or exercised as appropriate to that IC being tested.

c. The temperature that SEP tests are conducted at is 25°C +/- 10°C (ambient).

d. Particle penetration range is > 20 microns (Si).

e. The flux used is between 1E2 and 1E5 ions/cm^2/s.

f. The beam incidence angle(s) used are between 0° to 60° from normal.

g. Supply current and voltage(s) as well as SEU, SEL and faults are monitored and recorded in-situ.

h. For SEP test limits, see Table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table IA)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall also verify functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5 ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

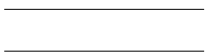
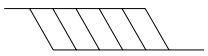
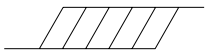
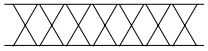
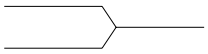
Test 1/	Device types
	All
I_{DD}	±1.0 mA
I_{OZ}	±2.0 µA
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameters shall be recorded before and after the required burn-in and life test to determine the delta.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

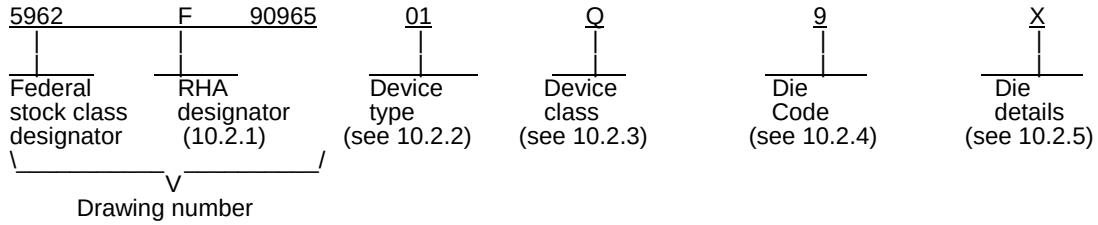
Appendix A

Appendix A forms a part of SMD 5962-90965

10. Scope

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
03	1020B	2000 gate, field programmable gate array	168.2 ns
05	RH1020	2000 gate, field programmable gate array	168.2 ns

10.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
03	254 mils X 267 mils	15±1 mils	A	A-1
05	254 mils X 267 mils	25±1 mils	B	A-1

10.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
03	A	A-1
05	B	A-1

10.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
03	Ti-cap+Al/Cu/Si,9-12kA	None (backgrind)	A	A-1
05	TiW+Al/Cu,9-12kA	None (backgrind)	B	A-1

10.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
03	Ox/Nitride	A	A-1
05	Ox/Nitride/Polyimide	B	A-1

10.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
03	Matsushita Electronics Corp. Japan	A	A-1
05	Lockheed Martin Federal System, VA	B	A-1

10.3 Absolute maximum ratings.
See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.
See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specification, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

30. REQUIREMENTS.

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be specified in 10.2.5.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figure A-1.

30.2.5 Truth table(s). Where technically applicable, (for die) the truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit will be as specified on figure 4 as shown within the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

30.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

30.8.1 Unprogrammed die delivered to the user. All testing shall be verified through wafer probe test as defined in 40.2.

30.8.2 Manufacturer-programmed die delivered to the user. The programming integrity test shall be performed during programming. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4)

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1, and 4.4.4.2 herein.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Pad#	Name	X-Coord	Y-Coord
1	I/O	-2922	2964
2	I/O	-2922	2259
3	I/O	-2922	2003
4	I/O	-2922	1747
5	I/O	-2922	1491
6	I/O	-2922	1251
7	GND	-2922	992
8	GND	-2922	674
9	I/O	-2922	431
10	I/O	-2922	265
11	I/O	-2922	98
12	I/O	-2922	-68
13	I/O	-2922	-253
14	VCC	-2922	-495
15	VCC	-2922	-814
16	I/O	-2922	-1056
17	I/O	-2922	-1223
18	I/O	-2922	-1489
19	I/O	-2922	-1745
20	I/O	-2922	-2001
21	I/O	-2922	-2257
22	VPP, VCC	-2788	-2987
23	I/O	-1912	-3085
24	I/O	-1685	-3085
25	I/O	-1459	-3085
26	I/O	-1233	-3085
27	I/O	-997	-3085
28	I/O	-830	-3085
29	GND	-588	-3085
30	I/O	-345	-3085
31	I/O	-179	-3085
32	I/O	--13	-3085
33	I/O	154	-3085
34	I/O	320	-3085
35	VCC	578	-3085
36	I/O	820	-3085
37	I/O	987	-3085
38	I/O	1222	-3085
39	I/O	1449	-3085
40	I/O	1680	-3085
41	I/O	1907	-3085
42	I/O	2920	-2962
43	I/O	2920	-2257
44	I/O	2920	-2001

Pad#	Name	X-Coord	Y-Coord
45	GND	2920	-1745
46	I/O	2920	-1489
47	I/O	2920	-1248
48	I/O	2920	-1082
49	GND	2920	-839
50	GND	2920	-521
51	I/O	2920	-278
52	I/O	2920	-112
53	I/O, CLK	2920	55
54	I/O	2920	297
55	MODE	2920	463
56	VCC	2920	706
57	VCC	2920	1024
58	I/O	2920	1267
59	I/O	2920	1433
60	I/O	2920	1674
61	I/O, SDI	2920	1930
62	I/O, DCLK	2920	2186
63	I/O, PRA	2920	2442
64	GND	2921	2964
65	I/O, PRB	2041	3087
66	I/O	1830	3087
67	I/O	1603	3087
68	I/O	1372	3087
69	I/O	1146	3087
70	I/O	979	3087
71	I/O	813	3087
72	GND	570	3087
73	I/O	328	3087
74	I/O	161	3087
75	I/O	-5	3087
76	I/O	-172	3087
77	I/O	-338	3087
78	VCC	-580	3087
79	I/O	-823	3087
80	I/O	-989	3087
81	I/O	-1233	3087
82	I/O	-1459	3087
83	I/O	-1685	3087
84	I/O	-1912	3087

NOTES:
1. The center of X-Y coordinate is at the center of the die.
2. All dimensions are in μm.

Figure A-1. A1020B and RH1020 Bond Pad Locations and Functions

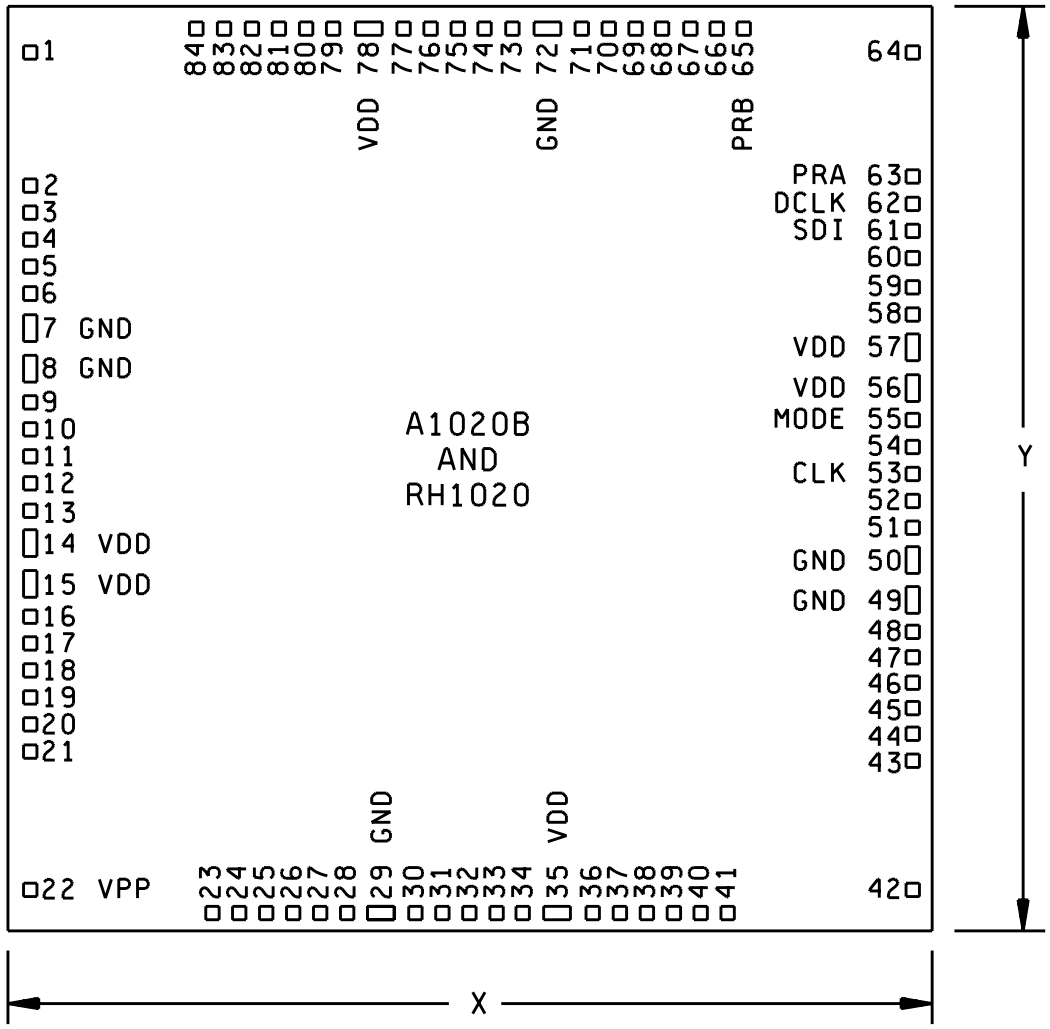


Figure A-1. A1020B and RH1020 Bond Pad Locations and Functions - Continued.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-09-21

Approved sources of supply for SMD 5962-90965 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-9096501MXA	2/	A1020A-JQ44B
5962-9096501MYA	2/	A1020A-JQ68B
5962-9096501MZA	2/	A1020A-JQ84B
5962-9096501MUC	2/ 2/	A1020A-PG84B TPC1020AMGB84B
5962-9096501MTC	2/ 2/	A1020A-CQ84B TPC1020AMHT84B
5962-9096501MMC	2/	TPC1020AMHFG84B
5962-9096502MXA	2/	A1020A-1-JQ44B
5962-9096502MYA	2/	A1020A-1-JQ68B
5962-9096502MZA	2/	A1020A-1-JQ84B
5962-9096502MUC	2/ 2/	A1020A-1-PG84B TPC1020AMGB84B-1
5962-9096502MTC	2/ 2/	A1020A-1-CQ84B TPC1020AMHT84B-1
5962-9096502MMC	2/	TPC1020AMHFG84B-1
5962-9096503MUC	0J4Z0	A1020B-PG84B
5962-9096503MTC	0J4Z0	A1020B-CQ84B
5962-9096503MMC	2/	A1020B-CQ84B
5962-9096504MUC	0J4Z0	A1020B-1PG84B
5962-9096504MTC	0J4Z0	A1020B-1CQ84B
5962-9096504MMC	2/	A1020B-1CQ84B

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962F9096505QTC	0J4Z0	RH1020-CQ84V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Not available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086

The following table lists the SMD part numbers for die.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar 1/ PIN
5962-9096503Q9A	0J4Z0	A1020B-DIE
5962F9096505Q9B	0J4Z0	RH1020-DIE

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086