Z86C66
CMOS Z8® 16K ROM MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C66	16	256	16, 20

* General-Purpose

- 44-Pin QFP Package
- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- –40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C66 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C66 is a member of the Z8 single-chip microcontroller family with 16 Kbytes of ROM and 256 bytes of RAM.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C66 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial, advanced scientific, and **specifically high security applications**.

For applications which demand powerful I/O capabilities, the Z86C66 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

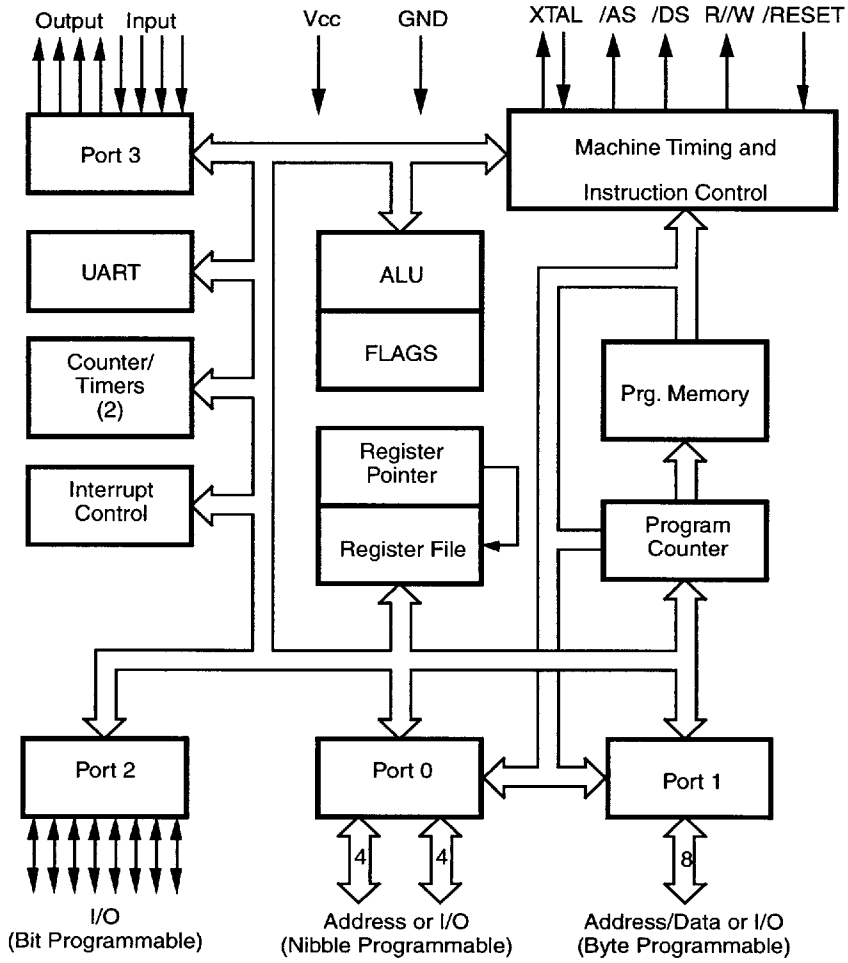
To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C66 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Block Diagrams).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

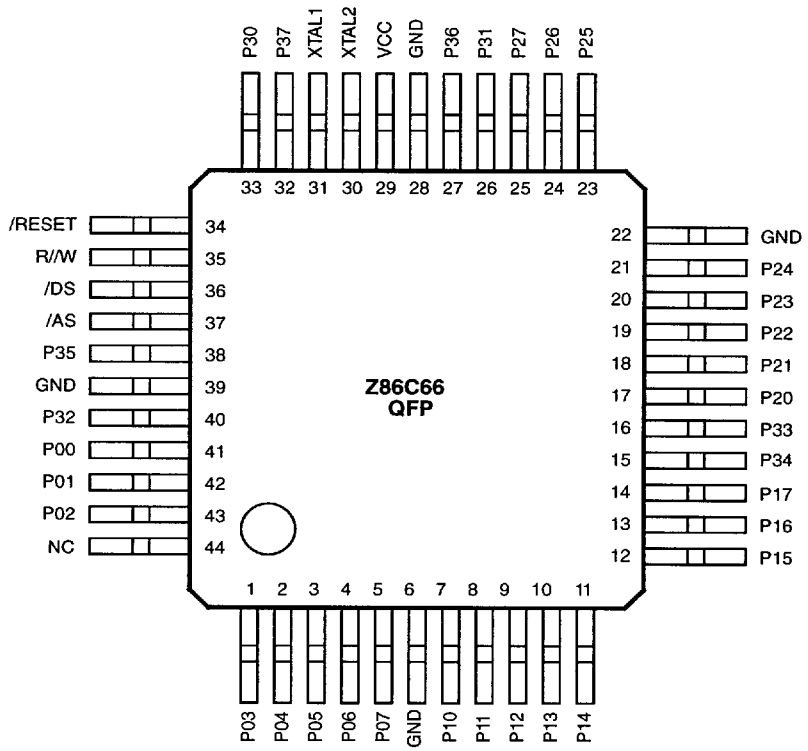
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION



Z86C66 Functional Block Diagram

PIN DESCRIPTIONS



44-Lead QFP Pin Assignments

44-Lead QFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 Pins 3,4,5,6,7	In/Output
6	GND	Ground, GND	Input
7-14	P10-P17	Port 1 Pins 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3 Pin 4	Output
16	P33	Port 3 Pin 3	Input
17-21	P20-P24	Port 2 Pins 0,1,2,3,4	In/Output
22	GND	Ground, GND	Input
23-25	P25-P27	Port 2 Pins 5,6,7	In/Output
26	P31	Port 3 Pin 1	Input
27	P36	Port 3 Pin 6	Output
28	GND	Ground, GND	Input
29	V_{CC}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3 Pin 7	Output
33	P30	Port 3 Pin 0	Input
34	/RESET	Reset	Input
35	R/W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3 Pin 5	Output
39	GND	Ground, GND	Input
40	P32	Port 3 Pin 2	Input
41-43	P00-P02	Port 0 Pins 0,1,2	In/Output
44	NC	No Connect	

ABSOLUTE MAXIMUM RATINGS

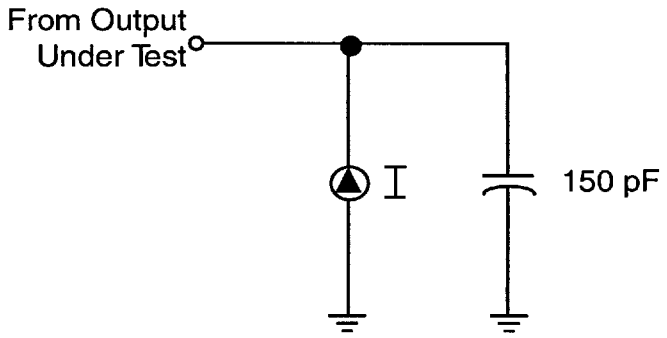
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Z86C66

Sym	Parameter	T_A=0°C to+70°C Min	Max	T_A=–40°C to+105°C Min	Max	Typical at 25°C	Units	Conditions
	MaxInputVoltage		7		7		V	[4]I_{IN}<250µA
V_{CH}	ClockInputHighVoltage	0.85V_{CC}	V_{CC}+0.3	0.85V_{CC}	V_{CC}+0.3		V	DrivenbyExternalClockGenerator
V_{CL}	ClockInputLowVoltage	V_{SS}–0.3	0.8	V_{SS}–0.3	0.8		V	DrivenbyExternalClockGenerator
V_{IH}	InputHighVoltage	2	V_{CC}+0.3	2	V_{CC}+0.3		V	
V_{IL}	InputLowVoltage	V_{SS}–0.3	0.2V_{CC}	V_{SS}–0.3	0.2V_{CC}		V	
V_{OH}	OutputHighVoltage	2.4		2.4			V	I_{OH}=–2.0mA
V_{OH}	OutputHighVoltage		V_{CC}–100mV		V_{CC}–100mV		V	I_{OH}=–100µA
V_{OH}	OutputHighVoltage(LowEMI)	2.4		2.4			V	I_{OH}=–0.5mA
V_{OL}	OutputLowVoltage		0.4		0.4		V	I_{OL}=+5.0mA[3]
V_{OL}	OutputLowVoltage(LowEMI)		0.4		0.4		V	I_{OL}=+2.0mA[3]
V_{OL}	OutputLowVoltage		0.6		0.6		V	I_{OL}=+4.0mA[2]
V_{OL}	OutputLowVoltage(LowEMI)		0.6		0.6		V	I_{OL}=+1.0mA[2]
V_{RH}	ResetInputHighVoltage	0.85V_{CC}	V_{CC}+0.3	0.85V_{CC}	V_{CC}+0.3		V	
V_{RI}	ResetInputLowVoltage	–0.3	0.2V_{CC}	–0.3	0.2V_{CC}		V	
I_{IL}	InputLeakage	–2	2	–2	2		µA	V_{IN}=0V,V_{CC}
I_{OL}	OutputLeakage	–2	2	–2	2		µA	V_{IN}=0V,V_{CC}
I_{RR}	ResetInputCurrent		–180		–180		µA	V_{RL}=0V
I_{CC}	SupplyCurrent(StandardMode)		35		35	24	mA	[1]@16MHz
I_{CC}	SupplyCurrent(StandardMode)		40		40	30	mA	[1]@20MHz
I_{CC}	SupplyCurrent(LowEMI)		6.0			4.0	mA	@4MHz
I_{CC1}	StandbyCurrent(StandardMode)		15		15	4.5	mA	[1]HALTModeV_{IN}=0V,V_{CC}@16MHz
I_{CC1}	StandbyCurrent(LowEMI)		1.6			0.8	mA	@4MHz
I_{CC2}	StandbyCurrent		10		20	5	µA	[1]STOPModeV_{IN}=0V,V_{CC}
I_{ALL}	AutoLatchLowCurrent	–14	14	–20	20	5	µA	

Notes:

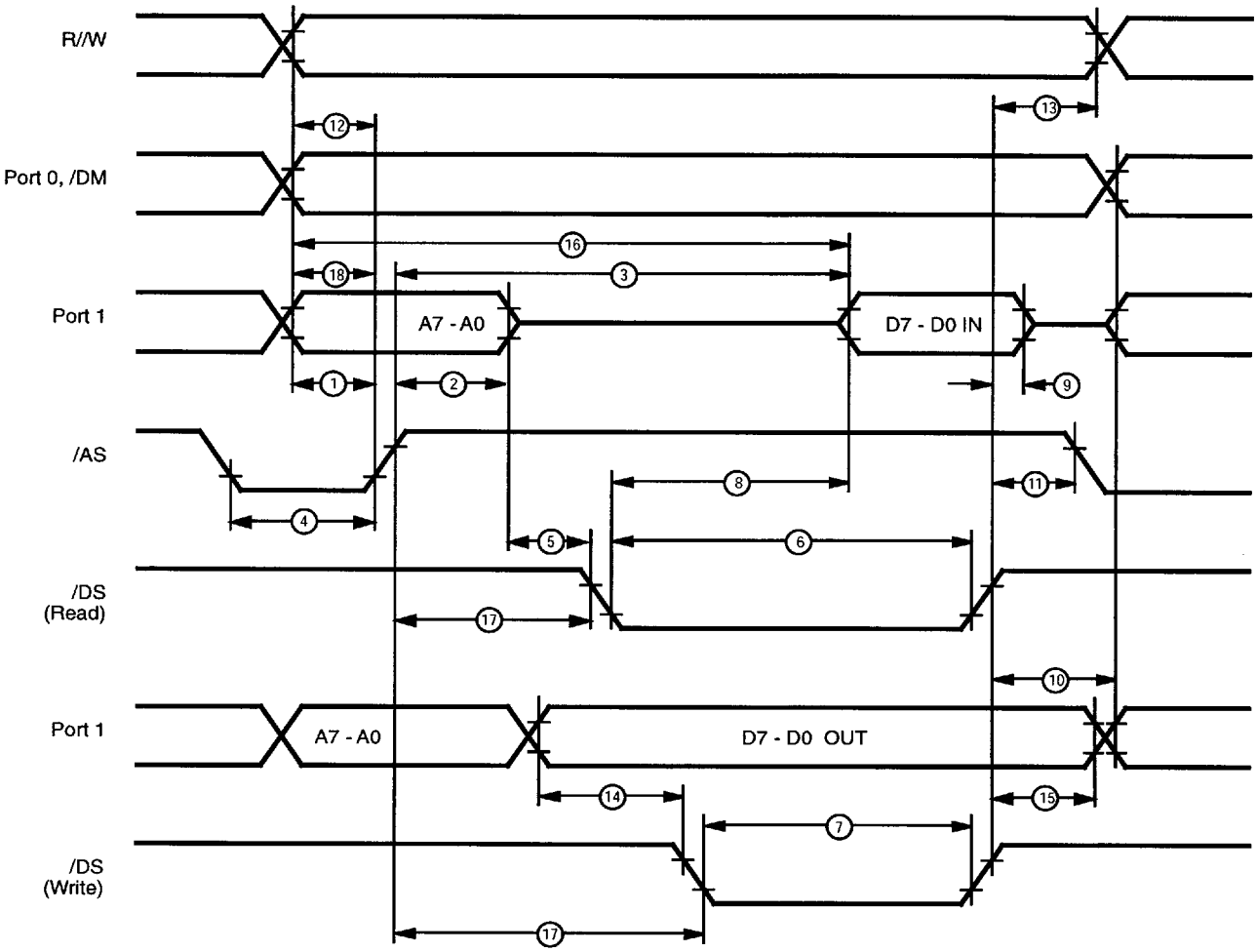
[1] All inputs driven to either 0V or V_{CC}, outputs floating.

[2] V_{CC} = 3.0V to 3.6V

[3] V_{CC} = 4.5V to 5.5V

[4] /Reset pin must be a maximum of V_{CC} + 0.3V.

AC CHARACTERISTICS



External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C66 (16 MHz—Standard Mode Only[4])

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C66 (20 MHz—Standard Mode Only[4])

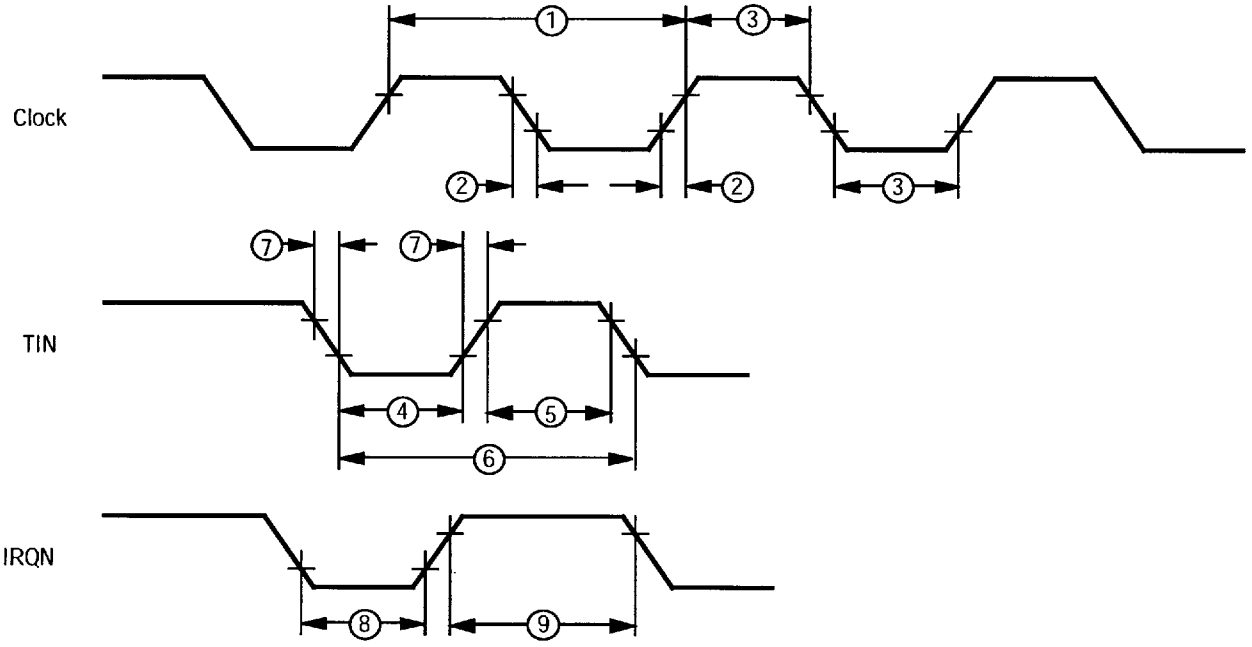
No	Symbol	Parameter	T_A = 0°C to +70°C 20 MHz Min	Max	T_A = –40°C to +105°C 20 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	[1,2,3]
4	TwAS	/AS Low Width	30		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	65		65		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS

Additional Timing Table
Z86C66 (Standard Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	25/31		25/31		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8 a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8 b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:

[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Additional Timing Table
Z86C66 (Low EMI Mode Only)

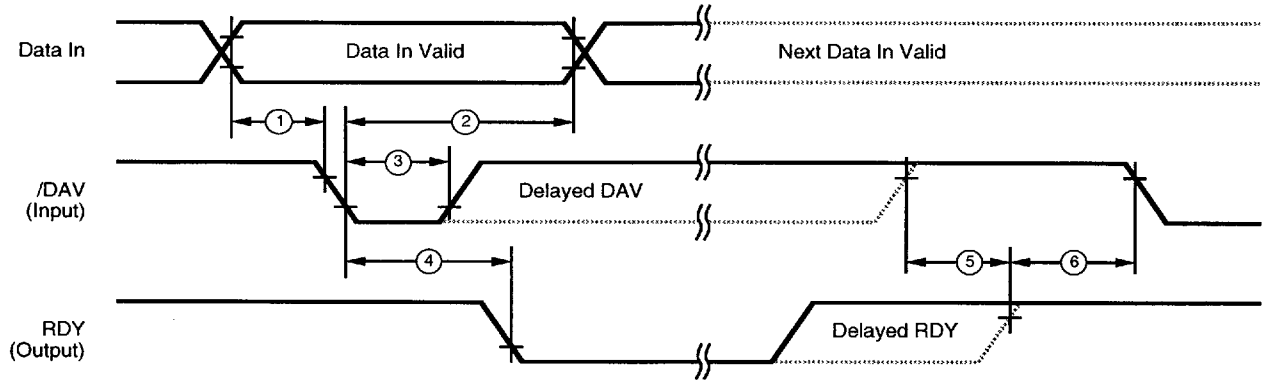
No	Symbol	Parameter	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	250	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	125		125		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	3 TpC		3 TpC		ns	[2]
6	TpTin	Timer Input Period	4 TpC		4 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8 a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8 b	TwIL	Interrupt Request Input Low Times	3 TpC		3 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	3 TpC		3 TpC		ns	[2,3]

Notes:

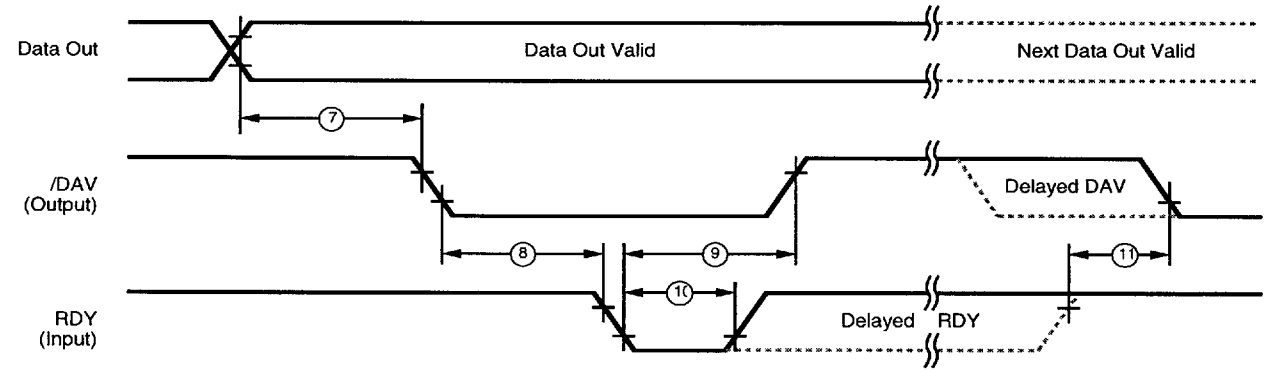
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

Z86C66

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV Fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	115		115		OUT

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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