

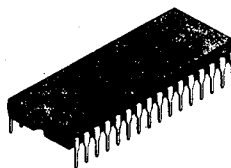
SONY®**CXK581001P/M** -70L/85L
70LL/85LL**131,072-word × 8-bit High Speed CMOS Static RAM****Description**

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAMs organized as 131,072 words by 8-bit and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

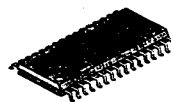
Features

- Fast access time: (Access time)
CXK581001P/M-70L/70LL 70ns (Max.)
CXK581001P/M-85L/85LL 85ns (Max.)
- Low power operation :
CXK581001P/M Standby/Operation
-70L/85L : 10 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
-70LL/85LL : 3.5 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
- Single +5V supply : +5V $\pm$ 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600mil 32 pin DIP package
- CXK581001M 525mil 32 pin SOP package

CXK581001P
32 pin DIP (Plastic)



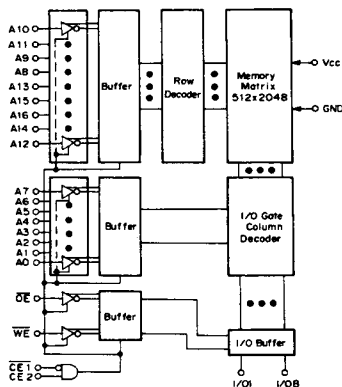
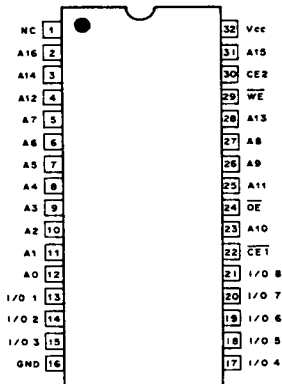
CXK581001M
32 pin SOP (Plastic)

**Function**

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A ₀ to A ₁₆	Address input
I/O ₀ to I/O ₇	Data input/output
CE ₁ , CE ₂	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
V _{cc}	+5V power supply
GND	Ground
NC	No connection

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Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to +7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581001P 1.0	W
		CXK581001M 0.7	
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	- 55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC}
L	H	L	H	Read	Data out	I _{CC}
L	H	x	L	Write	Data in	I _{CC}

x : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics**• DC and operating characteristics**(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

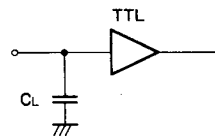
Item	Symbol	Test conditions	- 70L/85L			- 70LL/85LL			Unit
			Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}	- 1	—	1	- 1	—	1	μA
Average operating current	I _{CC}	Cycle=Min, Duty=100% I _{OUT} =0mA	—	47.5	80	—	47.5	80	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	100	—	—	20	μA
			0 to 40 °C	—	20	—	—	4	
			+25 °C	—	2	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	1.2	3	—	1.2	3	mA
Output high voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C**I/O capacitance**(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****• AC test conditions**(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	C _L *=100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	ns
Address access time	t _{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t _{CO2}	—	70	—	85	ns
Output enable to output valid	t _{OE}	—	40	—	45	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} , t _{HZ2} *	—	25	—	25	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	25	—	25	ns

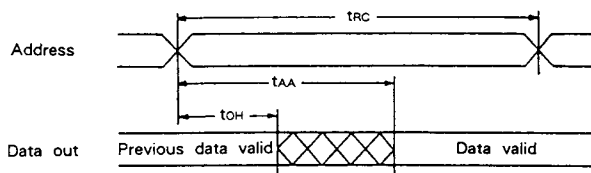
* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

• Write cycle

Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	ns
Address valid to end of write	t _{AW}	60	—	75	—	ns
Chip enable to end of write	t _{CW}	60	—	75	—	ns
Data to write time overlap	t _{DW}	25	—	30	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	60	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$, CE1)	t _{WR}	5	—	5	—	ns
Write recovery time (CE2)	t _{WR1}	10	—	10	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	—	25	—	30	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

- Read cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



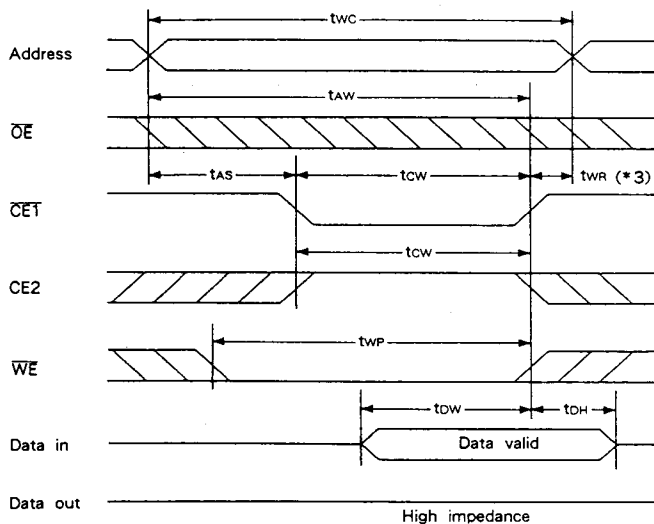
The diagram illustrates the timing characteristics of the 74VHC04 inverter. It shows the Address signal, which is a square wave with a rise/fall time t_{RC} . The Access time t_{AA} is the time from the start of the Address signal to the output becoming valid. The output is shown as a square wave with a delay t_{CO1} and a low-to-high transition time t_{LZ1} when the output is low, and a high-to-low transition time t_{HZ1} when the output is high. The output is also shown as a square wave with a delay t_{CO2} and a low-to-high transition time t_{LZ2} when the output is low, and a high-to-low transition time t_{HZ2} when the output is high. The output is shown as a square wave with a delay t_{OE} and a low-to-high transition time t_{LZ} when the output is low, and a high-to-low transition time t_{HZ} when the output is high. The output is shown as a square wave with a delay t_{OE} and a low-to-high transition time t_{LZ} when the output is low, and a high-to-low transition time t_{HZ} when the output is high. The output is shown as a square wave with a delay t_{OE} and a low-to-high transition time t_{LZ} when the output is low, and a high-to-low transition time t_{HZ} when the output is high.

The diagram illustrates the timing relationships for the 247 device. It shows the following signals and their timing parameters:

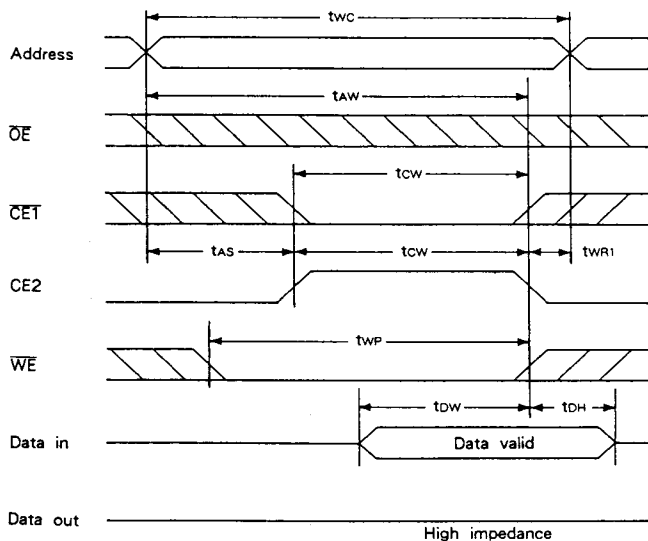
- Address:** Valid for t_{WC} (write cycle) and t_{AW} (address-to-write delay). Setup time before $\overline{OE}$ is t_{WR} (*3).
- $\overline{OE}$:** Output Enable signal, shown as a pulse.
- $\overline{CE1}$:** Chip Enable 1 signal, shown as a pulse.
- $\overline{CE2}$:** Chip Enable 2 signal, shown as a pulse.
- $\overline{WE}$:** Write Enable signal, shown as a pulse. Setup time before $\overline{WE}$ is t_{AS} . Pulse width is t_{WP} (*1).
- Data in:** Data input signal. Valid for t_{OW} (output write delay) and t_{DH} (data hold time).
- Data out:** Data output signal. Setup time before $\overline{OE}$ is t_{WHZ} (*2). After $\overline{OE}$, it goes to high impedance for t_{OW} (*2).

Additional labels include (*1), (*2), and (*3) indicating specific timing conditions or notes.

• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): $\overline{CE2}$ control



* 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and $\overline{CE2}$ is at high simultaneously.

* 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

* 3. t_{WR} is tested from the rising edge of $\overline{WE}$ or $\overline{CE1}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

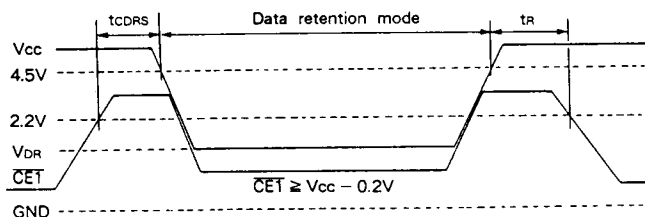
Item	Symbol	Test conditions	- 70L/85L			- 70LL/85LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =0.3V * 1	0 to 70 °C	—	50	—	—	12	μA
			0 to 40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	—	0.7	20	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

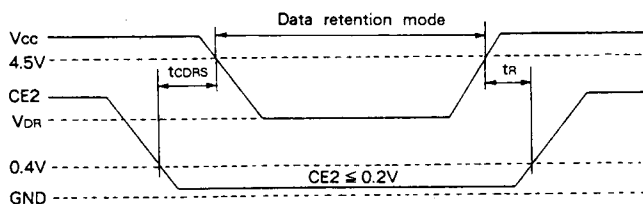
* 2. t_{RC} : Read cycle time

Data retention waveform

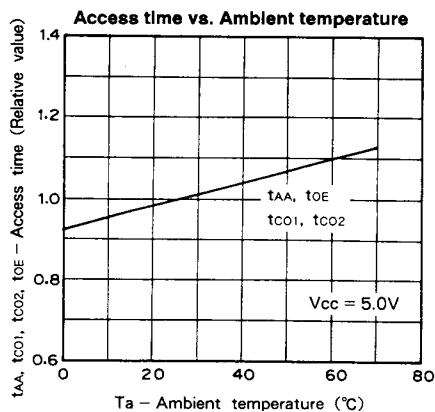
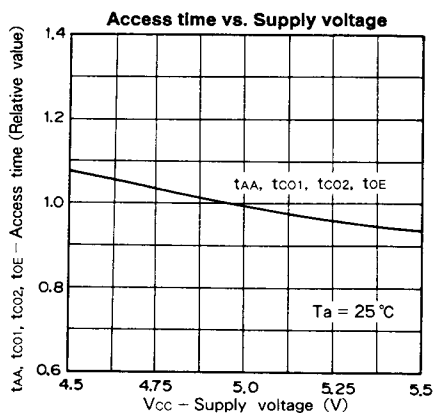
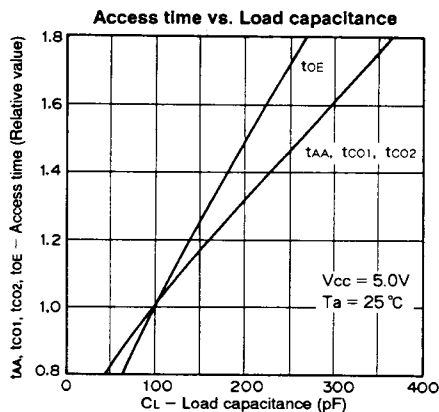
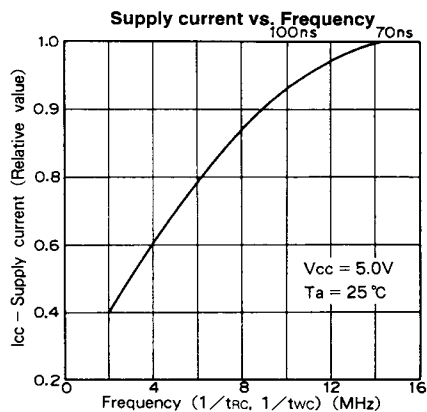
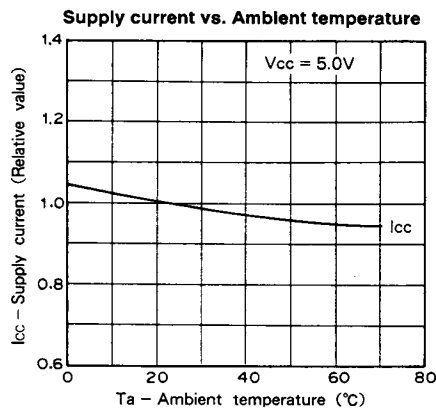
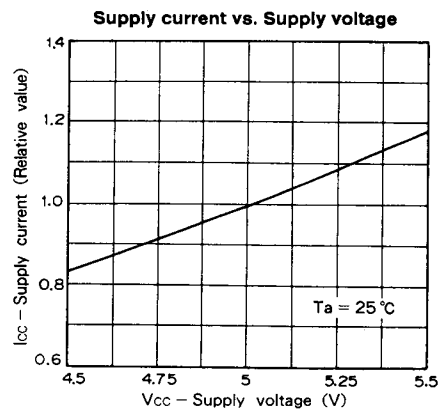
- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



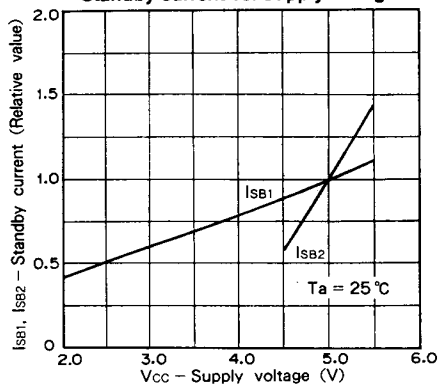
- Low supply voltage data retention waveform (2) ($CE2$ control)



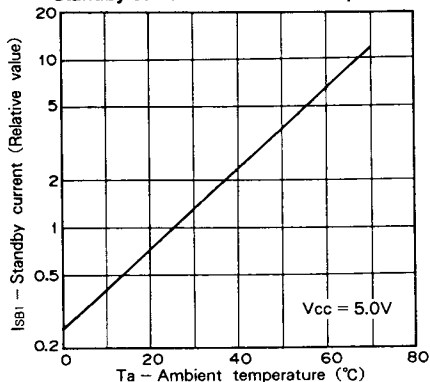
Example of Representative Characteristics



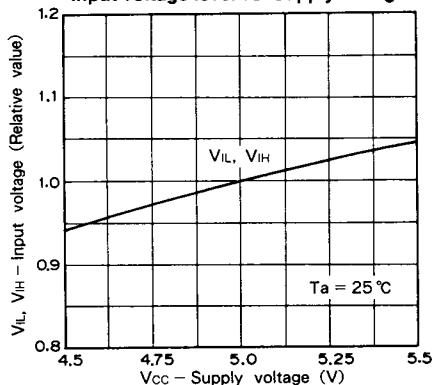
Standby current vs. Supply voltage



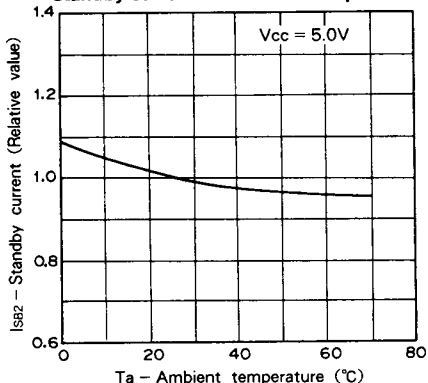
Standby current vs. Ambient temperature



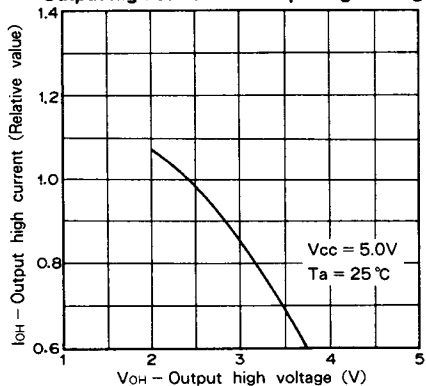
Input voltage level vs. Supply voltage



Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage

