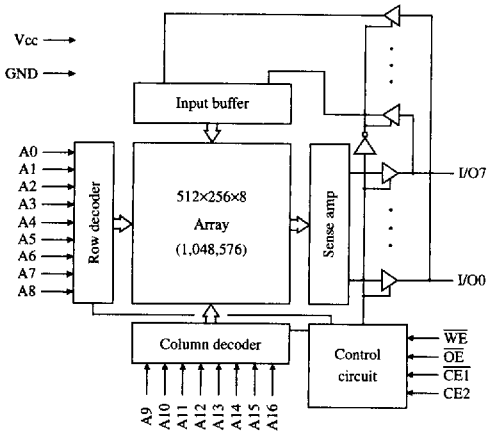
128K×8 CMOS SRAM (Common I/O)

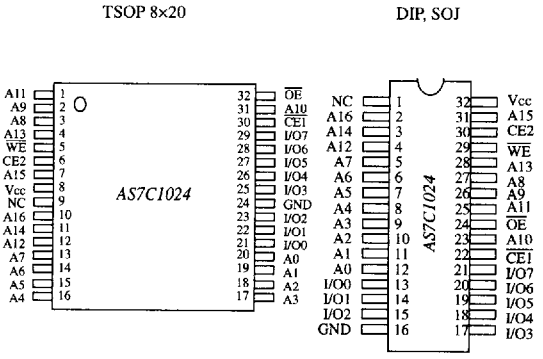
Features

- Organization: 131,072 words × 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Low power consumption
  - Active: 660 mW max (15 ns cycle)
  - Standby: 27.5 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
    Socket compatible with 7C512 (64K×8)
  - 400 mil SOJ
  - 8×20 TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 3.3V and 5.0V versions available
- Industrial and commercial temperature available

Logic block diagram



Pin arrangement



Selection guide

		7C1024-10 –	7C1024-12 7C31024-12	7C1024-15 7C31024-15	7C1024-20 7C31024-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		3	3	4	5	ns
Maximum operating current	AS7C1024	175	160	120	110	mA
	AS7C31024	–	100	70	65	mA
Maximum CMOS standby current		5	5	5	5	mA

Shaded areas contain advance information.

DID 11-20000-*A.

Functional description

The AS7C1024 and AS7C31024 are high performance CMOS 1,048,576-bit Static Random Access Memories (SRAM) organized as 131,072 words × 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 3/3/4/5 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. The standard AS7C1024 is guaranteed not to exceed 27.5 mW power consumption in standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled withoutput enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL/LVTTL-compatible, and operation is from a single 5V supply (AS7C1024) or 3.3V supply (AS7C31024). The AS7C1024 and AS7C31024 are packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	−0.5	+7.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1024	V_{CC}	4.5	5.0	5.5	V
	AS7C31024	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C1024	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C31024	V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}	−0.5	–	0.8	V

†V_{IL} min = −3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics [1]

Parameter	Symbol	Test conditions		-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{CC} = Max, V_{out} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, f = f_{max}, I_{out} = 0 mA	AS7C1024	–	175	–	160	–	120	–	110	mA
			AS7C31024	–	–	–	100	–	70	–	65	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, f = f_{max}		–	55	–	50	–	40	–	40	mA
	I_{SB1}	$\overline{CE1}$ ≥ V_{CC}−0.2V or CE2 ≤0.2V, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}−0.2V, f = 0		–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = −4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas contain advance information.

Capacitance [2]

(f = 1 MHz, T_a = Room temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Read cycle [3,9,12]

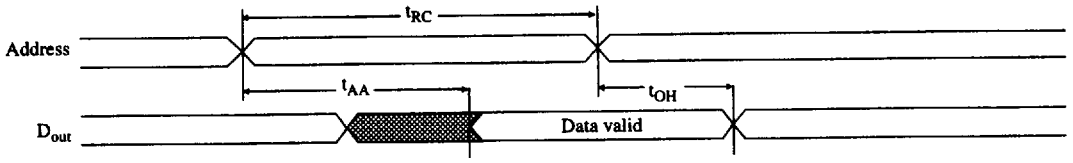
Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit	Notes
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	–	10	–	12	–	15	–	20	ns	3, 12
Chip enable (CE2) access time	t_{ACE2}	–	10	–	12	–	15	–	20	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	3	–	4	–	5	ns	
Output hold from address change	t_{OH}	2	–	3	–	3	–	3	–	ns	5
$\overline{CE1}$ LOW to output in Low Z	t_{CLZ1}	3	–	3	–	3	–	3	–	ns	4, 5, 12
CE2 HIGH to output in Low Z	t_{CLZ2}	3	–	3	–	3	–	3	–	ns	4, 5, 12
$\overline{CE1}$ HIGH to output in High Z	t_{CHZ1}	–	3	–	3	–	4	–	5	ns	4, 5, 12
CE2 LOW to output in High Z	t_{CHZ2}	–	3	–	3	–	4	–	5	ns	4, 5, 12
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}	–	3	–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5, 12
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5, 12

Key to switching waveforms

Rising input Falling input Undefined output/don't care

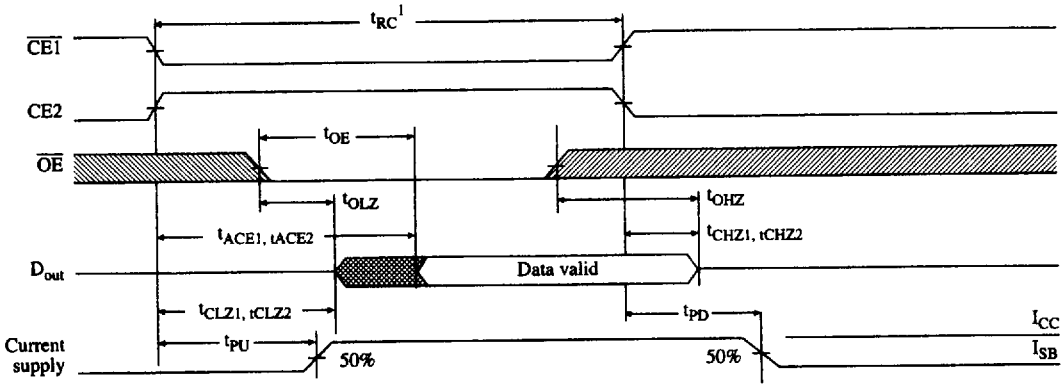
Read waveform 1 [3,6,7,9,12]

Address controlled



Read waveform 2 [3,6,8,9,12]

$\overline{CE1}$ and CE2 controlled



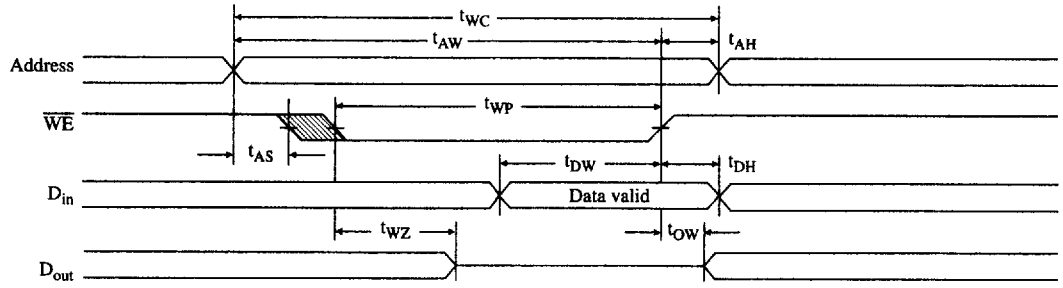
Write cycle [11, 12]

Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit	Notes
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	9	–	10	–	12	–	12	–	ns	12
Chip enable (CE2) to write end	t_{CW2}	9	–	10	–	12	–	12	–	ns	12
Address setup to write end	t_{AW}	9	–	10	–	12	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	6	–	6	–	9	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5

Shaded areas contain advance information.

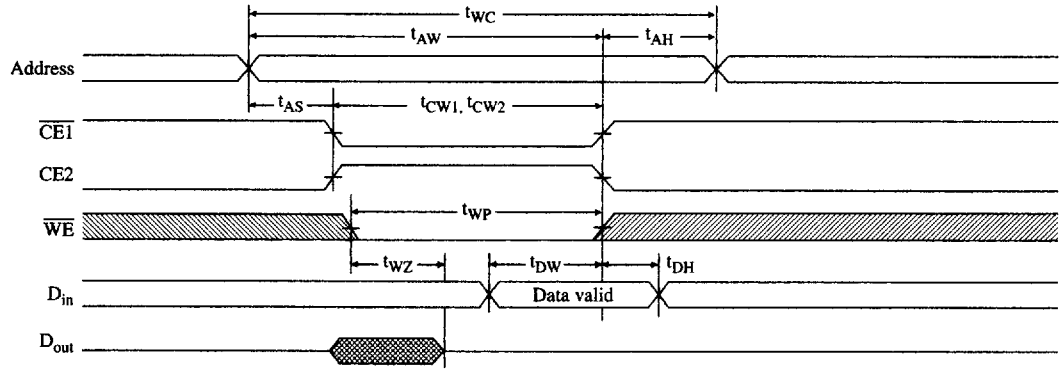
Write waveform 1 *10,11,12*

$\overline{WE}$ controlled



Write waveform 2 *10,11,12*

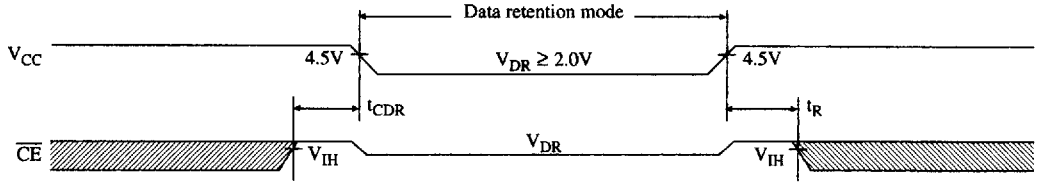
$\overline{CE1}$ and CE2 controlled



Data retention characteristics *14*

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE1} \geq V_{CC}$–0.2V or	–	500	µA
Chip deselect to data retention time	t_{CDR}	CE2 ≤ 0.2V	0	–	ns
Operation recovery time	t_R	$V_{in} \geq V_{CC}$–0.2V or	t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$	$V_{in} \leq$ 0.2V	–	1	µA

Data retention waveform



AC test conditions

- 5V output load: see Figure B, except as noted see Figure C.
- 3.3V output load: see Figure D, except as noted see Figure E.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

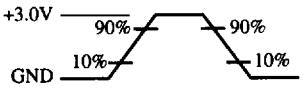


Figure A: Input waveform

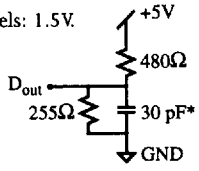


Figure B: Output load

Thevenin equivalent:

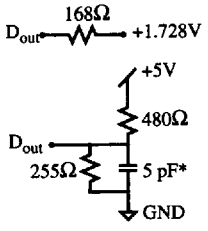


Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

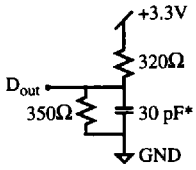


Figure D: Output load

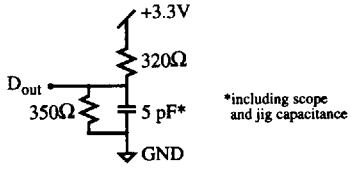


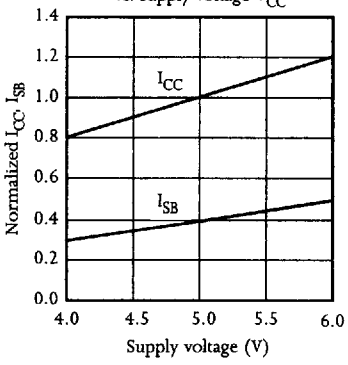
Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Notes

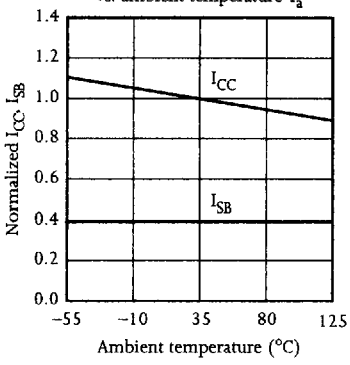
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.
13 This data applicable to the AS7C1024. The AS7C31024 functions similarly.
14 2V data retention applies to commercial tempoerature operating range only.

Typical DC and AC characteristics

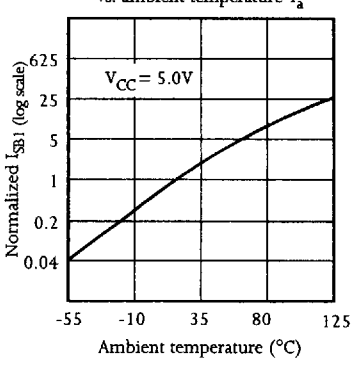
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



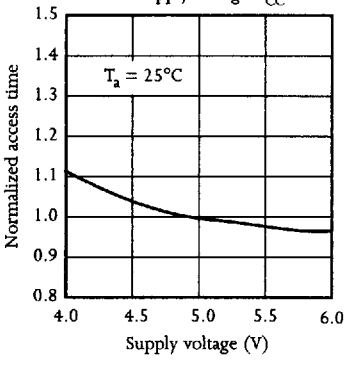
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



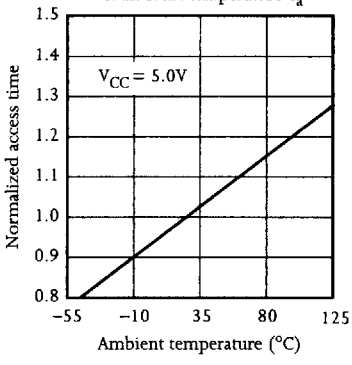
Normalized supply current I_{SB1} vs. ambient temperature T_a



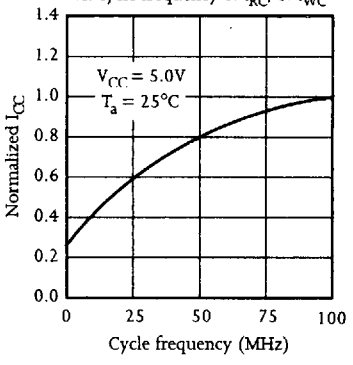
Normalized access time t_{AA} vs. supply voltage V_{CC}



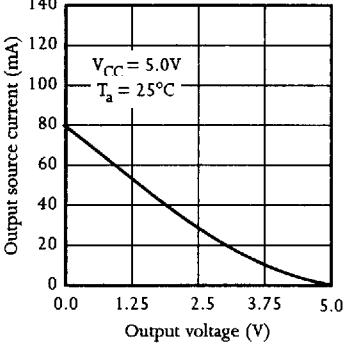
Normalized access time t_{AA} vs. ambient temperature T_a



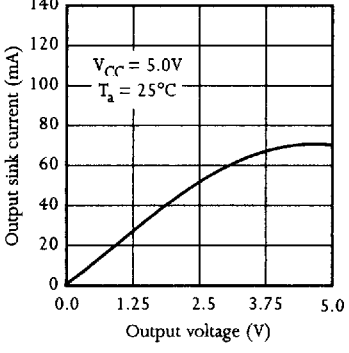
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



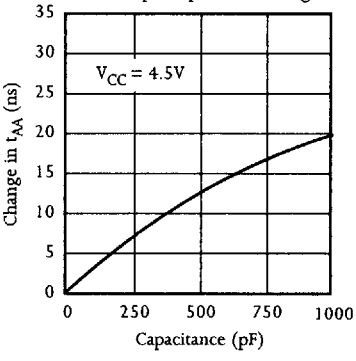
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



AS7C1024 ordering codes

Package \ Access time	10 ns	12 ns	15 ns	20 ns
Plastic DIP, 300 mil		AS7C1024-12TPC	AS7C1024-15TPC	AS7C1024-20TPC
		AS7C31024-12TPC	AS7C31024-15TPC	AS7C31024-20TPC
Plastic SOJ, 300 mil	AS7C1024-10TJC	AS7C1024-12TJC	AS7C1024-15TJC	AS7C1024-20TJC
		AS7C31024-12TJC	AS7C31024-15TJC	AS7C31024-20TJC
			AS7C31024-15TJI	AS7C31024-20TJI
Plastic SOJ, 400 mil	AS7C1024-10JC	AS7C1024-12JC	AS7C1024-15JC	AS7C1024-20JC
			AS7C1024-15JI	AS7C1024-20JI
		AS7C31024-12JC	AS7C31024-15JC	AS7C31024-20JC
			AS7C31024-15JI	AS7C31024-20JI
TSOP 8×20		AS7C1024-12TC	AS7C1024-15TC	AS7C1024-20TC
		AS7C31024-12TC	AS7C31024-15TC	AS7C31024-20TC

Shaded areas contain advance information.

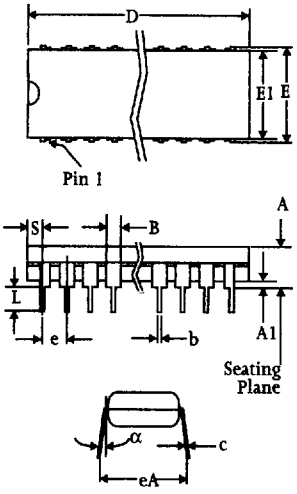
AS7C1024 part numbering system

AS7C	X	1024	–XX	X	X
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package:TP =PDIP 300 milT =TSOP 8×20 J =SOJ 400 milTJ =SOJ 300 mil	Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C

Plastic dual in-line package (PDIP)

	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil		32-pin 600 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Max
A	-	0.175	-	0.175	-	0.180	-	0.200	-	0.210
A1	0.010	-	0.010	-	0.015	-	0.015	-	0.010	-
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065	0.048	0.054
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022	0.016	0.022
c	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015	0.008	0.014
D	-	0.980	-	1.400	-	1.571	-	1.620	-	1.660
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425	0.590	0.610
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390	0.545	0.555
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.430	0.470	0.630	0.670
L	0.110	0.130	0.120	0.140	0.110	0.142	0.118	0.162	0.12	0.14
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	-	0.040	-	0.055	-	0.043	-	0.065	-	0.085

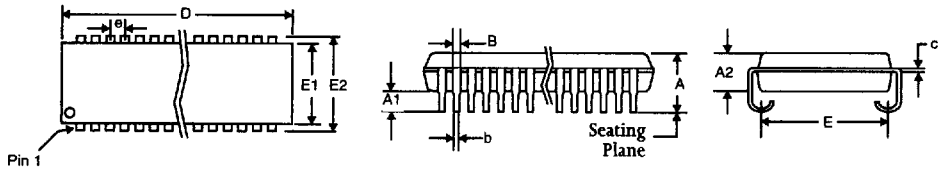
Dimensions in inches



Plastic small outline J-bend (SOJ)

	20/26-pin 300 mil		24/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		28-pin 400 mil		32-pin 400 mil		36-pin 400 mil		40-pin 400 mil		42-pin 400 mil		44-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.140	-	0.148	-	0.140	-	0.145	0.132	0.146	-	0.145	-	-	-	0.145	0.128	0.148	0.128	0.148
A1	0.020	-	0.026	-	0.025	-	0.025	-	0.062	-	0.025	-	-	-	0.025	-	0.025	-	0.025	-
A2	0.095	0.105	0.106 NOM		0.095	0.105	0.086	0.105	0.105	115	0.086	0.115	0.102 NOM		0.086	0.115	1.105	1.115	1.105	1.115
B	0.025	0.032	0.015	0.020	0.028 TYP		0.026	0.032	0.024	0.032	0.026	0.032	-	0.032	0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.028 NOM		0.018 TYP		0.014	0.020	0.013	0.021	0.015	0.020	0.013	0.021	0.015	0.022	0.015	0.020	0.015	0.020
c	0.008	0.014	0.006	0.008	0.010 TYP		0.006	0.013	0.005	0.012	0.007	0.013	-	-	0.007	0.014	0.007	0.013	0.007	0.013
D	-	0.686	0.670	0.680	-	0.730	0.820	0.830	0.720	0.729	0.820	0.830	0.920	0.930	1.015	1.035	1.070	1.080	1.120	1.130
E	0.245	0.285	0.255	0.275	0.245	0.285	0.250	0.275	0.354	0.378	0.360	0.380	0.350	0.390	0.348	0.390	0.370 NOM		0.370 NOM	
E1	0.295	0.305	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405	0.400 NOM		0.395	0.405	0.395	0.405	0.395	0.405
E2	0.327	0.347	0.328	0.339	0.327	0.347	0.330	0.340	0.430	0.440	0.435	0.445	0.435	0.445	0.435	0.445	0.435	0.445	0.435	0.445
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.045	0.055	0.050 BSC		0.050 NOM		0.050 NOM	

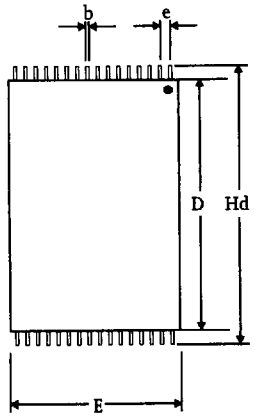
Dimensions in inches

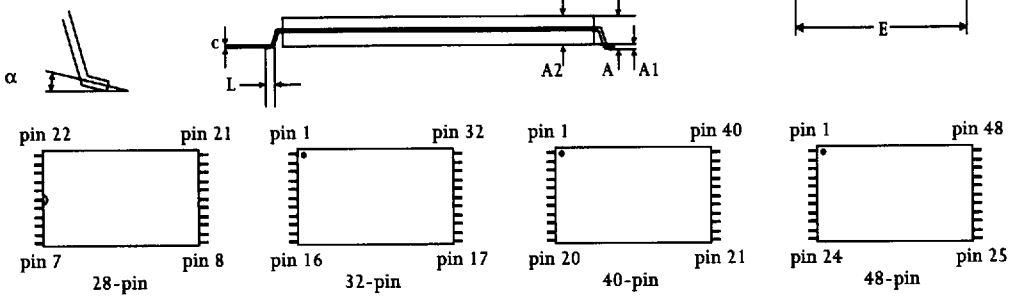


Thin small outline package (TSOP-I)

	28-pin 8×13.4		32-pin 8×20		40-pin 10×20		48-pin 12×20	
	Min	Max	Min	Max	Min	Max	Min	Max
A	–	1.20	–	1.20	–	1.20	–	1.27
A1	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.20
A2	0.90	1.05	0.90	1.05	0.95	1.05	0.95	1.05
b	0.17	0.27	0.17	0.23	0.17	0.27	0.1	0.3
c	0.10	-	0.10	-	0.10	0.20	0.15 nominal	
D	11.70	11.90	18.20	18.60	18.30	18.50	18.30	18.50
e	0.55 nominal		0.50 nominal		0.50 nominal		0.50 nominal	
E	8.0 nominal		7.80	8.20	9.90	10.10	11.90	12.10
Hd	13.20	13.60	19.80	20.20	19.80	20.20	19.80	20.20
L	0.30	0.70	0.40	0.60	0.50	0.70	0.40	0.60
α	0°	5°	1°	5°	0°	5°	0°	5°

Dimensions in millimeters

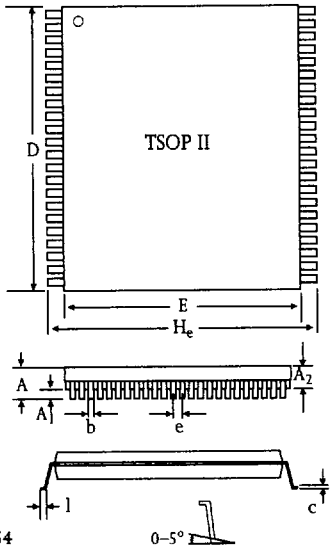


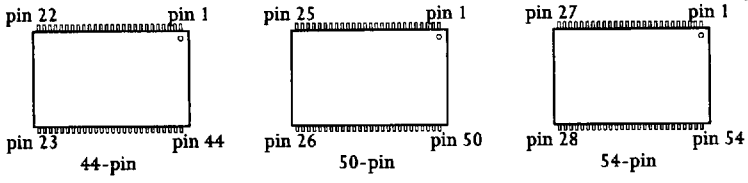


Thin small outline package (TSOP II)

	44-pin TSOP II		50-pin TSOP II		54-pin TSOP II	
	Min (mm)	Max (mm)	Min (mm)	Max (mm)	Min (mm)	Max (mm)
A	–	1.2	–	1.2	–	1.2
A_1	0.05	–	0.05	–	0.05	–
A_2	0.95	1.05	0.95	1.05	0.95	1.05
b	0.25	0.45	0.25	0.45	0.25	0.45
c	0.15 (typical)		0.10	0.25	0.10	0.25
D	18.31	18.51	20.85	21.05	22.22	22.72
E	10.06	10.26	10.06	10.26	10.06	10.26
e	0.80 (typical)		0.80 (typical)		0.80 (typical)	
H_e	11.56	11.96	11.56	11.96	11.56	11.96
l	0.40	0.60	0.40	0.60	0.40	0.60

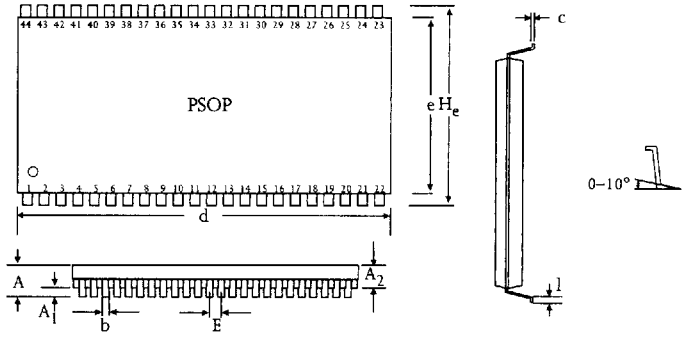
*ranges encompass both 44/50 and 50/50 pin configurations.





Plastic small outline package (PSOP)

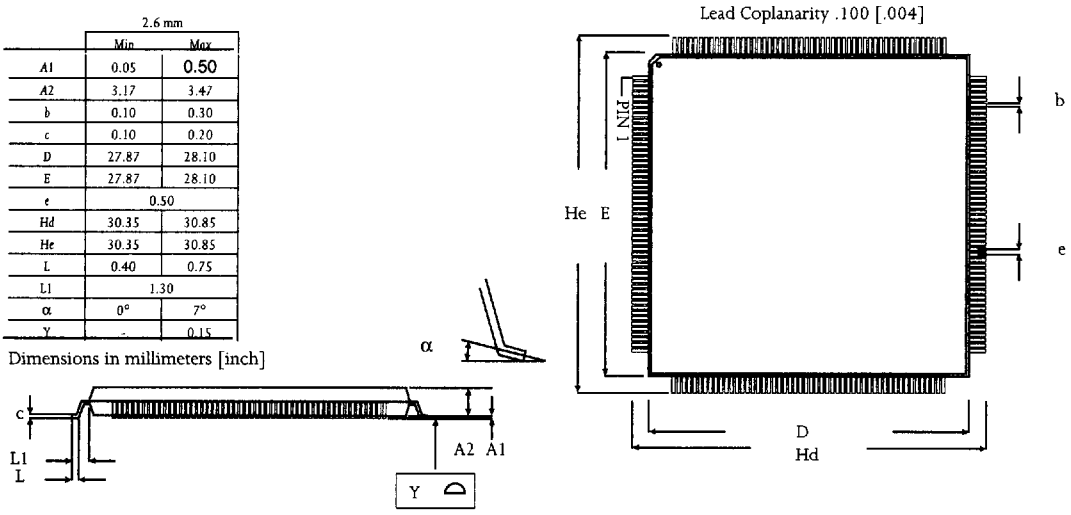
	44-pin PSOP	
	Min (mm)	Max (mm)
A	–	3.00
A_1	0.10	–
A_2	2.57	2.81
b	0.35	0.50
c	0.20 (typical)	
d	28.37	28.63
e	12.47	12.72
E	1.27 (typical)	
H_e	15.74	16.34
l	0.6	1.0



208-pin plastic quad flat pack (PQFP)

	2.6 mm	
	Min	Max
A1	0.05	0.50
A2	3.17	3.47
b	0.10	0.30
c	0.10	0.20
D	27.87	28.10
E	27.87	28.10
e	0.50	
Hd	30.35	30.85
He	30.35	30.85
L	0.40	0.75
L1	1.30	
α	0°	7°
Y	-	0.15

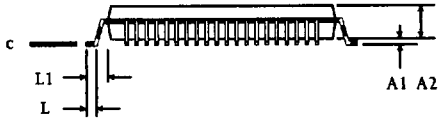
Dimensions in millimeters [inch]

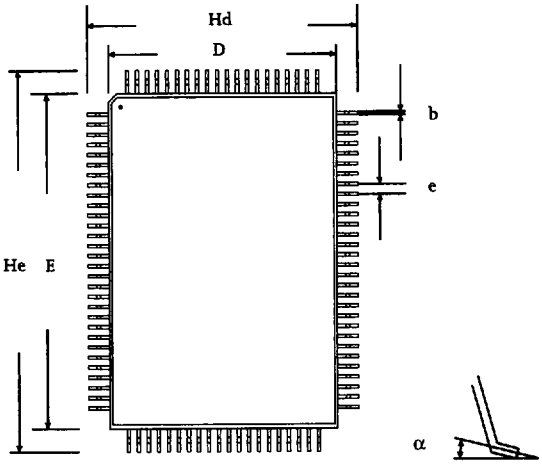


100-pin quad flat pack (PQFP and TQFP)

	(P)QFP		TQFP	
	Min	Max	Min	Max
A1	0.25	0.45	0.05	0.15
A2	2.57	2.87	1.35	1.45
b	0.20	0.40	0.22	0.38
c	0.10	0.20	0.09	0.20
D	13.90	14.10	13.90	14.10
E	19.90	20.10	19.90	20.10
e	0.65 nominal		0.65 nominal	
Hd	17.00	17.40	15.90	16.10
He	23.00	23.40	21.90	22.10
L	0.65	0.95	0.45	0.75
L1	1.60 nominal		1.00 nominal	
α	0°	10°	0°	7°

Dimensions in millimeters



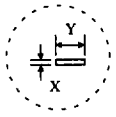


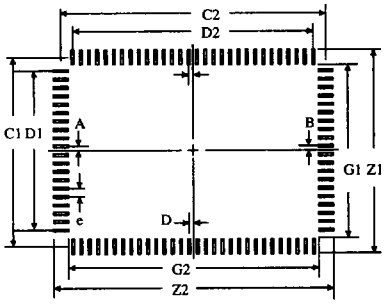
100-pin PQFP and TQFP PCB land pattern

Symbol	Description	TQFP/PQFP Min	Max
C1	Reference	15.98 ref.	
C2	Reference	21.98 ref.	
D1	Reference	12.35 ref.	
D2	Reference	18.85 ref.	
e	Pad pitch	0.65	
G1	Pad inner dimension	13.69	13.79
G2	Pad inner dimension	19.69	19.79
N	Pad count	100	
X	Pad width	0.35	0.38
Y	Pad length	2.24 ref.	
Z1	Pad outer dimension	18.16	18.26
Z2	Pad outer dimension	24.16	24.26

Controlling dimension: mm.

This land pattern accommodates both PQFP and TQFP packages.

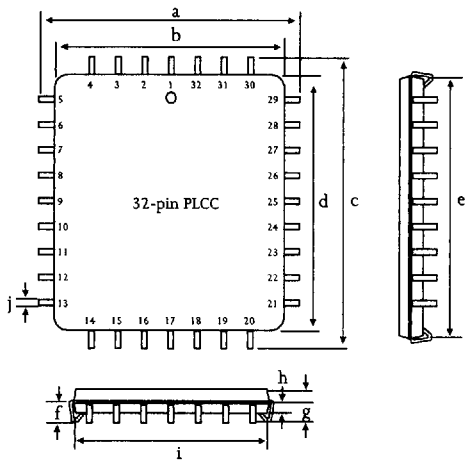




Notes on land pattern

1 Pad requirement to accommodate two package types is larger than for one package type.
2 All dimensioning and tolerancing conform to ANSI Y14.5M-1982. Dimensions in mm.
3 Datums A--B and --D-- to be determined from the center two leads.
4 Based on the surface mount Design and Land Pattern Standard in IPC-SM-782 rev. A, subsection 11.3, 8/93 for PQFP.

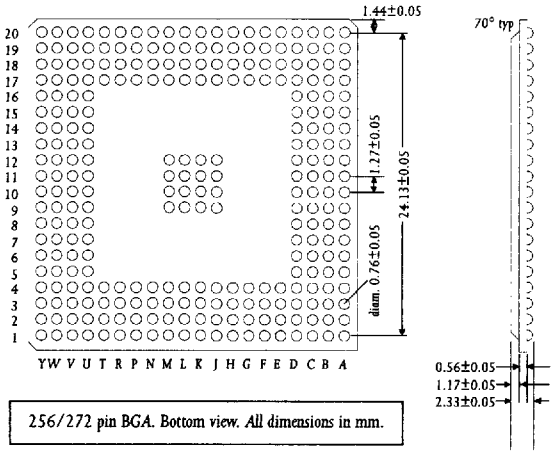
Plastic leaded chip carrier (PLCC)



	32-pin PLCC typical (inch)
a	0.49
b	0.45
c	0.59
d	0.55
e	0.51
f	0.09
g	0.14
h	0.11
i	0.41
j	0.004

JEDEC outline	MS-016 AE
Body size	0.450 in. × 0.550 in.
Package thickness	0.110 in.
Board standoff	0.020 in. (min)
Lead pitch	0.050 in.
Coplanarity	0.004 in. (max)

Plastic ball grid array (PBGA) package dimensions



256/272 pin BGA. Bottom view. All dimensions in mm.