High Performance
32K×9
CMOS SRAM

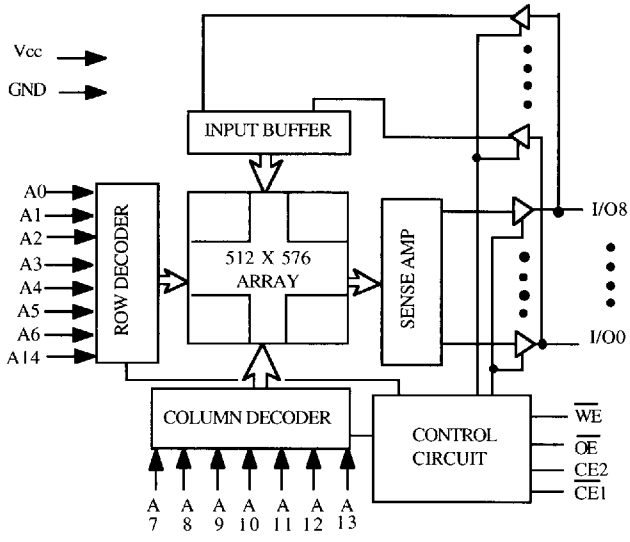
AS7C259
AS7C259L

32K×9 CMOS SRAM (Common I/O)

FEATURES

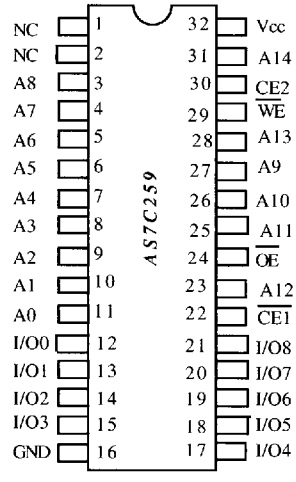
- Organization: 32,768 words x 9 bits
- High Speed - Industry's fastest $\overline{OE}$ Access Time
  12/15/20/25/35 ns Address access time
  4/4/5/6/8 ns Output Enable access time
- Very Low Power
  Active 605mW (max) at 12ns cycle time
  Standby: 55mW TTL I/O
  11mW CMOS I/O
- Power dissipation reduces to 125mW at 10MHz
- Ideal for modem, LAN, 16/32 bit notebook, laptop and palmtop applications
  75% power dissipation reduction during CPU idle or suspend mode
- Extremely Low DC component in Active power
  Power reduces significantly as a function of frequency
- 2.0V data retention (L version)
- Two Chip Enable controls
- TTL compatible I/O
- Completely static memory - No clocks or timing strobe required
- Equal access and cycle times
- Available packages, 32 pin:
  300 mil PDIP
  300 mil SOJ
  8 x 14 TSOP
- JEDEC standard compatible pinout
- ESD protection exceeds 2000 volts
- Latch-up current ≥200mA

LOGIC BLOCK DIAGRAM



PIN ARRANGEMENT

DIP and SOJ



SELECTION GUIDE

		7C259-12	7C259-15	7C259-20	7C259-25	7C259-35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)		110	105	100	90	80
	L	105	100	95	85	75
Maximum Standby Current (mA)		2.0	2.0	2.0	2.0	2.0
	L	0.2	0.2	0.2	0.2	0.2

FUNCTIONAL DESCRIPTION

The AS7C259 is a high-performance CMOS 294,912 bit Static Random Access Memory (SRAM) organized as 32,768 words of 9 bits. It is designed for memory applications where high performance, low power, and simple interfacing are required. When ($\overline{CE1}$) is high or (CE2) is low, this device automatically goes to standby mode consuming very low power. In standby mode, the AS7C259 is guaranteed not to exceed 11mW for the standard part and 1.1mW for the L version.

The L version typically consumes less than 500µW and offers battery-backup data retention capability at Vcc=2.0V. Power consumption in this mode will not exceed 200µW. The chip is ideal for portable computers and other low-power applications.

In addition, the AS7C259 has a significant advantage over the competition with respect to active current during CPU idle, CPU suspend and CPU clock stretch modes. This is accomplished because the active current drops by 75% after the intial access thereby making this part ideal for laptop, palmtop, modem and local area network applications.

The address access time tAA of 12/15/20/25/35ns with output enable ($\overline{OE}$) access time of 4/4/5/6/8ns is ideal for high performance applications. Easy memory expansion is provided by an active low chip enable ($\overline{CE1}$) and an active high chip enable (CE2).

When chip enable ($\overline{CE1}$) and write enable ($\overline{WE}$) are low and (CE2) is high, writing into the device is accomplished. Data on the input pins (I/O0 - I/O8) is written into the memory location identified by address pins A0 through A14. Output enable ($\overline{OE}$) may be kept HIGH during writing to minimize bus-contention.

Reading is implemented by taking chip enable ($\overline{CE1}$) and output enable ($\overline{OE}$) LOW, (CE2) and write enable ($\overline{WE}$) HIGH. The contents of the memory location specified by address pins A0 through A14 will appear on the nine I/O pins (I/O0 - I/O8). The output pins stay in high-impedance mode when chip enable ($\overline{CE1}$) or output enable ($\overline{OE}$) is HIGH, or when (CE2) or write enable ($\overline{WE}$) is LOW.

All AS7C259 inputs and outputs are TTL-compatible. The AS7C259 is a fully static asynchronous circuit which requires no clock for refresh or operation. Equal access and cycle time make for easy use.

The AS7C259 is packaged in all high volume industry standard plastic packages.

ABSOLUTE MAXIMUM RATINGS *

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to GND		Vt	-0.5 to +7.0	V
Power Dissipation		Pd	1.0	W
Storage Temperature	Plastic	Tstg	-55 to +150	℃
Temperature Under Bias		Tbias	-10 to +85	℃
DC Output Current		Iout	20	mA

*NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O	MODE
H	X	X	X	HIGH Z	Standby (Isb,Isb1)
L	H	H	H	HIGH Z	Output Disable
L	H	H	L	Dout	Read
L	H	L	X	Din	Write
X	L	X	X	HIGH Z	Standby (Isb,Isb1)

KEY: X=Don't Care
L=Low
H=High
Z=High Impedence

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	VIH	2.2	--	6.0	V
	VIL	-0.5*	--	0.8	V

DC AND OPERATING CHARACTERISTICS [1] (Vcc = 5V±10%, GND = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Test Conditions		-12		-15		-20		-25		-35		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Leakage Current	|ILI|	Vcc = Max., Vin = GND to Vcc		--	1	--	1	--	1	--	1	--	1	uA
Output Leakage Current	|ILO|	$\overline{CE1}$=VIH | CE2=VIL Vcc=Max Vout = GND to Vcc		--	1	--	1	--	1	--	1	--	1	uA
Operating Power Supply Current	Icc	$\overline{CE1}$=VIL, CE2 = VIH Iout = 0 mA (f=fmax)		--	110	--	105	--	100	--	90	--	80	mA
			L	--	105	--	100	--	95	--	85	--	75	mA
Standby Power Supply Current	Isb	CE1=VIH, or CE2 = VIL f=fmax		--	10	--	10	--	10	--	10	--	10	mA
			L	--	8	--	8	--	8	--	8	--	8	mA
	Isb1	$\overline{CE1}$≥Vcc-0.2V;CE2≤ 0.2v f=0 Vin ≤ 0.2V		--	2.0	--	2.0	--	2.0	--	2.0	--	2.0	mA
		Vin ≥ Vcc - 0.2V	L	--	0.2	--	0.2	--	0.2	--	0.2	--	0.2	mA
Output Voltage	VOL	IOL = 8mA, Vcc = Min.		--	0.4	--	0.4	--	0.4	--	0.4	--	0.4	V
	VOH	IOH = -4.0mA, Vcc=Min.		2.4	--	2.4	--	2.4	--	2.4	--	2.4	--	V

CAPACITANCE [2] (f = 1 MHz, Ta = Room Temperature, Vcc = 5V)

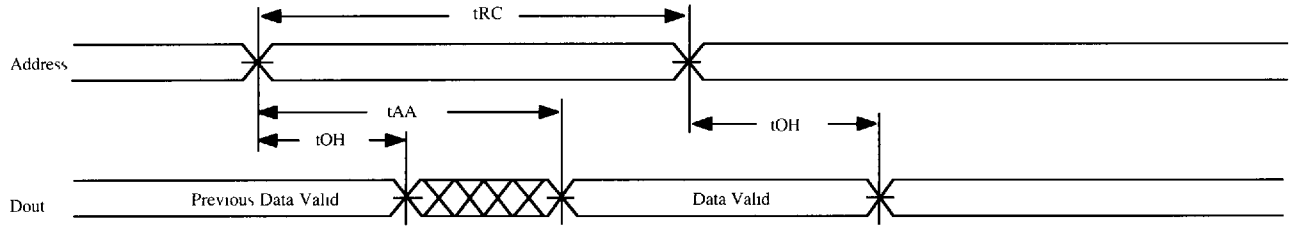
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	Cin	Vin = 0 V	--	--	5	pF
Output Capacitance	Cout	Vout = 0 V	--	--	7	pF

* VIL min. = -3.0V for pulse width less than 10ns

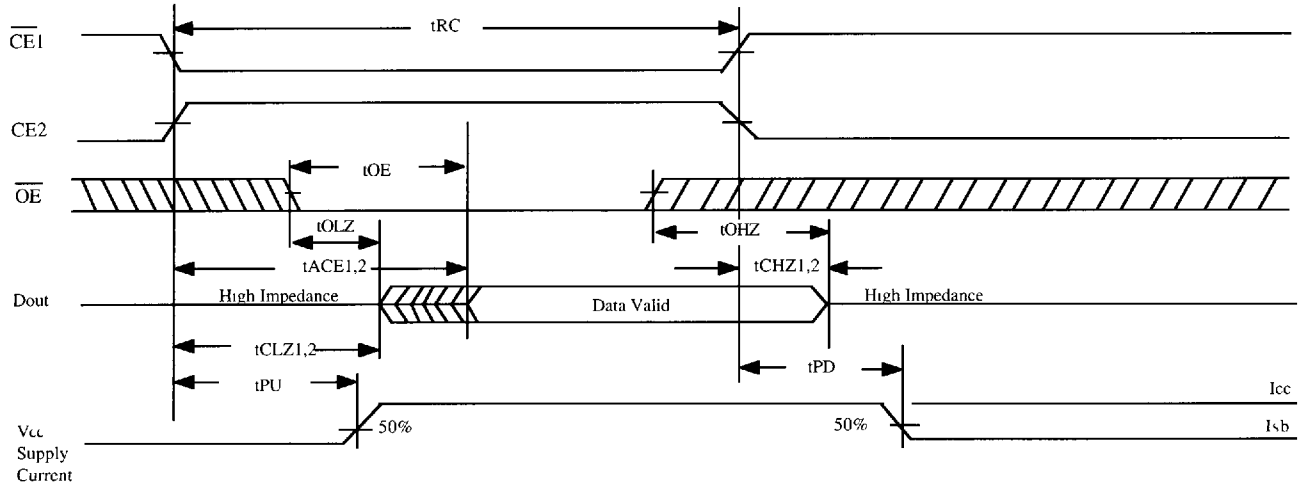
READ CYCLE [0, 3, 11] (Vcc = 5.0V ± 10%, GND = 0V, Ta = 0°C to +70°C)

#	Std Symbol	Parameter	-12		-15		-20		-25		-35		Units	Notes
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max	Min.	Max		
1	tRC	Read Cycle Time	12	-	15	-	20	-	25	-	35	-	ns	
2	tAA	Address Access Time	-	12	-	15	-	20	-	25	-	35	ns	3
3	tACE1	Chip Enable ($\overline{CE1}$) Access Time	-	12	-	15	-	20	-	25	-	35	ns	
4	tACE2	Chip Enable (CE2) Access Time	-	12	-	15	-	20	-	25	-	35	ns	
5	tOE	Output Enable Access Time	-	4	-	4	-	5	-	6	-	8	ns	
6	tOH	Output Hold from Address Change	3	-	3	-	3	-	3	-	3	-	ns	5
7	tCLZ1	Chip Enable ($\overline{CE1}$) Low to Output in Low Z	3	-	3	-	3	-	3	-	3	-	ns	4, 5
8	tCLZ2	Chip Enable (CE2) High to Output in Low Z	3	-	3	-	3	-	3	-	3	-	ns	
9	tCHZ1	Chip Enable ($\overline{CE1}$) High to Output in High Z	-	4	-	4	-	5	-	6	-	8	ns	4, 5
10	tCHZ2	Chip Enable (CE2) Low to Output in High Z	-	4	-	4	-	5	-	6	-	8	ns	
11	tOLZ	Output Enable Low to Output in Low Z	0	-	0	-	0	-	0	-	0	-	ns	4, 5
12	tOHZ	Output Enable High to Output in High Z	-	4	-	4	-	5	-	6	-	8	ns	4, 5
13	tPU	Chip Enable to Power Up Time	0	-	0	-	0	-	0	-	0	-	ns	4, 5
14	tPD	Chip Disable to Power Down Time	-	12	-	15	-	20	-	25	-	35	ns	

TIMING WAVEFORM OF READ CYCLE NO. 1 [3,6,7,11] (Address Controlled, $\overline{CE1}$ and CE2 Active)



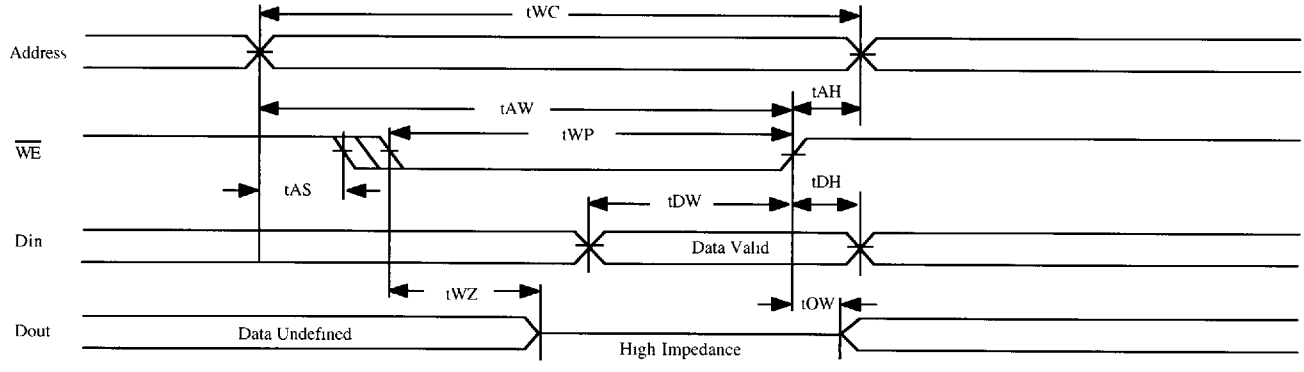
TIMING WAVEFORM OF READ CYCLE NO. 2 [3,6,8,11] ($\overline{CE1}$ and CE2 Controlled)



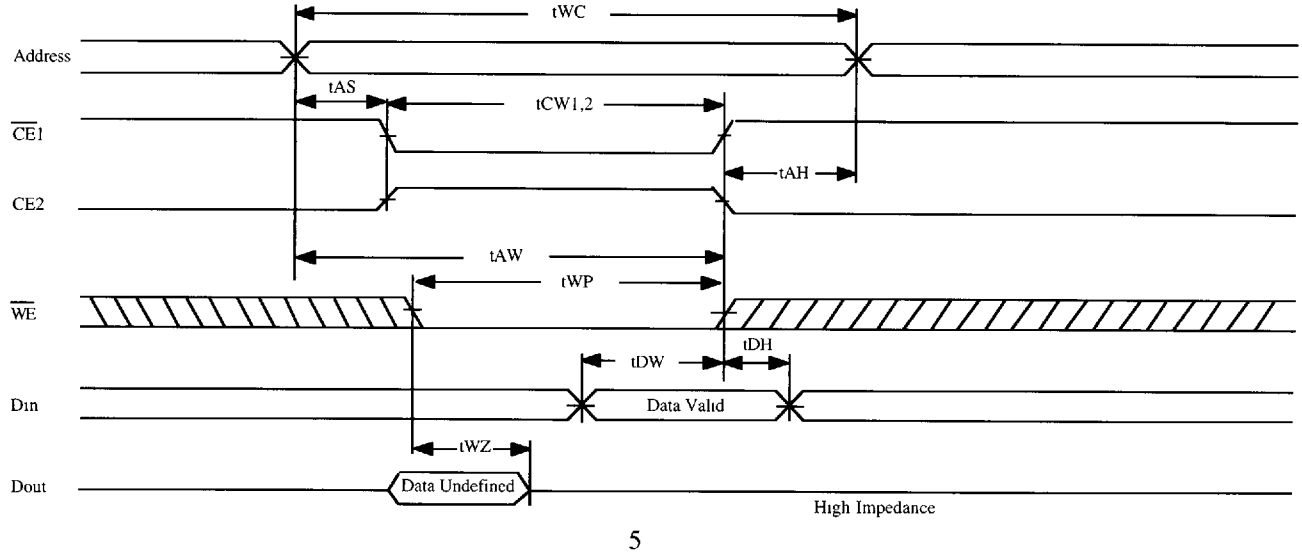
WRITE CYCLE [0, 3, 10] (Vcc = 5V ± 10%, GND = 0V, Ta = 0°C to +70°C)

#	Std. Symbol	Parameter	-12		-15		-20		-25		-35		Units	Notes
			Min.	Max.	Min.	Max	Min.	Max.	Min	Max.	Min.	Max.		
15	tWC	Write Cycle Time	12	–	15	–	20	–	20	–	30	–	ns	
16	tCW1	Chip Enable ($\overline{CE1}$) to Write End	9	–	10	–	12	–	15	–	20	–	ns	
17	tCW2	Chip Enable (CE2) to Write End	9	–	10	–	12	–	15	–	20	–	ns	
18	tAW	Address Set-up to Write End	9	–	10	–	12	–	15	–	20	–	ns	
19	tAS	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns	
20	tWP	Write Pulse Width	9	–	9	–	12	–	15	–	17	–	ns	
21	tAH	Address Hold From End of Write	0	–	0	–	0	–	0	–	0	–	ns	
22	tDW	Data Valid to Write End	9	–	9	–	12	–	15	–	15	–	ns	
23	tDH	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns	4,5
24	tWZ	Write Enable to Output in High Z	–	5	–	5	–	5	–	5	–	5	ns	4,5
25	tOW	Output Active from Write End	3	–	3	–	3	–	3	–	3	–	ns	4,5

TIMING WAVEFORM OF WRITE CYCLE NO. 1 [9] ($\overline{WE}$ Controlled)



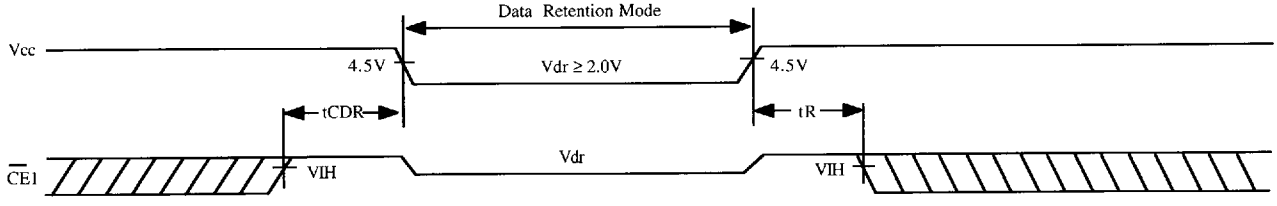
TIMING WAVEFORM OF WRITE CYCLE NO. 2 [9] ($\overline{CE1}$ and CE2 Controlled)



DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
Vdr	Vcc for Data Retention	Vcc = 2.0V $\overline{CE1}$ ≥ Vcc-0.2V or CE2 ≤ 0.2V Vin ≥ Vcc-0.2V or Vin ≤ 0.2V	2	--	V
Iccdr	Data Retention Current		--	100	uA
tCDR	Chip Deselect to Data Retention Time		0	--	ns
tR	Operation Recovery Time		tRC	--	ns
|ILI|	Input Leakage Current		--	1	uA

DATA RETENTION WAVEFORM (L Version Only) ; CE2 Low



AC TEST LOADS AND WAVEFORMS

AC Test Conditions:

- Input Pulse Levels: GND to 3.0V (Figure A)
- Input Rise and Fall Times: 5ns (Figure A)
- Input and Output Timing Reference Levels: 1.5V
- Output Load: See Figures B and C

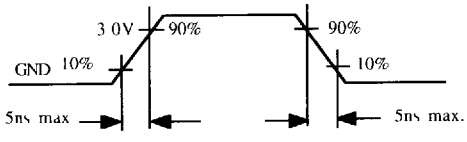


Fig. A Input Waveform

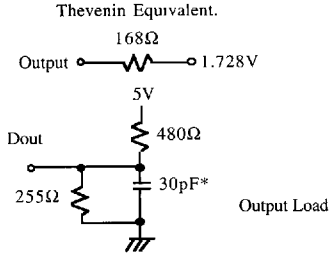


Fig. B Output Load

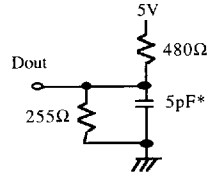


Fig. C Output Load

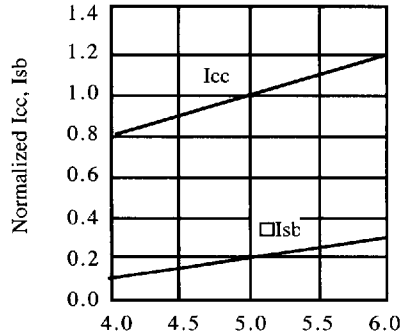
*Including scope and jig capacitance

NOTES

1 During Vcc power-up, a pull-up resistor to Vcc on the $\overline{CE1}$ or a pull down resistor on CE2 is required to meet Isb specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see AC Test Loads and Waveforms, Figures A , B and C
4. tCLZ and tCHZ are specified with CL = 5pF as in Figure C Transition is measured ±500mV from steady-state voltage
5 This parameter is guaranteed but not tested
6 $\overline{WE}$ is high for read cycle
7 $\overline{CE1}$ and $\overline{OE}$ are low for read cycle, CE2 is high
8 Address valid prior to or coincident with $\overline{CE1}$, or CE2 whichever is the later active transition
9. $\overline{CE1}$ or $\overline{WE}$ must be high or CE2 low during Address transitions
10 All write cycle timings are referenced from the last valid address to the first transitioning address
11 All read cycle timings are referenced from the last valid address to the first transitioning address.

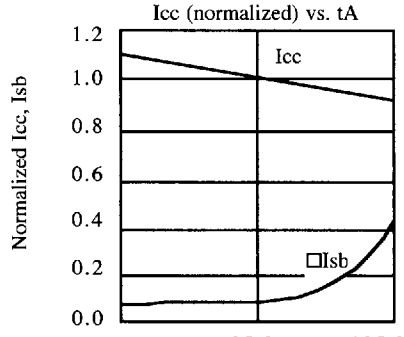
TYPICAL DC and AC CHARACTERISTICS

Normalized Supply Current
vs. Supply Voltage
Icc (normalized) vs. Vcc



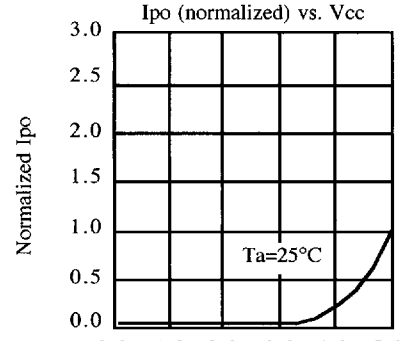
Graph #1

Normalized Supply Current
vs. Ambient Temperature
Icc (normalized) vs. tA



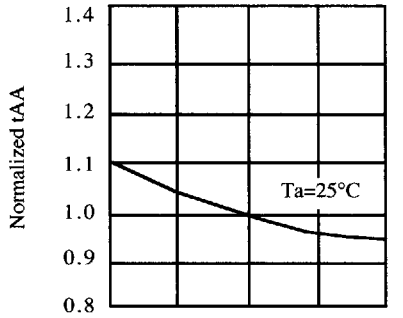
Graph #2

Typical Power On Current
vs. Supply Voltage
Ipo (normalized) vs. Vcc



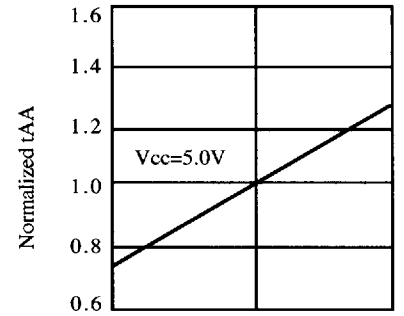
Graph #3

Normalized Access Time
vs. Supply Voltage
tAA (normalized) vs. Vcc



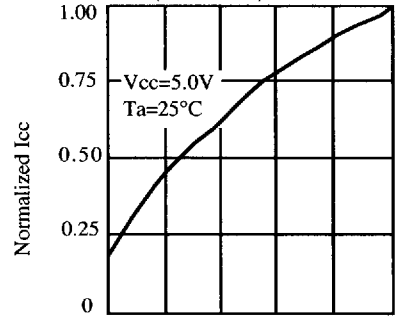
Graph #4

Normalized Access Time
vs. Ambient Temperature
tAA (normalized) vs. Ta



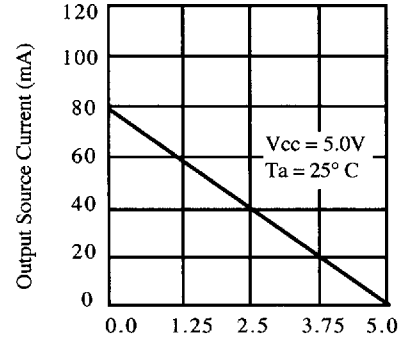
Graph #5

Normalized Icc
vs. Cycle Time
Icc (normalized) tRC or tWC



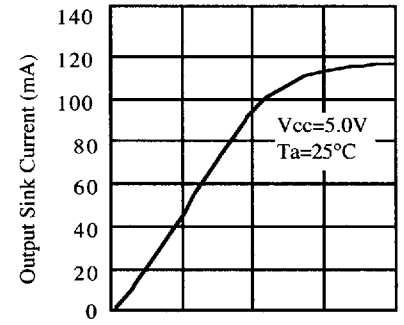
Graph #6

Output Source Current
vs. Output Voltage
IOH vs. VOH



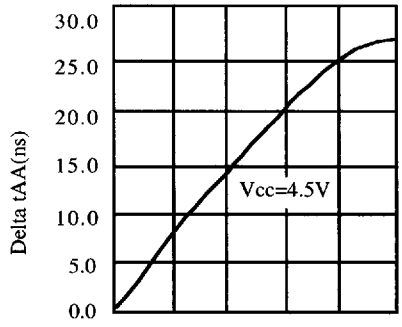
Graph #7

Output Sink Current
vs. Output Voltage
IOL vs. VOL



Graph #8

Typical Access Time Change
vs. Output Loading
tAA vs. CL

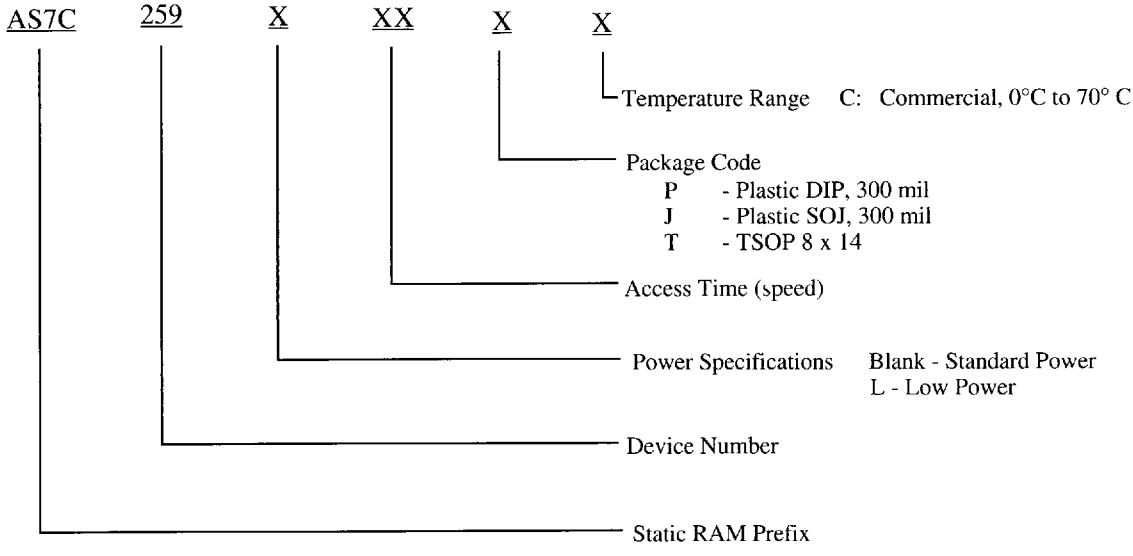


Graph #9

ORDERING INFORMATION

Speed	12ns	15ns	20ns	25ns	35ns
Ordering Code	AS7C259-12PC AS7C259L-12PC	AS7C259-15PC AS7C259L-15PC	AS7C259-20PC AS7C259L-20PC	AS7C259-25PC AS7C259L-25PC	AS7C259-35PC AS7C259L-35PC
	AS7C259-12JC AS7C259L-12JC	AS7C259-15JC AS7C259L-15JC	AS7C259-20JC AS7C259L-20JC	AS7C259-25JC AS7C259L-25JC	AS7C259-35JC AS7C259L-35JC
	AS7C259-12TC AS7C259L-12TC	AS7C259-15TC AS7C259L-15TC	AS7C259-20TC AS7C259L-20TC	AS7C259-25TC AS7C259L-25TC	AS7C259-35TC AS7C259L-35TC

PART NUMBERING SYSTEM



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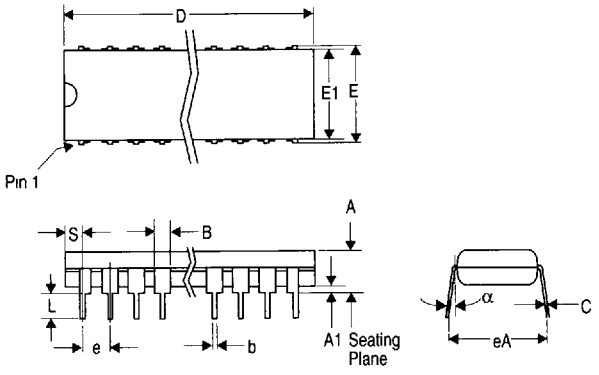
June 1993

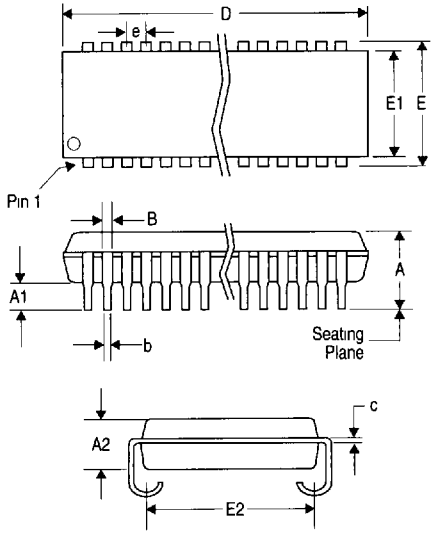
Plastic Dual In-line Package (PDIP)



	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max
A	–	0.175	–	0.175	–	0.180	–	0.200
A1	0.010	–	0.010	–	0.020	–	0.015	–
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022
C	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015
D	–	0.980	–	1.400	1.560	1.570	1.610	1.620
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.330	0.370
L	0.110	0.130	0.120	0.140	0.125	0.135	0.115	0.160
α	0°	15°	0°	15°	0°	15°	0°	15°
S	–	0.040	–	0.055	–	0.038	–	0.040

Dimensions in inches

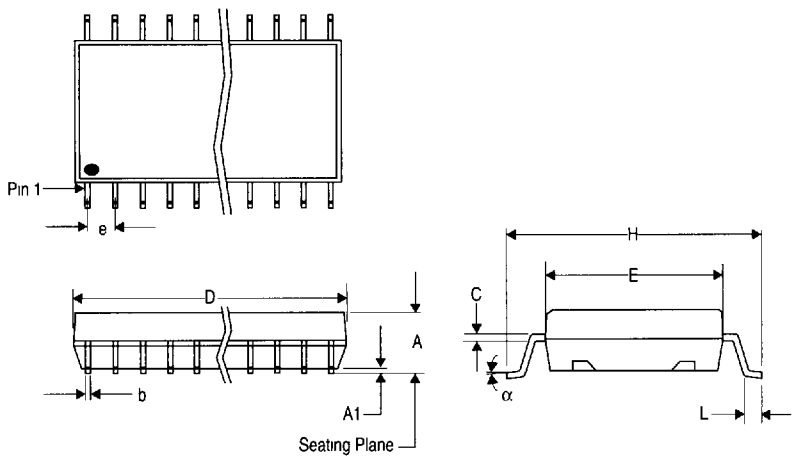
Plastic Small Outline J-Bend (SOJ)



	20/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil		40-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	–	0.140	–	0.140	–	0.145	–	0.145	–	0.145
A1	0.020	–	0.025	–	0.025	–	0.025	–	0.025	–
A2	0.095	0.105	0.095	0.105	0.086	0.094	0.086	0.090	0.086	0.115
B	0.026	0.032	0.028 TYP		0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.018 TYP		0.014	0.020	0.015	0.020	0.015	0.022
c	0.008	0.014	0.010 TYP		0.006	0.013	0.007	0.013	0.007	0.014
D	–	0.686	–	0.730	0.820	0.830	0.820	0.830	1.015	1.035
E	0.327	0.347	0.327	0.347	0.330	0.340	0.435	0.445	0.435	0.445
E1	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405
E2	0.245	0.285	0.245	0.285	0.250	0.275	0.360	0.380	0.378	0.390
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	

Dimensions in inches

Plastic Small Outline Gull-Wing IC (SOIC)



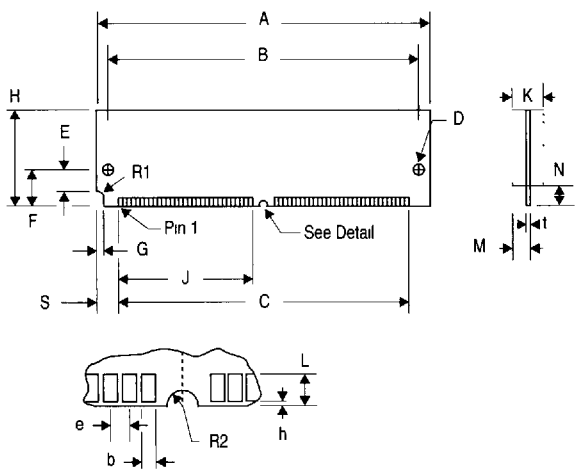
32-pin 525 mil

	Min	Max
A	–	0.118
A1	0.002	
b	0.014	0.020
C	0.008	0.012
D	0.801	0.811
e	0.050 BSC	
E	0.445	0.455
H	0.546	0.570
	0.026	0.036
α	0°	8°

Dimensions in inches

PRELIMINARY

Single In-Line Memory Module (SIMM)



64 dual readout

	Min	Max
A	3.840	3.860
B	3.584 TYP	
b	0.040	0.042
C	3.350 TYP	
D	0.123	0.127
E	0.150 TYP	
e	0.050 BSC	
F	0.400 TYP	
G	0.075	0.085
H	–	1.125
h	–	0.010
J	1.550 TYP	
K	–	0.360

64 dual cont'd

	Min	Max
L	0.100	–
M	–	0.208
N	0.225	–
R1	0.060	0.064
R2	0.060	0.064
S	0.250 TYP	
t	0.045	0.055

Dimensions in inches