SRAM

512K x 8 SRAM

LOW POWER,
EVOLUTIONARY PINOUT

AVAILABLE AS MILITARY SPECIFICATION
- SMD 5962-95613 Pending
- MIL STD-883

FEATURES
- Ultra Low Power with 2V Data Retention
- Fully Static, No Clocks
- Single +5V ±10% power supply
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Ease of upgradability from 1 meg using the 32 pin evolutionary version

OPTIONS MARKING
- **Timing**

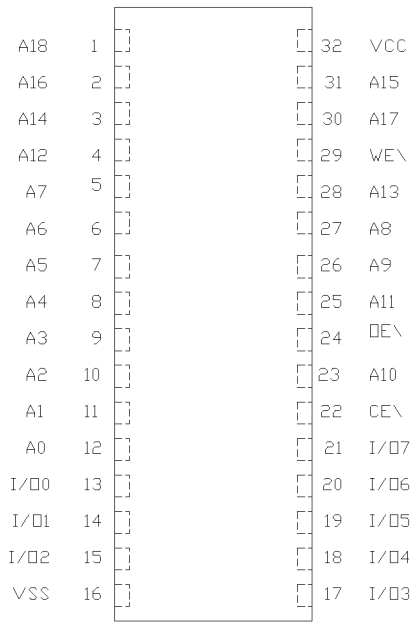
55ns access	-55
70ns access	-70
85ns access	-85
100ns access	-100

- **Packages**

Ceramic Dip (600 mil)	CW	No. 112
Ceramic SOJ	ECJ	No. 502

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)
32-Pin DIP
32-Pin LCC
32-Pin SOJ



GENERAL DESCRIPTION

The AS5C4009LP is organized as 524,288 x 8 SRAM's utilizing a special low power design process. ASI 4Meg SRAMs are fabricated using double-layer metal, double / triple-layer polysilicon technology.

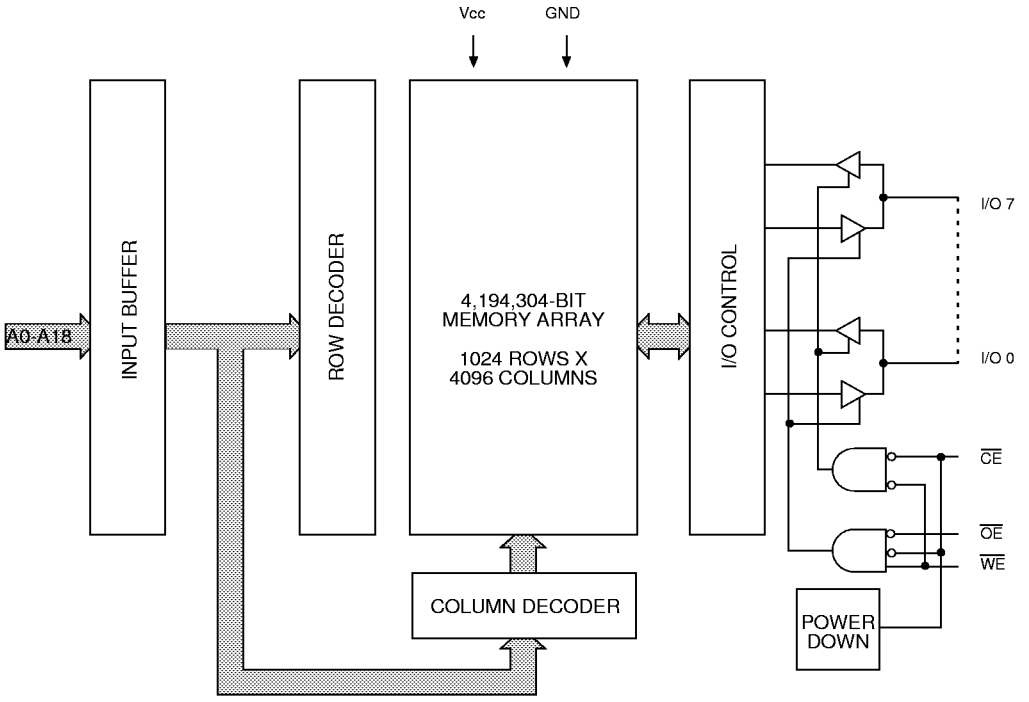
The evolutionary 32 pin version allows for easy upgrades from the 1 meg SRAM design.

For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capabilities.
These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled, by lowering VCC to 2V and maintaining CE\ = 2V. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	I/O	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to +7.0V
Storage Temperature .....-55°C to +150°C
Short Circuit Output Current (per I/O).....20mA
Voltage on any Pin Relative to Vss.....-5V to Vcc+1 V
Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55 ℃ ≤ T A ≤ 125 ℃; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-55	-70	-85	-100	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{CC}	100	80	70	60	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{SBT1}	10	10	10	10	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SBC}	1	1	1	1	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Output Capacitance	T_A = 25 ℃; 1 = MHz	C_I	8	pF	4
Input Capacitance	V_{CC} = 5V	C_O	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5) (-55 ℃ ≤ T_A ≤ 125 ℃; V_{CC} = 5V ±10%)

DESCRIPTION		-55		-70		-85		-100			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	^tRC	55		70		85		100		ns	
Address access time	^tAA		55		70		85		100	ns	
Chip Enable access time	^tACE		55		70		85		100	ns	
Output hold from address change	^tOH	5		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	10		10		10		10		ns	4,6,7
Chip disable to output in High-Z	^tHZCE		20		25		30		30	ns	4,6,7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		55		70		85		100	ns	4
Output Enable access time	^tAOE		30		35		40		45	ns	
Output Enable to output in Low-Z	^tLZOE	5		5		5		5		ns	4,6,7
Output disable to output in High-Z	^tHZOE		20		25		30		30	ns	4,6,7
WRITE Cycle											
WRITE cycle time	^tWC	55		70		85		100		ns	
Chip Enable to end of write	^tCW	50		60		70		80		ns	
Address valid to end of write	^tAW	50		60		70		80		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	45		50		55		60		ns	
WRITE pulse width	$^tWP2$	45		50		55		60		ns	
Data setup time	^tDS	30		30		35		40		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	4,6,7
Write Enable to output in High-Z	^tHZWE		25		25		30		30	ns	4,6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

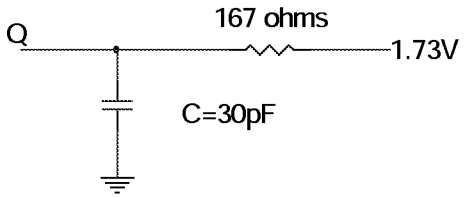


Fig. 1 Output Load Equivalent

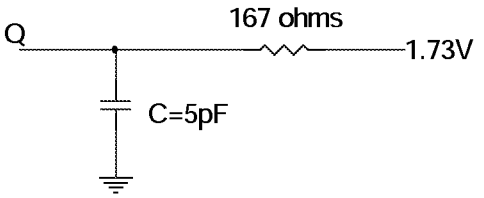


Fig. 2 Output Load Equivalent

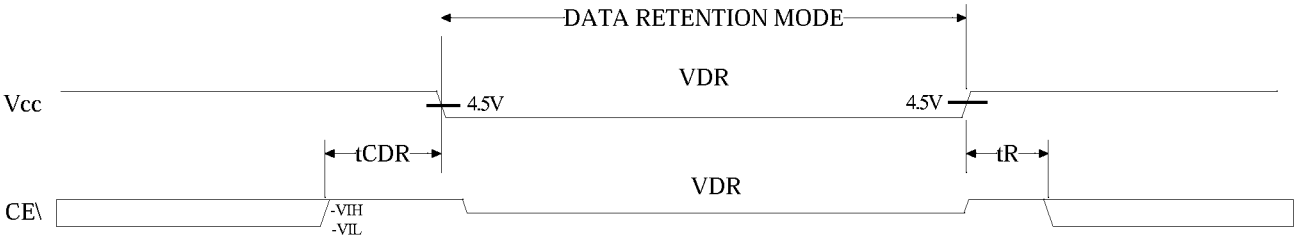
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}LZCE, ^{t}LZWE, ^{t}LZOE, ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

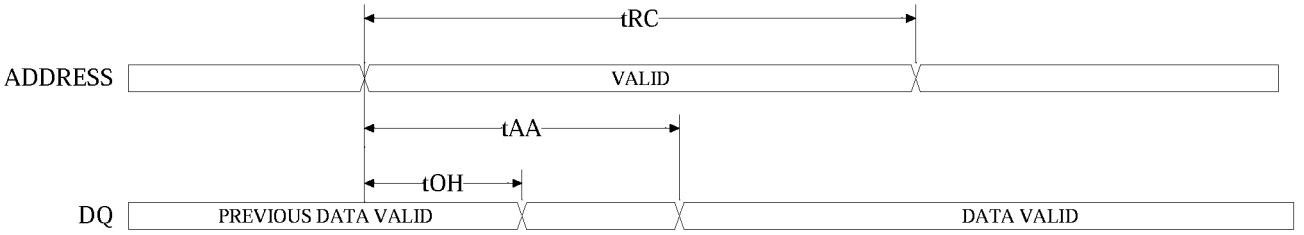
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
VCC for Retention Data			V_{DR}	2		V	
Data Retention Current L version	CE ≥ (Vcc -0.2V)	VCC = 2V	I_{CCDR}		200	µA	
	VIN ≥ (VCC -0.2V)	VCC = 3V	I_{CCDR}		400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

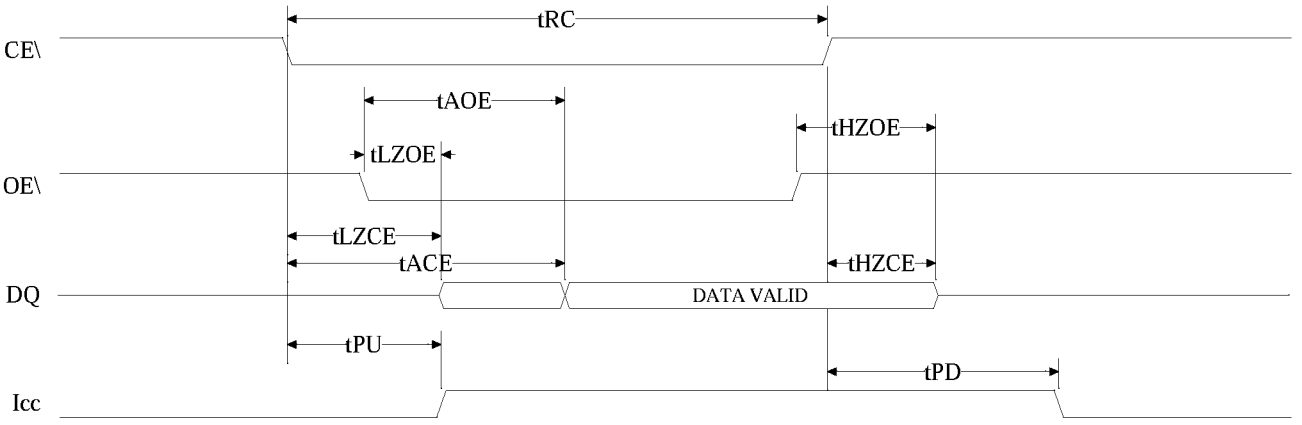
LOW V_{CC} DATA RETENTION WAVEFORM



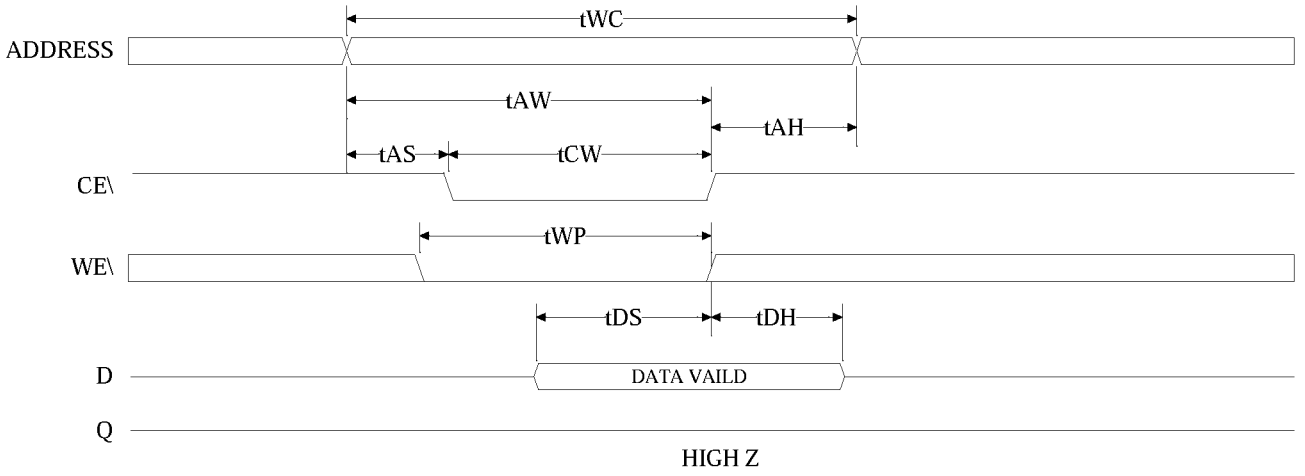
READ CYCLE NO. 1 [8, 9]
(Write Enabled Controlled)



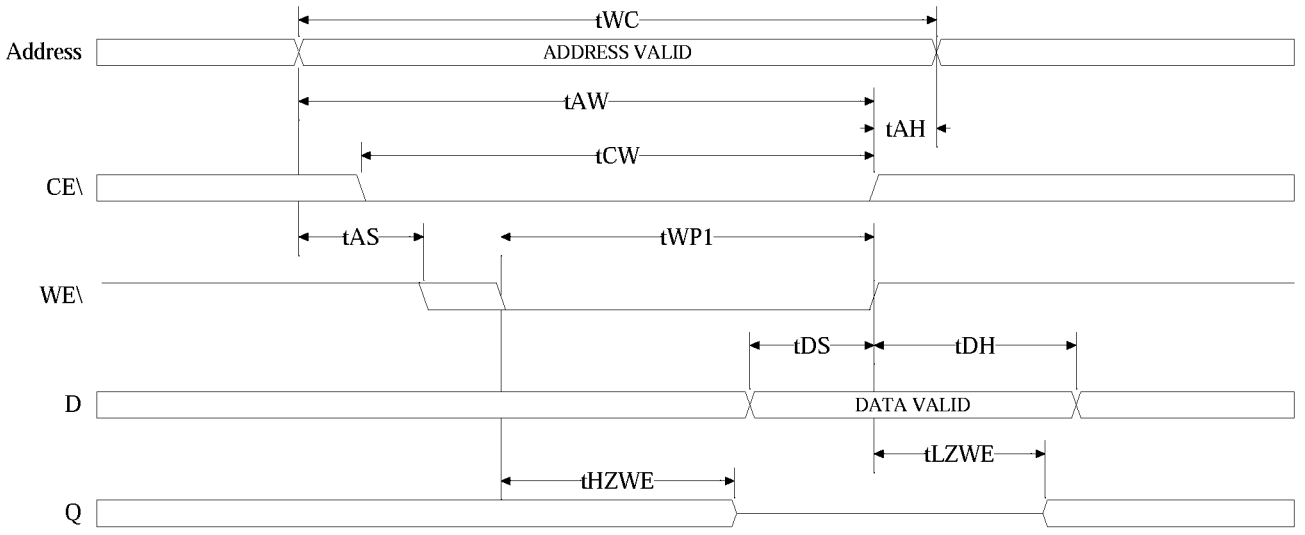
READ CYCLE NO. 2 [7, 8, 10]
(Write Enabled Controlled)



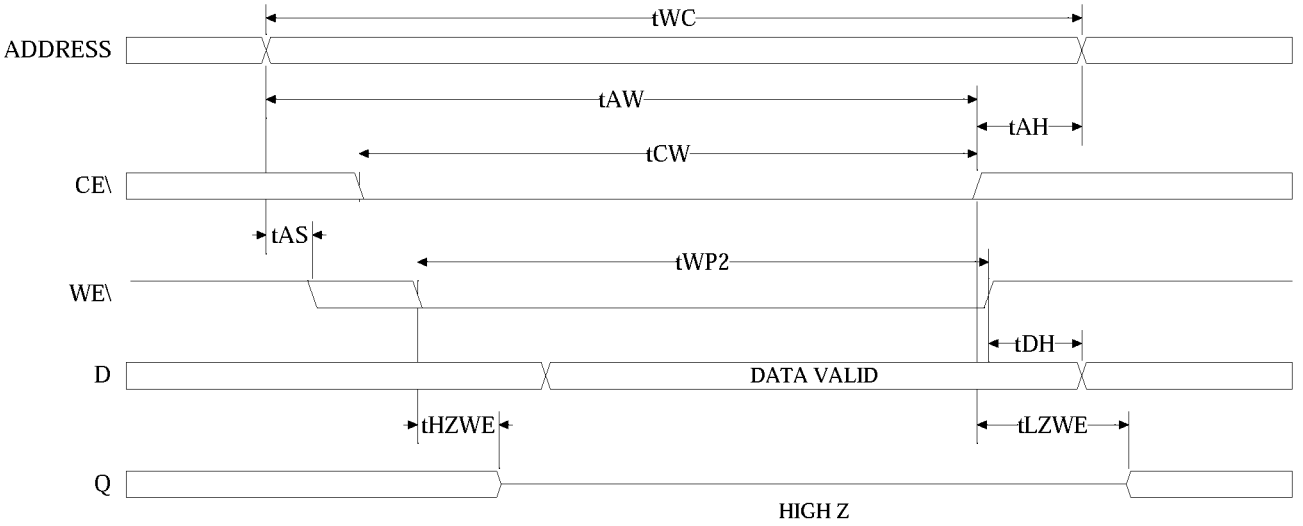
WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



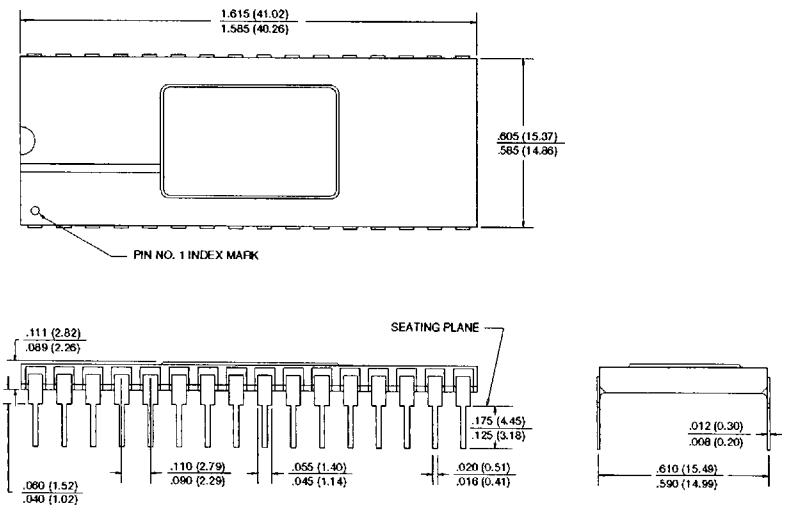
WRITE CYCLE NO. 2 [12, 13]
(Write Enabled Controlled)



WRITE CYCLE NO. 3 [7, 12, 14]
(Write Enabled Controlled)

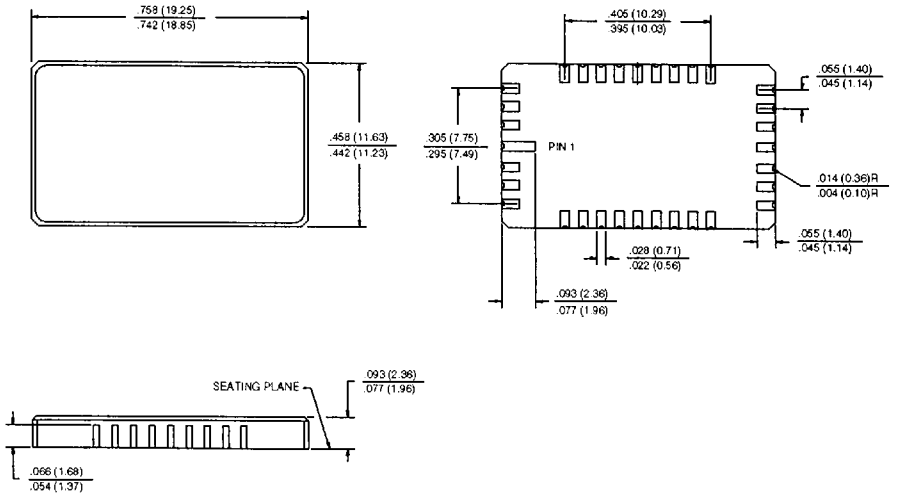


PACKAGE NO. 112
32 CDIP (600 mils)

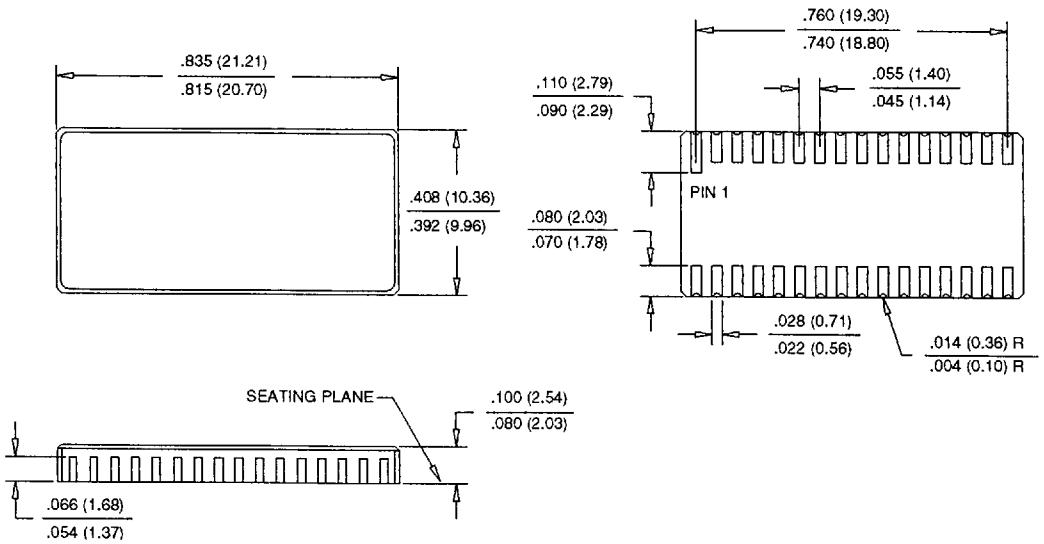


PKG-7

PACKAGE NO. 206
32 CLCC

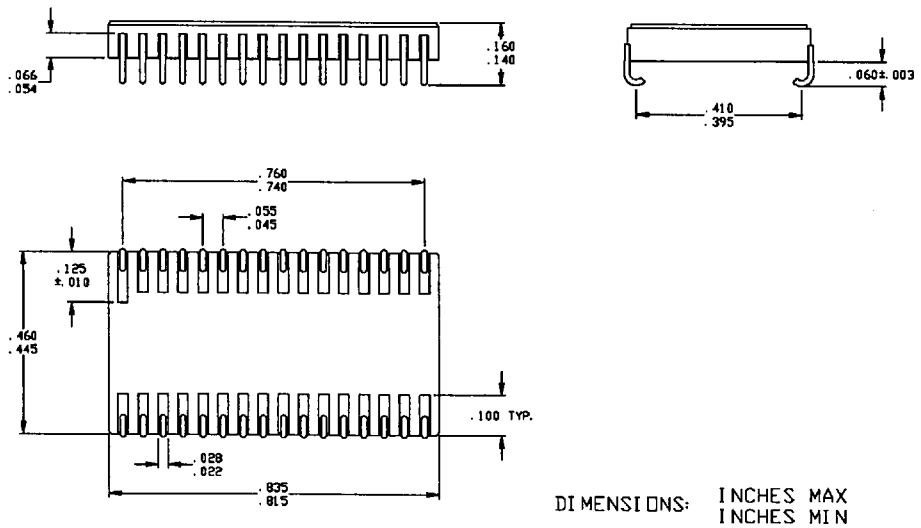


PACKAGE NO. 207
32 CLCC



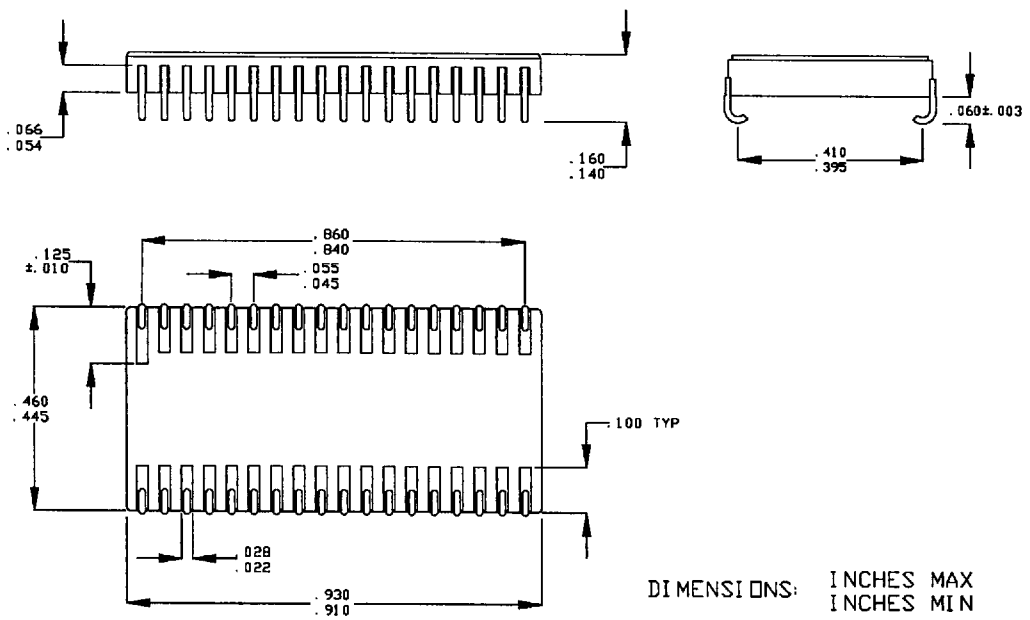
PKG-11

PACKAGE NO. 502
32 CSOJ



DIMENSIONS: INCHES MAX
INCHES MIN

PACKAGE NO. 503
36 CSOJ



DIMENSIONS: INCHES MAX
INCHES MIN

PKG-21