MOTOROLA

DSPRAM™
8K x 24 Bit Fast Static RAM

ELECTRICALLY TESTED PER:
MPG56824A

56824A

Commercial Plus and Mil/Aero Applications

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883: 56824A - XX/BXCJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CLCC: Y

XX = Speed in ns (25, 30, 35)

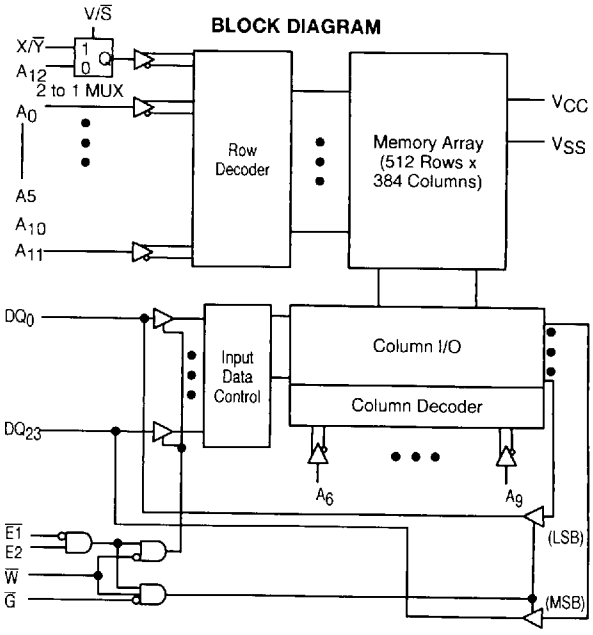
The 56824A is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high performance silicon-gate CMOS technology. This device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to Motorola's Military 56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic. This device can also be used as three 8K x 8 SRAMs by holding V/$\overline{S}$ low.

The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, which is useful in low-power applications. A single on-chip multiplexer selects A_{12} or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re-partitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands stored in lower memory. By connecting 56001 address A15 select to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. Refer to the application diagrams at the end of this data sheet for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise. The 56824A is available in 52 pin ceramic leaded chip-carrier (CLCC).

- Single 5.0 V ± 10% Power Supply
- Fast Access Times: 25/30/35 ns
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- On-Chip Single Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three-State Outputs
- Low-Power Standby Mode
- Fully TTL Compatible

BLOCK DIAGRAM



DSPRAM is a trademark of Motorola, Inc.

PIN ASSIGNMENT AND FUNCTION TABLE

Pin	Symbol	Name
1	DQ0	Data Input/Output
2	DQ1	Data Input/Output
3	DQ2	Data Input/Output
4	V_{SS}	Ground
5	DQ3	Data Input/Output
6	DQ4	Data Input/Output
7	DQ5	Data Input/Output
8	DQ6	Data Input/Output
9	DQ7	Data Input/Output
10	DQ8	Data Input/Output
11	V_{SS}	Ground
12	DQ9	Data Input/Output
13	DQ10	Data Input/Output
14	DQ11	Data Input/Output
15	A9	Address Input
16	A8	Address Input
17	A7	Address Input
18	A6	Address Input
19	$\overline{G}$	Output Enable
20	V_{CC}	+5 V Power Supply
21	V_{SS}	Ground
22	$\overline{E1}$	Chip Enable
23	E2	Chip Enable
24	$\overline{W}$	Write Enable
25	NC	No Connection
26	DQ12	Data Input/Output

Pin	Symbol	Name
27	DQ13	Data Input/Output
28	DQ14	Data Input/Output
29	V_{SS}	Ground
30	DQ15	Data Input/Output
31	DQ16	Data Input/Output
32	DQ17	Data Input/Output
33	DQ18	Data Input/Output
34	DQ19	Data Input/Output
35	DQ20	Data Input/Output
36	V_{SS}	Ground
37	DQ21	Data Input/Output
38	DQ22	Data Input/Output
39	DQ23	Data Input/Output
40	A5	Address Input
41	A4	Address Input
42	A3	Address Input
43	A2	Address Input
44	A1	Address Input
45	A0	Address Input
46	V_{CC}	+5 V Power Supply
47	NC	No Connection
48	$V/\overline{S}$	Address Multiplexed Control
49	$X/\overline{Y}$	Multiplexed Address
50	A12	Address Input
51	A11	Address Input
52	A10	Address Input

Truth Table

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	$V/\overline{S}$	Mode	I/O Status	Supply Current
H	X	X	X	X	Not Selected	High - Z	I_{SB}
X	L	X	X	X	Not Selected	High - Z	I_{SB}
L	H	H	H	X	Output Disable	High - Z	I_{CC}
L	H	L	H	H	Read Using $X/\overline{Y}$	Data Out	I_{CC}
L	H	L	H	L	Read Using A_{12}	Data Out	I_{CC}
L	H	X	L	H	Write Using $X/\overline{Y}$	Data In	I_{CC}
L	H	X	L	L	Write Using A_{12}	Data In	I_{CC}

X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note, Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (TA = 70°C, V_{CC} = 5 V, t_{AVAV} = 50 ns)	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 55 to + 125	°C
Operating Temperature	T_A	– 55 to + 125	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltages higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board and transverse air flow of at least 300 linear feet per minute is maintained. Outputs are terminated through a 100-ohm resistor to – 2.0 volts.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V + 10%, T_A = –55 to + 125°C, Unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.0	0.8	V

*V_{IL} (min) = – 3.0 V_{AC} (pulse width ≤ 20 ns)

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0-DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0-DQ23	$C_{I/O}$	6	8	pF

DC CHARACTERISTICS

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Functional Parameters:	+ 25°C		+ 125° C		– 55°C			
		Min	Max	Min	Max	Min	Max		
I_{IL}, I_{IH}	Input Leakage Current	—	± 1.0	—	± 1.0	—	± 1.0	µA	All inputs, V_{in} = 0 to V_{CC}
I_{OL},I_{OH}	Output Leakage Current	—	± 1.0	—	± 1.0	—	± 1.0	µA	$\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC}
I_{CCA}	AC Supply Current								
	56824A-25/BYCIC Cycle Time ≥ 25 ns	—	280	—	280	—	280	mA	$\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IH}, I_{out} = 0 mA, All other inputs = V_{IL} = 0 V or V_{IH} = 3 V
	56824A-30/BYCIC Cycle Time ≥ 30 ns	—	250	—	250	—	250		
	56824A-35/BYCIC Cycle Time ≥ 35 ns	—	180	—	180	—	180		
I_{SB1}	Standby Current	—	15	—	15	—	15	mA	$\overline{E1}$ = V_{IH}, E2 = V_{IL}, All inputs = V_{IL} or V_{IH}
I_{SB2}	CMOS Standby Current	—	10	—	10	—	10	mA	$\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V
V_{OL}	Output Low Voltage	—	0.4	—	0.4	—	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	—	2.4	—	2.4	—	V	I_{OH} = – 4.0 mA

AC TEST LOADS

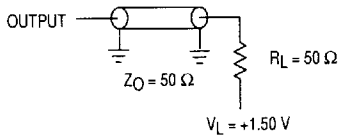


Figure 1A.

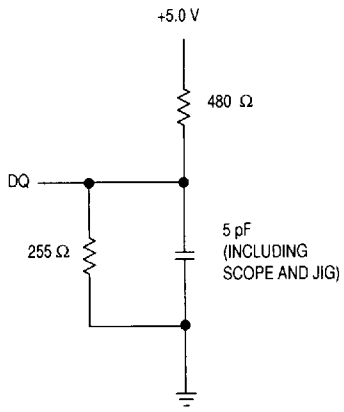


Figure 1B.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to + 125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3.0 ns

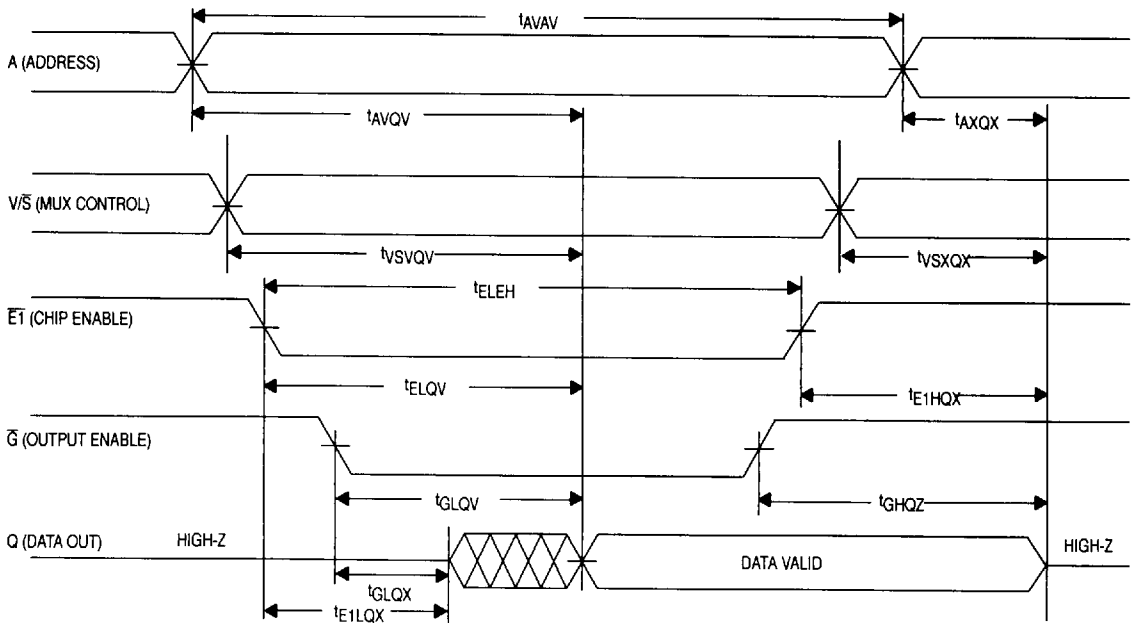
Output Timing Measurement Reference Level .... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ CYCLE (See Note 1, 2, 3)

Parameters	Symbol	Alternate Symbol	56824A-25		56824A-30		56824A-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	—
MUX Control Valid to Output Valid	t_{VSVQV}	t_{AA}	—	25	—	30	—	35	ns	—
Chip Enable to Valid Output	t_{E1LQV} t_{E2HQV}	t_{AC1} t_{AC2}	—	25	—	30	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	12	—	15	—	15	ns	—
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	t_{CLZ}	2	—	2	—	2	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	t_{OLZ}	2	—	2	—	2	—	ns	5
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	t_{VSOH}	5	—	5	—	5	—	ns	
Chip Enable to Output High-Z	t_{E1HQZ} t_{E2LQZ}	t_{CHZ}	0	12	0	15	0	15	ns	4, 5
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	12	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. E1 in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B. At any given voltage and temperature, $t_{E1HQZmax}$ is less than $t_{E1LQXmin}$, $t_{E2LQXmax}$ is less than $t_{E2HQXmin}$, and $t_{GHQZmax}$ is less than $t_{GLQXmin}$ for a given device and from device to device.

READ CYCLE

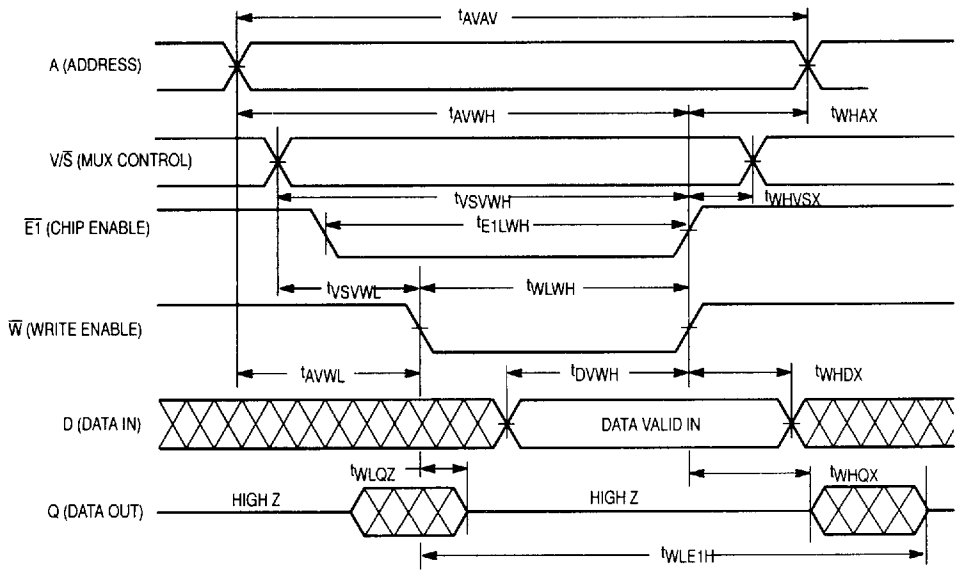


WRITE CYCLE TIMING, WRITE ENABLE INITIATED (See Note 1)

Parameter	Symbol		56824A-25		56824A-30		56824A-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{ASVWL}	t_{VSS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	ns	
MUX Control Valid to End of Write	t_{ASVWL}	t_{VSW}	20	—	25	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	18	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	t_{CW}	15	—	18	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	t_{CW}	15	—	18	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	t_{VSR}	0	—	0	—	0	—	ns	
Write High to Output Low-Z	t_{WHQX}	t_{OW}	2	—	2	—	2	—	ns	6
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	0	12	0	15	0	15	ns	6

NOTES: 1. A write cycle starts at the transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, or $\overline{W}$ high, or E2 low.
2. Write must be high for all address and transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of the opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min, for a given device and from device to device.

$\overline{W}$ INITIATED WRITE CYCLE

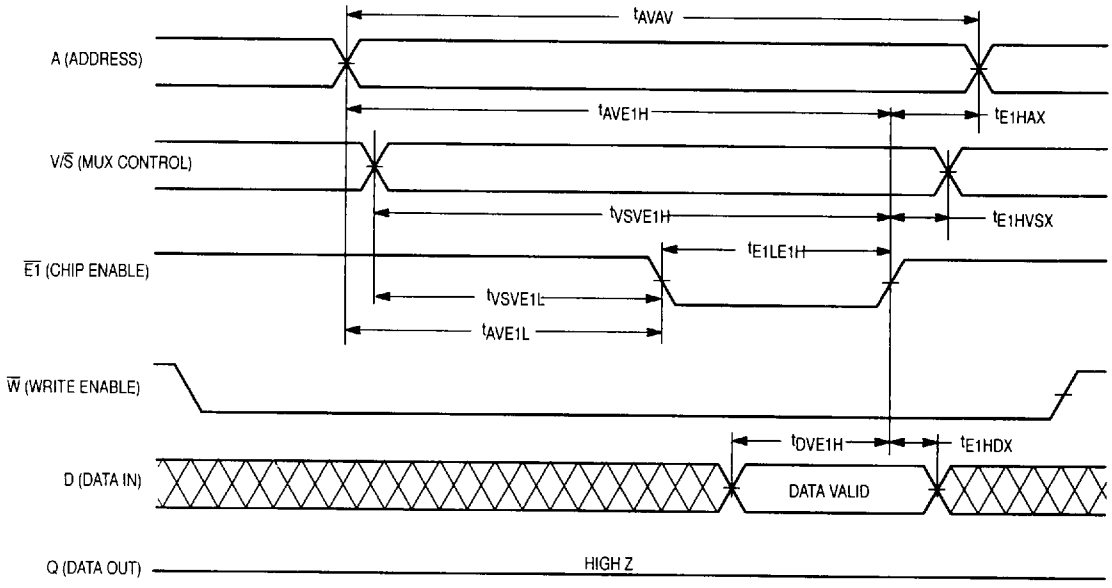


WRITE CYCLE TIMING, CHIP ENABLE INITIATED (See Note 1)

Parameter	Symbol		56824A-25		56824A-30		56824A-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	2
Address Setup Time	t_{AVE1L} t_{AVE2H}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	t_{VSS}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	t_{SW}	20	—	25	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	t_{VSW}	20	—	25	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	t_{CW}	15	—	18	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	t_{DW}	10	—	12	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	t_{DH}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	t_{VSR}	0	—	0	—	0	—	ns	2

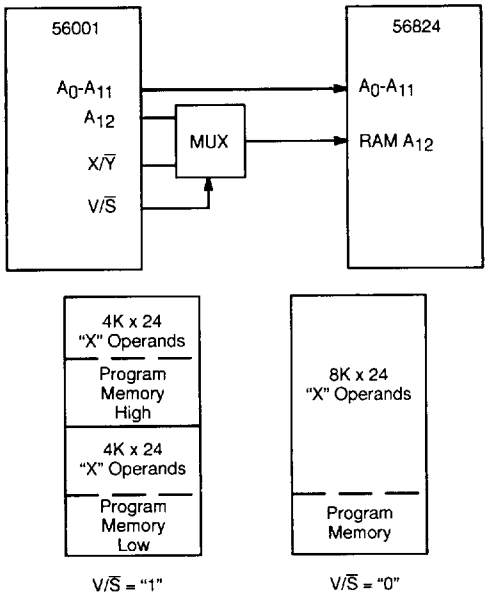
NOTES: 1. A write cycle starts at the transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, or $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. During this time the output pins may be in the output state. Signals of the opposite phase must not be applied to the outputs at this time.

$\overline{E1}$ OR E2 INITIATED WRITE CYCLE



BLOCK DIAGRAM

56824A DSPRAM Multiplexed Vector/Scalar Address Maps



56824A 8K x 24 DSPRAM Used in Typical Application