

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# 2SK1636(L), 2SK1636(S)

Silicon N-Channel MOS FET

**RENESAS**

ADE-208-1304 (Z)  
1st. Edition  
Mar. 2001

## Application

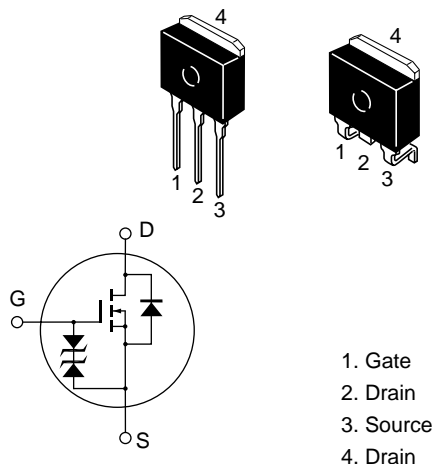
High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

## Outline

LDBPAK



## 2SK1636(L), 2SK1636(S)

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	250	V
Gate to source voltage	V <sub>GSS</sub>	±30	V
Drain current	I <sub>D</sub>	15	A
Drain peak current	I <sub>D(pulse)</sub> <sup>*1</sup>	60	A
Body to drain diode reverse drain current	I <sub>DR</sub>	15	A
Channel dissipation	Pch <sup>*2</sup>	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes 1. PW 10 μs, duty cycle 1%

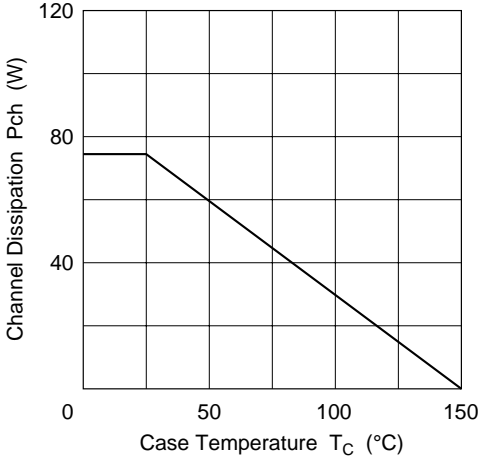
2. Value at T<sub>c</sub> = 25°C

## Electrical Characteristics (Ta = 25°C)

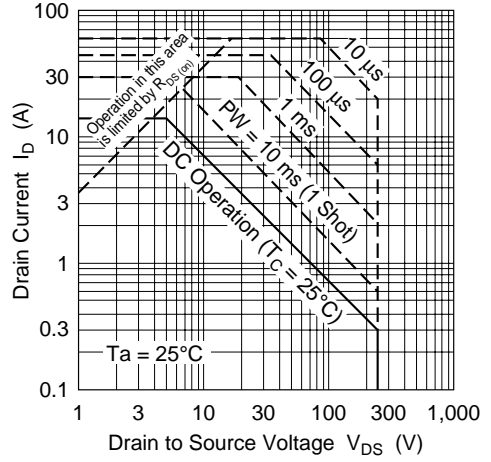
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 30$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	250	$\mu\text{A}$	$V_{DS} = 200 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static Drain to source on state resistance	$R_{DS(on)}$	—	0.22	0.27		$I_D = 8 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	6.0	10.0	—	S	$I_D = 8 \text{ A}, V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	1250	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$
Output capacitance	$C_{oss}$	—	510	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	—	85	—	pF	
Turn-on delay time	$t_{d(on)}$	—	24	—	ns	$I_D = 8 \text{ A}, V_{GS} = 10 \text{ V},$
Rise time	$t_r$	—	85	—	ns	$R_L = 3.75$
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	$t_f$	—	60	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	1.0	—	V	$I_F = 15 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	400	—	ns	$I_F = 15 \text{ A}, V_{GS} = 0,$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note 1. Pulse test

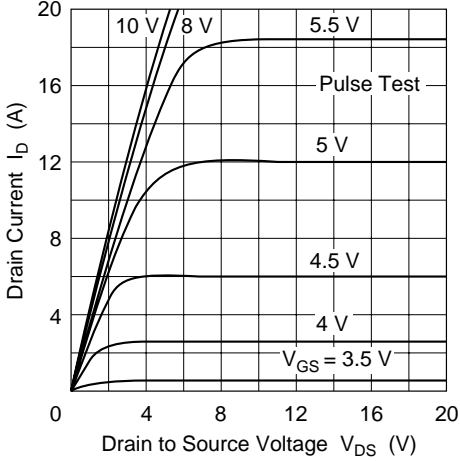
Power vs. Temperature Derating



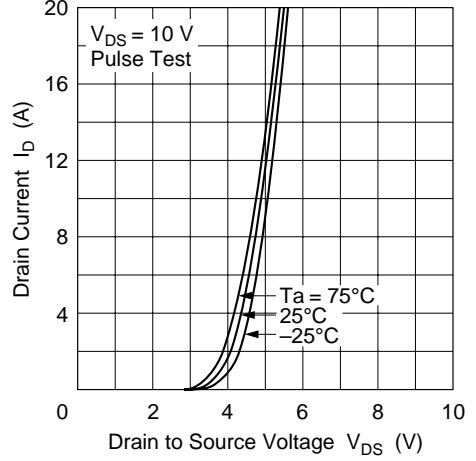
Maximum Safe Operation Area

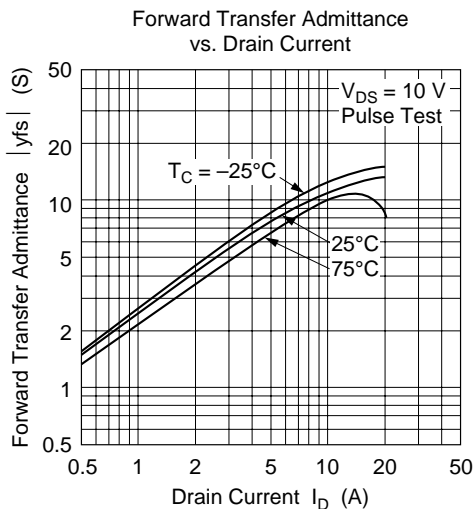
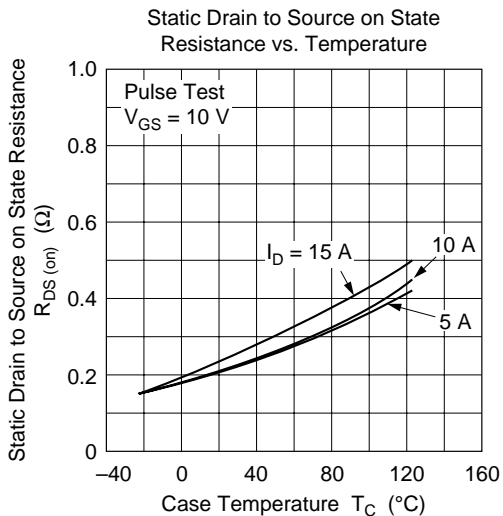
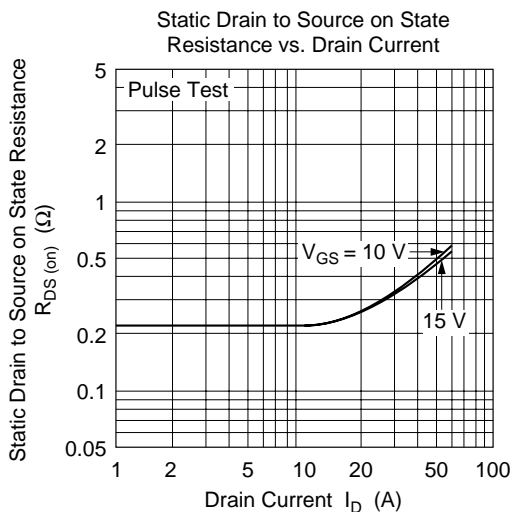
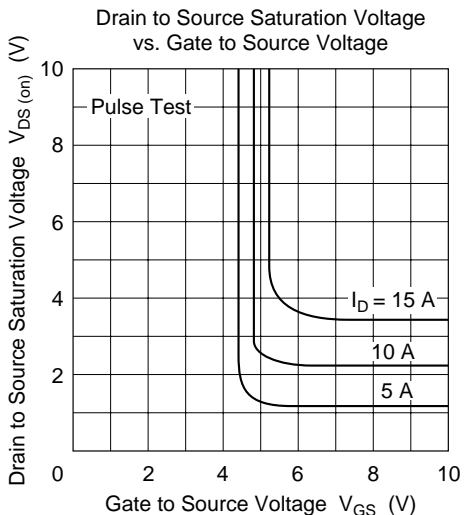


Typical Transfer Characteristics

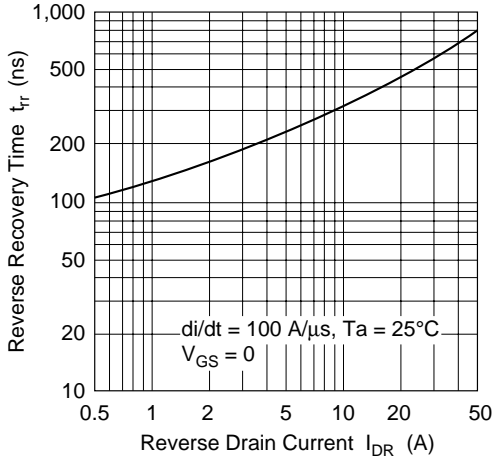


Typical Transfer Characteristics

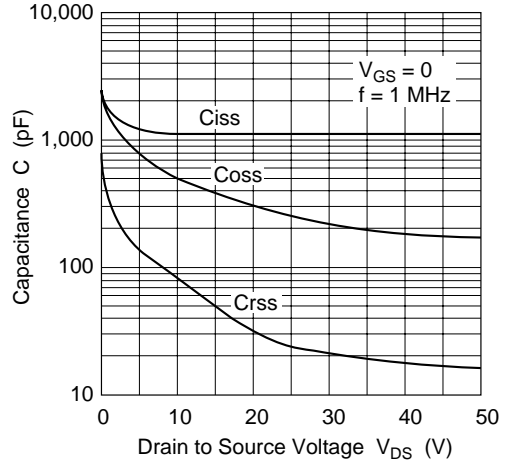




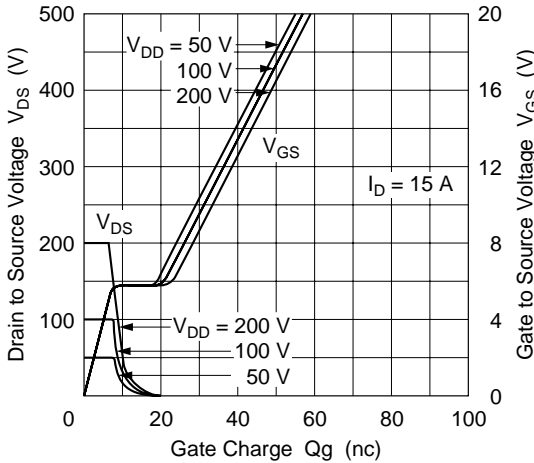
Body to Drain Diode Reverse Recovery Time



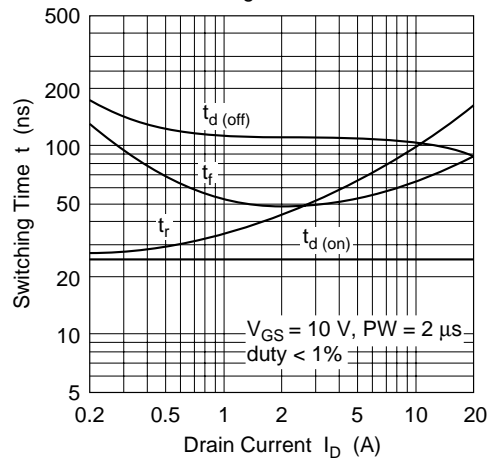
Typical Capacitance vs. Drain to Source Voltage



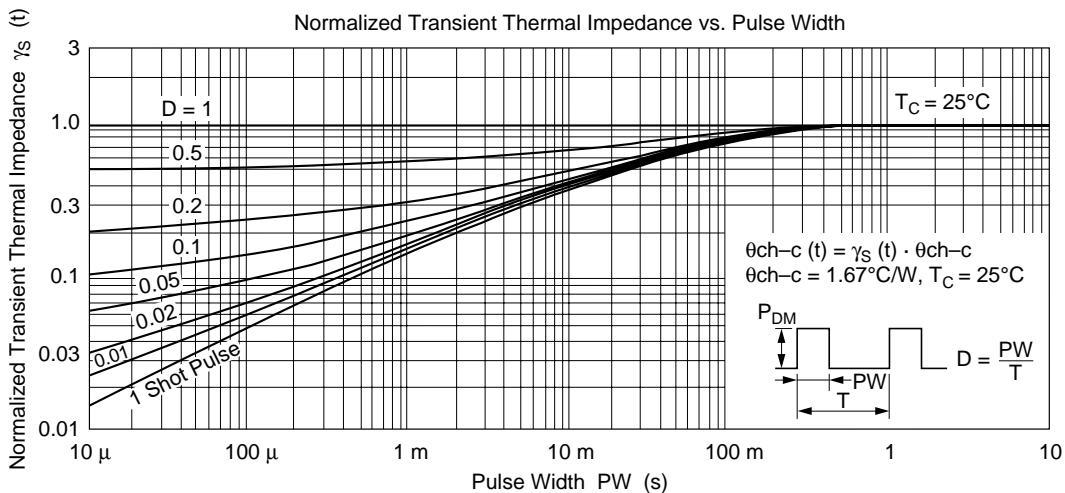
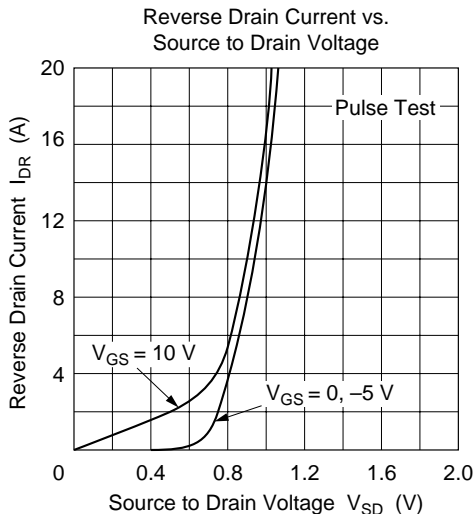
Dynamic Input Characteristics



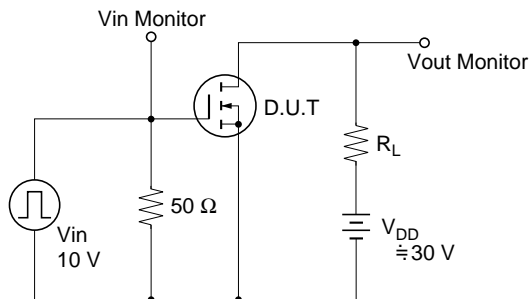
Switching Characteristics



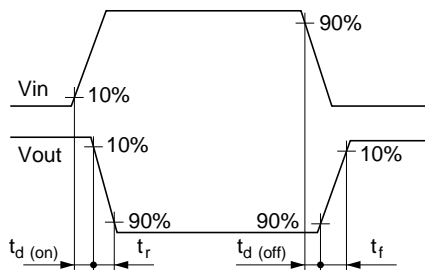




Switching Time Test Circuit

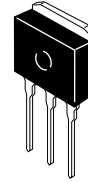
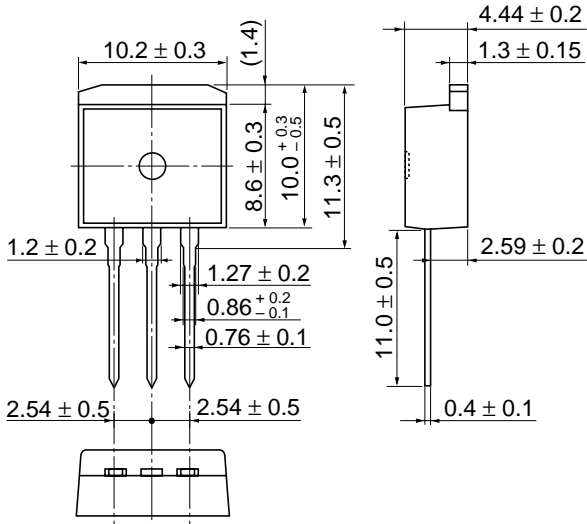


Waveforms



Package Dimensions

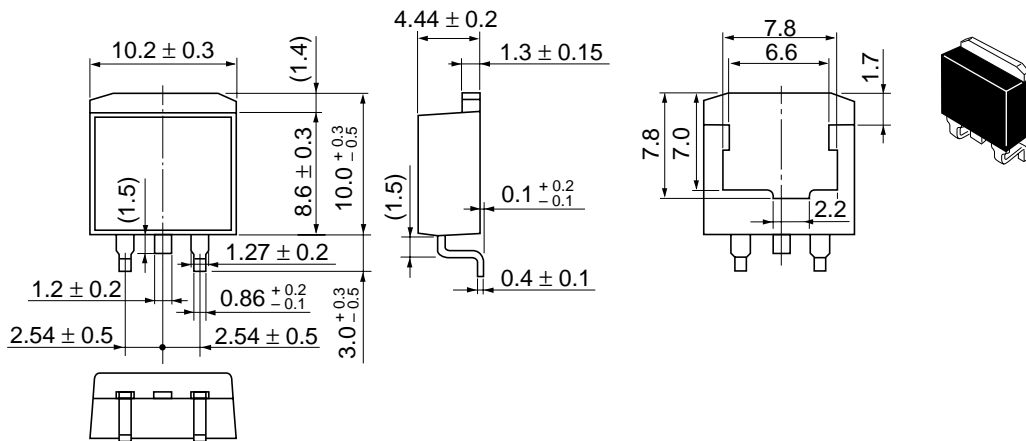
As of January, 2001  
Unit: mm



Hitachi Code	LDBAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

As of January, 2001

Unit: mm

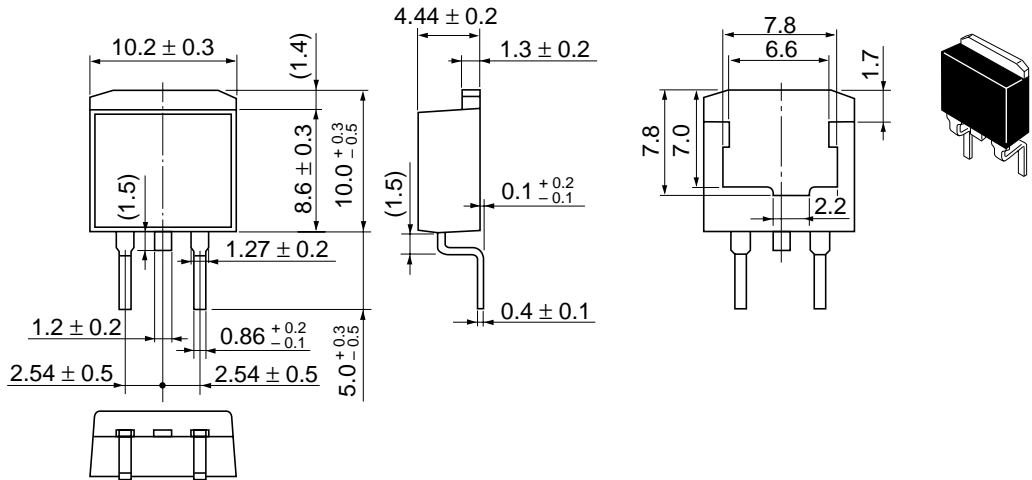


Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

# 2SK1636(L), 2SK1636(S)

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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