Voice/Melody/LCD Controller (*ViewTalk* ™ Series)

GENERAL DESCRIPTION

The W536A031, a member of *ViewTalk*™ family, is a high-performance 4-bit micro-controller (uC) with built-in speech unit, melody unit and 64seg * 16 com LCD driver unit which includes internal regulator, pump circuit and dedicated two pages LCD RAM. The 4-bit uC core contains dual clock source, 4-bit ALU, two 8-bit timers, one 14 bits divider, 16 pads for input or output, 8 interrupt sources and 8-level nesting for subroutine/interrupt applications. Speech unit, integrated as a single chip with maximum 32 seconds (based on 6.4K sample rate with 5 bits MDPCM), is capable of expanding to 512 seconds speech addressed by external memory W55XXX with serial bus interface. It can be implemented with Winbond Power Speech using MDPCM algorithm. Melody unit provides dual tone output and can store up to 1k notes. Power reduction mode is also built in to minimize power dissipation. It is ideal for games, educational toys, remote controllers, watches, clocks and other application products that incorporate both LCD display and speech.

Body	**W536A031**
Voice	30 sec
I/O pad	8I/O, 8I (RA/RB/RC/RD)
WDT disable/Enable (Mask Option)	Y
Sub-clock RC/XTAL mode (Mask Option)	Y
RD port shared as serial bus (Mask Option)	Y (1)
Tri-state serial bus (Mask Option) (3)	Y
Cascaded Voice ROM through serial bus (2)	Y (1)

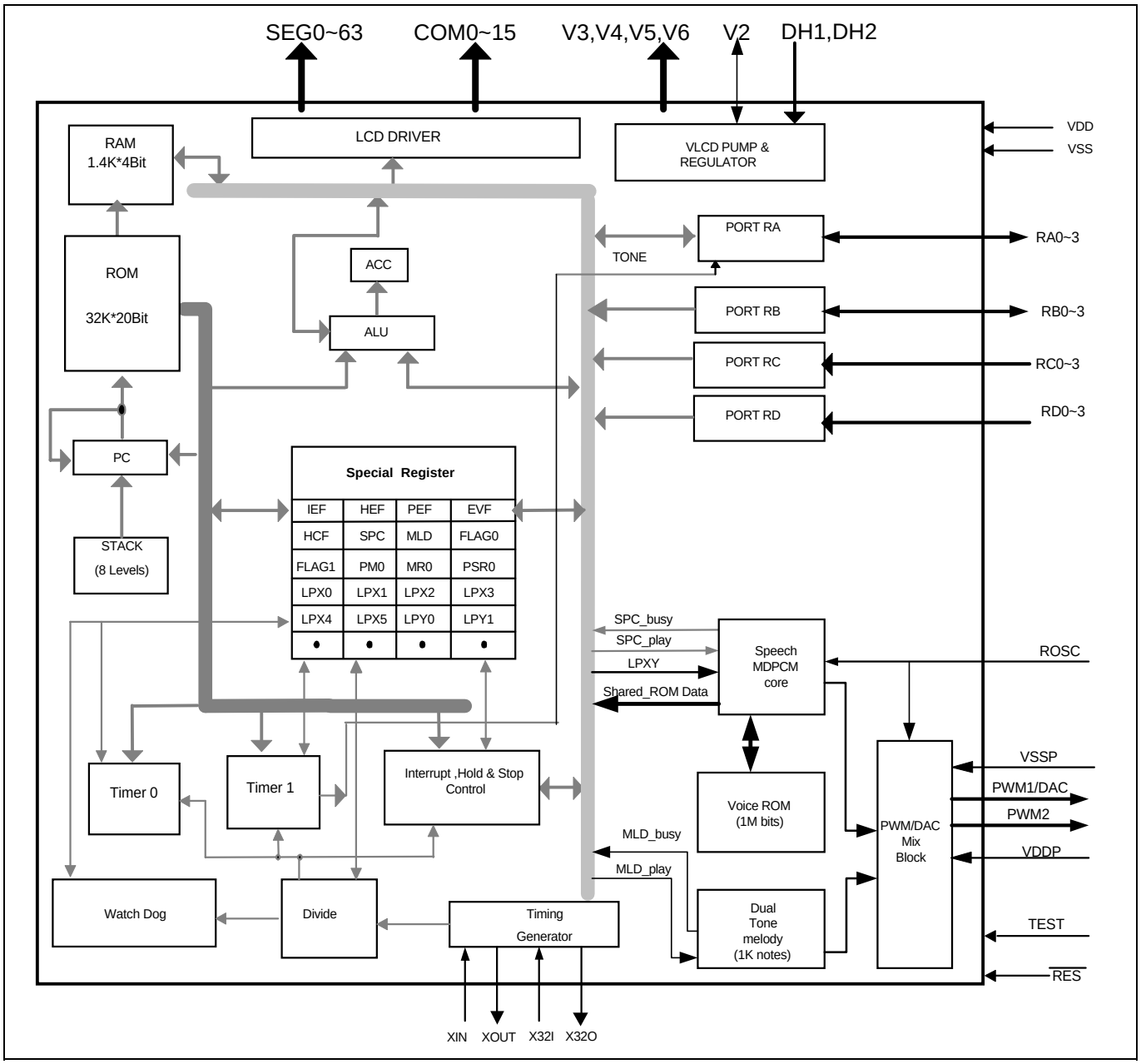
(1) Share 3 pads of RD port (RD1/ADDR, RD2/DATA and RD3/CLK)
(2) Dedicate serial bus 3 pads (ADDR, DATA and CLK) to interface with W55XXX. Cascaded Voice ROM can help to expand voice up to 512 sec by W55XXX chip.
(3) Tri-state serial bus mask option can float serial bus while voice playing is no active. Let this mask option is disabled to get minimum power consumption in general.

FEATURES

- Operating voltage: 2.4 volt ~ 5.5 volt
- Watch dog disabled/enabled by mask option
- Dual clock operating system
  - Main clock with Ring/Crystal (400 KHz to 4 MHz)
  - Sub-clock with 32.768 KHz RC/Crystal by mask option

- Memory
  - Program ROM (P-ROM): 32K × 20 (ROM Bank0, 1, 2)
  - Data RAM (W-RAM): 1.4K × 4 bit
    (RAM Bank 0 is 896 nibbles from 0:000 ~0:37F and 0:380~0:3FF are mapped to special register.
    RAM Bank F is 512 nibbles from F: 200 ~F: 3FF either data RAM or dedicated to script kernel)
  - LCD RAM (L-RAM): 256× 4 bit × 2 pages (RAM Bank1, 2 from 200~2FF)
- 16 input/output pads
  - Ports for input only: 8 pads (RC, RD port; RD1~3 can share as serial bus for external memory W55XXX interface @W536A031)
  - Ports for Input/output: 8 pads (RA and RB port; RB port is available)
- Power-down mode
  - Hold mode (except for 32kHz oscillator)
  - Stop mode (including 32kHz oscillator and release by RD or RC port)
- Eight types of interrupts
  - Five internal interrupts (Divider, Timer 0, Timer 1, Speech, Melody)
  - Three external interrupts (Port RC, RD, RA)
- One built-in 14-bit clock frequency divider circuit
- Two built-in 8-bit programmable countdown timers
  - Timer 0: one of two clock sources (FOSC/4 or FOSC/1024) can be selected
  - Timer 1: built-in auto-reload function includes internal timer, external event counter from RC.0
- Built-in 18/14-bit watchdog timer for system reset.
- Powerful instruction sets
- 8-level subroutine (including interrupt) nesting
- LCD driver unit capability
  - VLCD higher than (VDD-0.5V)
  - Built-in voltage regulator to V2 pad
  - 64 seg × 16 com
  - 1/16 or 1/8 duty, 1/5 or 1/4 bias, internal pump circuit option by special register
  - COM 8~ 15 and SEG40~63 can be shared as general input/output by special register
  - Either uC ROM or voice ROM used as LCD picture
- Speech function
  - Provided 1M bits Voice ROM for W536A031 based on 5 bits MDPCM algorithm
  - Voice ROM (V-ROM) available for uC data or LCD picture data.
  - Maximum 8*256 Label/Interrupt vector (voice section number) available
  - Provide two types of speech busy flag to either each GO or each trigger
  - Maximum up to 16M bits speech address capability interface with external memory W55XXX through serial bus.
- Melody function
  - Provide 1K notes (22bits/note) dedicated melody ROM
  - Provide two types of melody busy flag to uC either each note or each song
  - Provide 6 kinds of beat, 16 kinds of tempo, and pitch range from G3# to C7
  - Tremolo, triple frequency and 3 kinds of percussion available
  - Maximum 31 songs available
- Can mix speech with melody
- Multi-engine controller
- Direct driving speaker/buzzer or DAC output
- Chip On Board available

BLOCK DIAGRAM



PAD DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN/RXIN	I	Input pad for main clock oscillator. It can be connected to crystal when crystal mode is selected (SCR0.2=1), otherwise connect a resistor to VDD to generate main system clock while Ring mode is selected (SCR0.2=0 and default). Oscillator can be enabled or stopped by set SCR0.1 to 1 or clear to 0 separately. External capacitor connects to start oscillation while crystal mode and get more accurate clock when crystal mode
XOUT	O	Output pad for oscillator, which is connected to another crystal pad when in crystal mode. External capacitor connects to start oscillation when in crystal mode.
X32I/RSUB1	I	32.768 KHz crystal input pad or external resistor node 1 **by mask option**. External 15~20pF capacitor connects to start oscillation and get more accurate clock when in crystal mode.
X32O/RSUB2	O	32.768 KHz crystal output pad or external resistor node 2 **by mask option.** External 15~20pF capacitor connects to start oscillation and get more accurate clock when in crystal mode.
RA0 ~ RA3/TONE (7)	I/O	General Input/Output port specified by PM1 register. If output mode is selected, PM0 register bit 0 can be used to specify CMOS/NMOS driving capability option (7). Initial state is input mode. RA3 may be uses as TONE if bit 0 of MR0 special register is set to logic 1. An interrupt source.
RB0 ~ RB3 (7)	I/O	General Input/Output port specified by PM2 register. If output mode is selected, PM0 register bit 1 can be used to specify CMOS/NMOS driving capability option (7). Initial state is input mode
RC0 ~ RC3	I	4-bit schmitter input with internal pull high option specified by PM3 register bit 2. Each pad has an independent interrupt capability specified by PEFL special register. Interrupt and STOP mode wake up source. RC0 is also the external event counter source of Timer1.
RD0 RD1/ADDR RD2/DATA RD3/CLK (4)	I	4-bit schmitter input port with internal pull high option specified by PM3 register bit 3. Each pad has an independent interrupt capability specified by PEFH special register. Interrupt and STOP mode wake up source. RD1~3 will be shared as the external memory W55XXX interface pads while RD port shared as serial bus mask option is enabled. "Tri-state serial bus" mask option can use to float CLK/ADDR/SPDATD while "RD port shared as serial bus" mask option is enabled.
$\overline{\text{RES}}$	I	System reset pad, active low with internal pull-high resistor.
TEST	I	Test pad. Active high with internal pull low resistor.
ROSC	I	Connect resistor to VDD pad to generate speech or melody playing clock source.
PWM1/DAC	O	While speech or melody is active, PWM1/DAC is speaker direct driving output or DAC output controlled by voice output file.

PWM2	O	While speech or melody is active, PWM2 is another speaker direct driving output.
SEG0–SEG39	O	Dedicated LCD segment output pads.
SEG40/PORTN.0 | SEG43/PORTN.3	O/O	LCD segment output pads, and can be shared as general output by register LCDM3 bit 1. Default function is segment pad.
SEG44/PORTM.0 | SEG47/PORTM.3	O/I	LCD segment output pads, and can be shared as general input by register LCDM3 bit 0. Default function is segment pad and PM5.1=0 to inhibit LCD waveform abnormal.
SEG48/PORTL.0 | SEG51/PORTL.3	O/O	LCD segment output pads, and can be shared as general output by register LCDM2 bit 3. Default function is segment pad.
SEG52/PORTK.0 | SEG55/PORTK.3	O/I	LCD segment output pads, and can be shared as general input by register LCDM2 bit 2. Default function is segment pad and PM5.0=0 to inhibit LCD waveform abnormal.
SEG56/PORTJ.0 | SEG59/PORTJ.3	O/IO	LCD segment output pads, and can be shared as general input/output by register LCDM2 bit 1. PM4 register is used to select input or output while shared I/O function is active. Default function is segment pad and PM4.3=0 to inhibit LCD waveform abnormal.
SEG60/PORTI.0 | SEG63/PORTI.3	O/IO	LCD segment output pads, and can be shared as general input/output by register LCDM2 bit 0. PM4 register is used to select input or output while shared I/O function is active. Default function is segment pad and PM4.2=0 to inhibit LCD waveform abnormal.
COM0–COM7	O	LCD common signal output pads either 1/16 duty or 1/8 duty. The LCD frame rate is controlled by LCDM1 register, and default value LCDM1=0111b with 64Hz frame rate.
COM8 / PORTP.0 | COM11/PORTP.3	O/O	LCD common signal output pads, or shared as general output by register LCDM3.2 when in 1/8 duty mode. Default function is common function.
COM12/PORTO.0 | COM15/PORTO.3	O/I	LCD common signal output pads, or shared as general input by register LCDM3.2 when in 1/8 duty mode. Default function is common function and PM5.2=0 to inhibit LCD waveform abnormal.
DH1, DH2 (5)	O	Connection terminal for voltage double capacitor with 0.1uF. The DH2 connects to capacitor positive node and DH1 negative node if polar capacitor is used.
V3 ~ V6 (5)	O	LCD COM/SEG output driving voltage. Need an external 0.1uF capacitor to every pad terminal.

V2 (5)	I/O	Voltage regulator output pad. An external capacitor is a must. Output level can be controlled from 0~Fh by LCDM4 register. If internal pump is enabled (LCDM3.3=0 and default value), LCD operating voltage (VLCD) will be 4*V2 or 5*V2 depending on 1/4 bias or 1/5 bias. A limitation should be noted that VLCD must be higher than (VDD-0.5v) to avoid chip leakage current. While external reference voltage is selected (LCDM3.3=1), V2 pad input voltage cannot be over 1.5 Volt to inhibit chip damage.
VSSP (6)	I	Power ground for PWM or DAC playing output.
VSS (6)	I	Power ground
VDDP (6)	I	Power source for PWM or DAC playing output.
VDD (6)	I	Power source.

(4) RD1~3 are shared as ADDR/DATA/CLK to interface with W55XXX

(5) 0.1uF is default value, and capacitor value should be larger than 0.1uF if LCD dot size over 0.5mm * 0.5mm.

(6) External application circuit should connect together, please refer to APPLICATION CIRCUIT. To sure chip operation properly, please bond all VDD, VDDP, VSS and VSSP pads and connect VSS and VSSP from chip outside PCB circuit.

(7) When working at NMOS open drain mode, external pull high voltage can't higher than VDD to avoid leakage current.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(VDD−VSS = 3.0V, No load, F_M = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD panel on with dot size 0.5mm*0.5mm; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT
Op. Voltage	V_{DD}		2.4		5.5	V
Op. Current (No Load, no Voice, no Melody)	I_{OP1}	Dual clock with crystal	-	600	700	uA
		Dual clock with Ring type		600	700	
		Sub-clock only, LCD off		40	50	
		Sub-clock only, LCD on		70	90	
Hold Mode Current (No Load, LCD OFF)	I_{OP2}	Sub-clock active only		6	10	uA
Hold Mode Current (No load, LCD ON)	I_{OP3}	Sub-clock active only			70	uA
Stop Mode Current	I_{OP4}	LCD auto off			1	uA
ADDR/CLK Output High Current	I_{OH1}	Vout=2.7V			-0.8	mA
ADDR/CLK Output low Current	I_{OL1}	Vout=0.4V			0.8	mA
Input Low Voltage	V_{IL}	-	VSS	-	0.3	VDD
Input High Voltage	V_{IH}	-	0.7	-	1	VDD
Port RA, RB Output Low Voltage	V_{ABL}	IOL = 2.0 mA	-	-	0.4	V
Port RA, RB Output High Voltage	V_{ABH}	IOH = -2.0 mA	2.4	-	-	V
Ports(I,J,L,N,P) Output Sink Current	I_{OL3}	V_{OL}= 0.4V	-300			uA
Pull-up Resistor	R_{CD}	Port RC, RD	200	300	400	KΩ
RES Pull-up Resistor	R_{RES}	-	50	100	200	KΩ
PWM1/2 Source Current (8) (R_{LOAD} =8Ω between PWM1 And PWM2)	I_{SPH}	Volume Option =00		-20		mA
		Volume Option =01		-70		
		Volume Option =10		-110		
		Volume Option =11		-135		
PWM1/2 Sink Current (8) (R_{LOAD} =8Ω between PWM1 And PWM2)	I_{SPL}	Volume Option =00		20		mA
		Volume Option =01		70		
		Volume Option =10		110		
		Volume Option =11		135		
DAC output Current	I_{DAC}	VDD=3v, RL=100ohm	-4	-5	-6	mA
LCD Supply Current	I_{LCD}	No Load, All Seg. ON	-	50	-	μA
COM/SEG On Resistor	R_{ON}	IOH = ± 50 μA		5K	10K	Ω
V2 Pad Output Voltage	V_{RR}	Depended on LCDM4	0.7		1.45	V
V2 Pad Output Deviation (9)	V_{D1}	No Load			± 5	%
V2 Pad Voltage Step	V_{R2}	LCDM4 increased 1		50		mV

V6 Pad Output Voltage (LCD's VLCD depended on LCDM4 register) (9)	VLCD	1/4 Bias & no load	3.8 * V2	3.85 * V2	3.9 * V2	V
		1/5 Bias & no load	4.75 * V2	4.8 * V2	4.85 * V2	
V2 input voltage	VEXT	LCDM3.3=1			1.5	V

(8) PWM current deviation will be ±20%.

(9) Deviation is governed by LCD dot size. More larger LCD dot will get larger deviation..

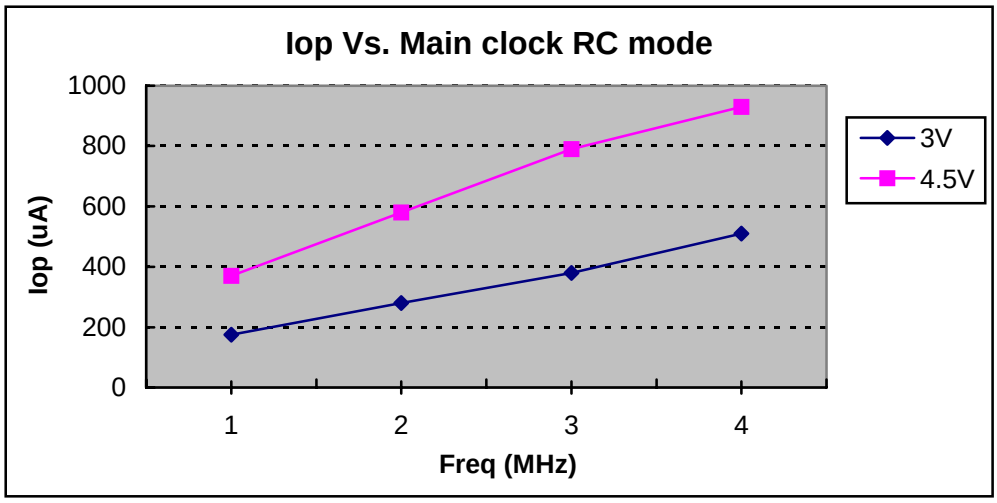
AC CHARATERISTICS

(VDD−VSS = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD on with dot size 0.5mm*0.5mm; unless otherwise specified)

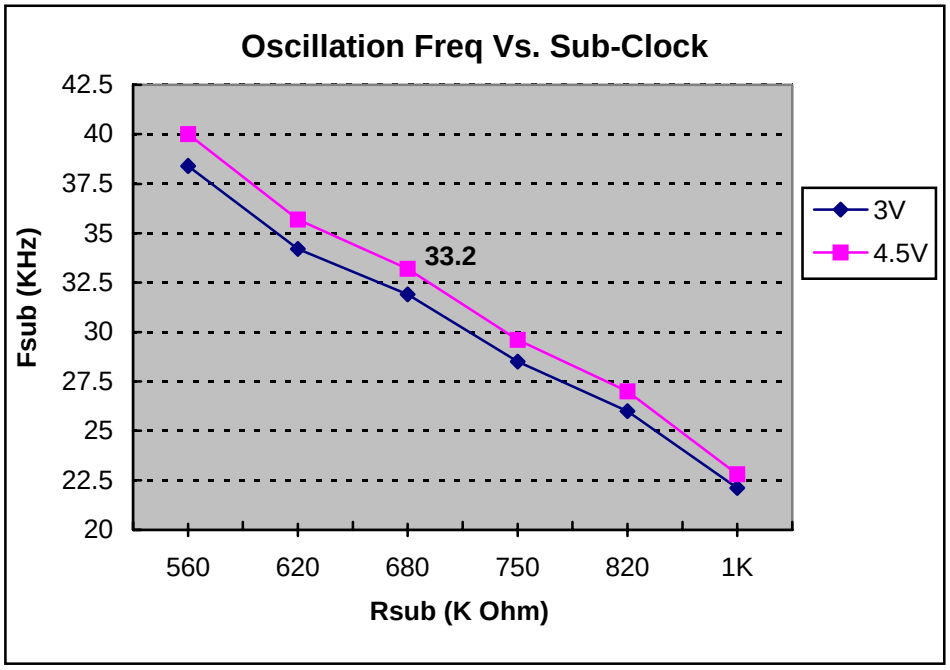
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	FSUB	Crystal type and X32IN and X32O with 17pF external cap.		32768		Hz
Main-clock Frequency	FM	Ring type/Crystal type	400K	-	4M	Hz
Chip Operation Frequency	FOSC	SCR0.0=1,FSYS=FSUB		32768		Hz
		SCR0.0=0;FSYS= FMAIN	400K	-	4M	
Instruction Cycle Time	TCYC	One machine cycle	-	4/FOSC	-	S
Reset Active Width	TRAW	FOSC = 32.768 KHz	1	-	-	µS
Interrupt Active Width	TIAW	FOSC = 32.768 KHz	1	-	-	µS
Main clock Ring frequency (10)	FRXIN	RXIN =680KΩ		1M		Hz
		RXIN =330K Ω		2M		
		RXIN =200KΩ		3M		
		RXIN =150KΩ		4M		
Sub-Clock RC Oscillator	FRSUB	RSUB=680KΩ		32		KHz
Sub-Clock Oscillation Stable Time @ Cold Start	FSTOP	RSUB=680KΩ	0.8		1	S
Frequency Deviation of main-clock FRXIN ≤ 2MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			10	%
Frequency Deviation of main-clock FRXIN = 3 MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			15	%
Frequency Deviation of main-clock FRXIN =4 MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			20	%
ROSC Frequency	FROSC	ROSC=680KΩ		3		MHz
Frequency Deviation of FROSC = 3MHz	$\frac{\Delta f}{f}$	$\frac{f(3V)-f(2.4V)}{f(3V)}$			7.5	%
Frame frequency	FLCD	LCDM1=0111 b (default)		64		Hz

(10)The deviation will be +20% while VDD drops from 5.5V to 2.4V based on same resistor

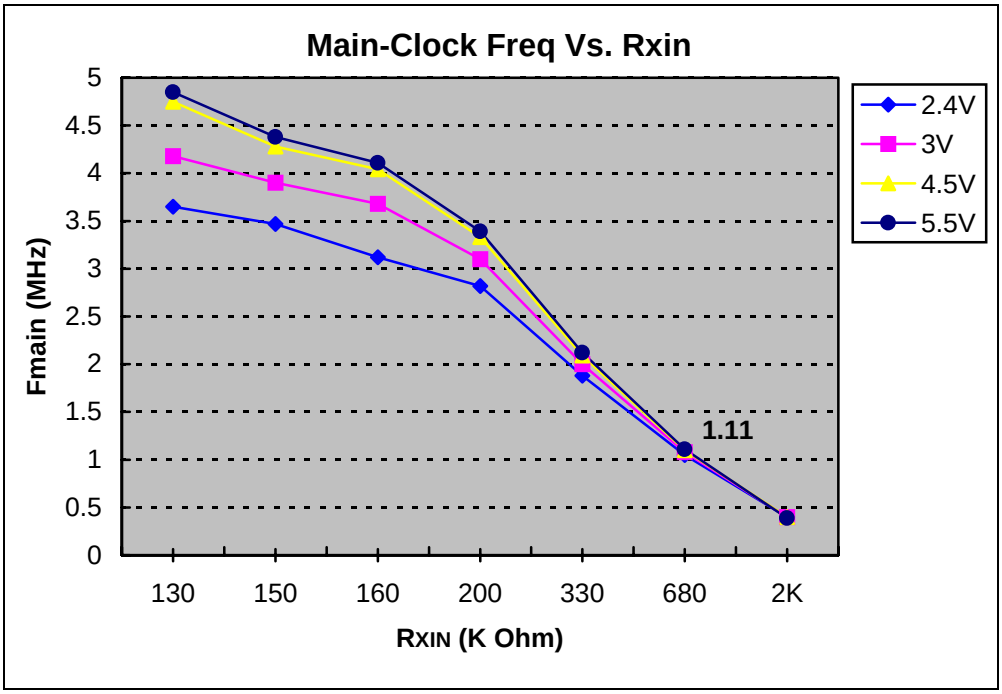
Operating Current Vs. Main clock (RC Mode)



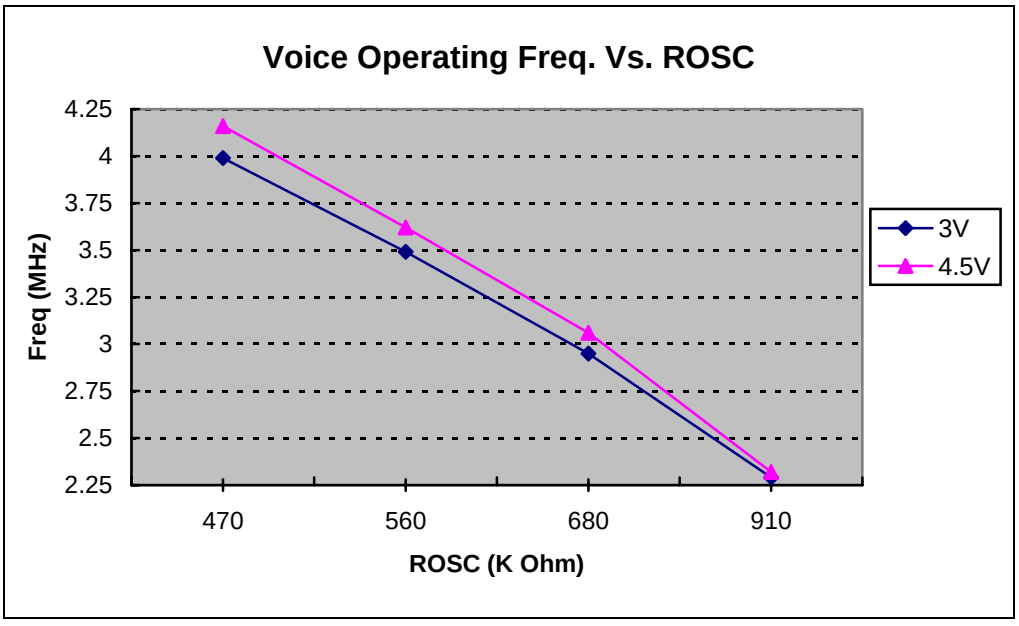
Sub-Clock oscillation Freq Vs. Resistor



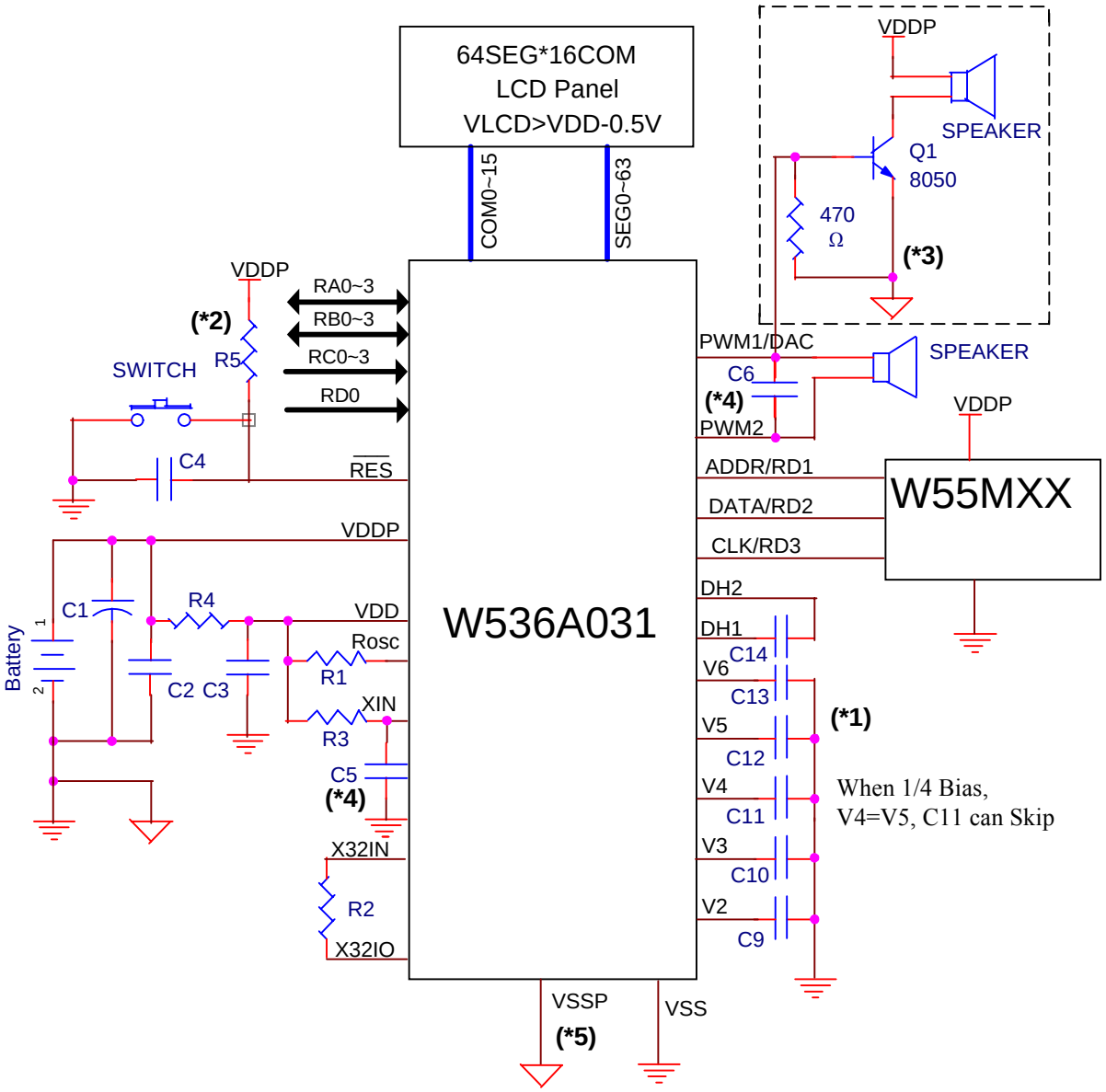
Main-Clock oscillation Freq Vs. Resistor



Voice Operating Freq Vs. Resistor (ROSC)



APPLICATION CIRCUIT-- 1: Sub clock with RC mode



Component	C1	C2~C4	C5, C6	C7, C8	C9~C14	R1	R2	R3	R4
Value	4.7uF	0.1uF	100pF	15~ 30pF	0.1~1uF	680KΩ	680KΩ	650KΩ/1Mhz 350KΩ/2Mhz 225KΩ/3Mhz 160KΩ/4Mhz	100Ω

Note:

(1). C9~C14 depends on LCD panel dot size.

(2). Option R5 equals to 100Ω if high noise immunity is needed.

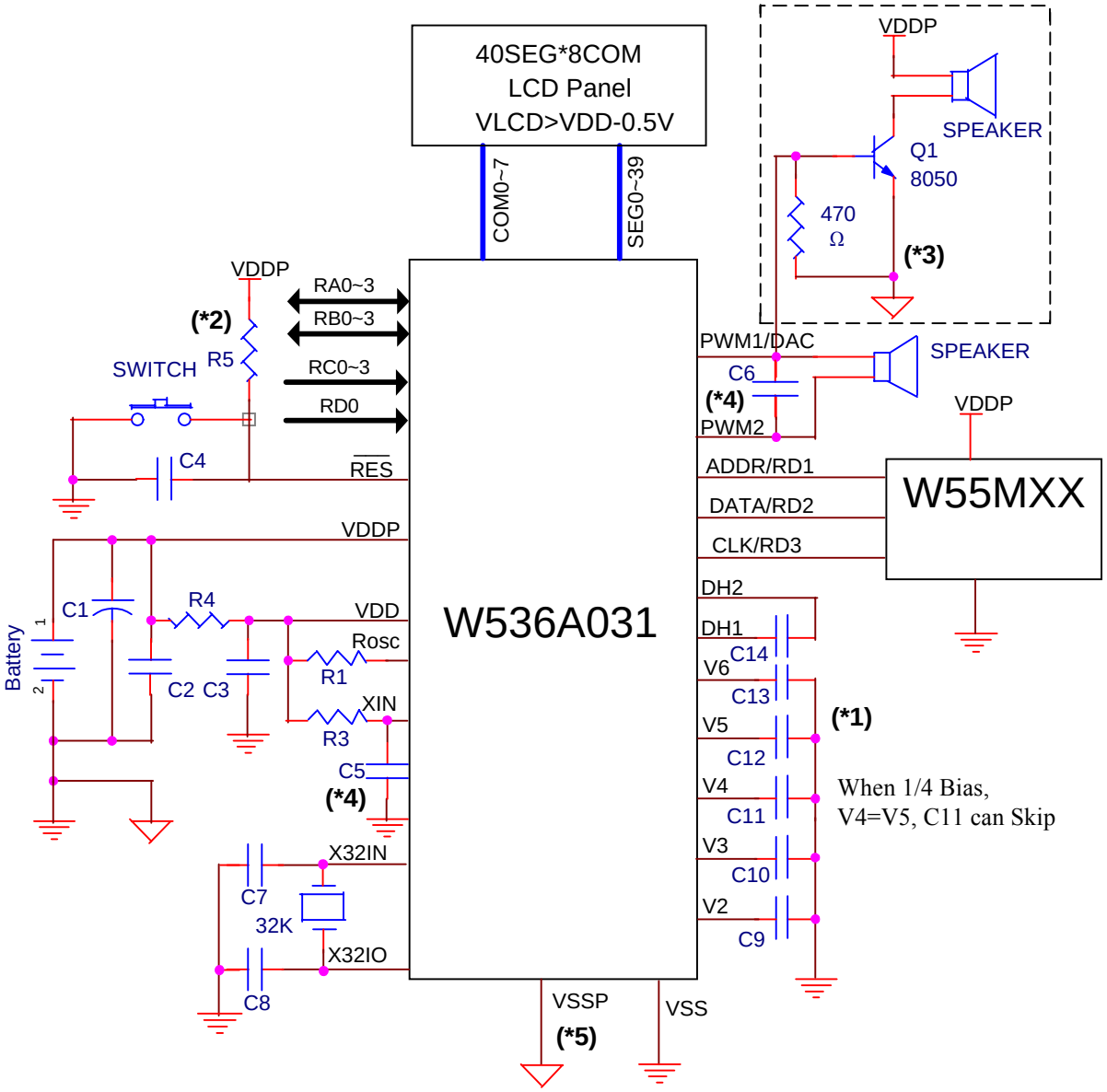
(3). For DAC option application.

(4). To ensure that three batteries function well in W536F20 demo board. C_6 should stay close to pad PWM/PWM2 at its best. Under the mask ROM version, C_5 and C_6 can be skipped.

(5). Sure chip operation properly, please bond all VDDP, VDD, VSSP and VSS; and connect VSSP pad to VSS from external PCB circuit.

(6) Main clock with Ring type, the frequency deviation is depended on VDD and resistor

APPLICATION CIRCUIT--- 2: Sub clock with Crystal mode



Component	C1	C2~C4	C5, C6	C7, C8	C9~C14	R1	R2	R3	R4
Value	4.7uF	0.1uF	100pF	15~ 30pF	0.1~1uF	680KΩ	-	650KΩ/1Mhz 350KΩ/2Mhz 225KΩ/3Mhz 160KΩ/4Mhz	100Ω

Note:

(1). C9~C14 depends on LCD panel dot size.

(2). Option R5 equals to 100Ω if high noise immunity is needed.

(3). For DAC option application.

(4). To ensure that three batteries function well in W536F20 demo board. C_6 should stay close to pad PWM/PWM2 at its best. Under the mask ROM version, C_5 and C_6 can be skipped.

(5). Sure chip operation properly, please bond all VDDP, VDD, VSSP and VSS; and connect VSSP pad to VSS from external PCB circuit.

(6) Main clock with Ring type, the frequency deviation is depended on VDD and resistor