Military-Standard Products

UT7164 Radiation-Hardened 8K x 8 SRAM -- SEU Tolerant

Data Sheet

August 1990

FEATURES

- 55ns maximum address access time, single-event upset less than 1.0×10^{-8} errors/bit-day (−55°C to +125°C)
- Asynchronous operation for compatibility with industry-standard 8K x 8 SRAM
- TTL-compatible input and output levels
- Three-state bidirectional data bus
- Low operating and standby current
- Full military operating temperature range, −55°C to +125°C, screened to specific test methods listed in Table I MIL-STD-883 Method 5004 for Class S or Class B
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0×10^6 rads (Si)
  - Dose rate upset: 1.0×10^9 rads (Si)/sec
  - Dose rate survival: 1.0×10^{12} rads (Si)/sec
  - Single-event upset: $<1.0 \times 10^{-8}$ errors/bit-day
- Industry standard (JEDEC) 64K SRAM pinout
- Packaging options:
  - 28-pin 100-mil center DIP (.600 x 1.2)
  - 28-pin 50-mil center flatpack (.700 x .75)
- 5 volt operation
- Post-radiation AC/DC performance characteristics guaranteed by MIL-STD-883 Method 1019 testing at 1.0×10^6 rads(Si)

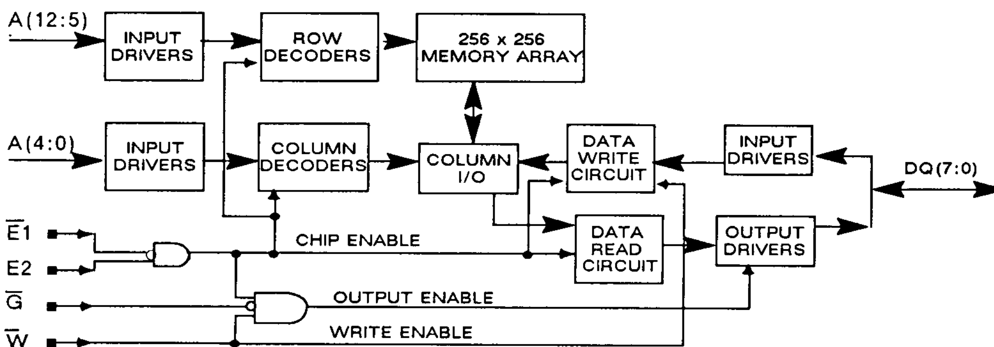

Figure 1. SRAM Block Diagram

INTRODUCTION

The UT7164 SRAM is a high performance, asynchronous, radiation-hardened, 8K x 8 random access memory conforming to industry-standard fit, form, and function. The UT7164 SRAM features fully static operation requiring no external clocks or timing strobes. UTMC designed and implemented the UT7164 SRAM using an advanced radiation-hardened twin-well CMOS process. Advanced CMOS processing along with a device enable/disable function result in a high performance, power-saving SRAM. The combination of radiation-hardness, fast access time, and low power consumption make UT7164 ideal for high-speed systems designed for operation in radiation environments.

PIN NAMES

A(12:0)	Address	$\overline{W}$	Write
DQ(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E1}$	Enable 1	VDD	Power
E2	Enable 2	VSS	Ground

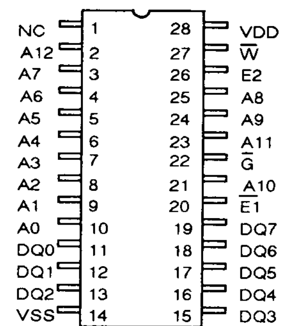

Figure 2. SRAM Pinout

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DEVICE OPERATION

The UT7164 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); thirteen address inputs, A(12:0); and eight bidirectional data lines, DQ(7:0). $\overline{E1}$ and E2 are device enable inputs that control device selection, active, and standby modes. Asserting both $\overline{E1}$ and E2 enables the device, causes IDD to rise to its active value, and decodes the thirteen address inputs to select one of 8,192 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E1}$	E2	I/O Mode	Mode
X(1)	X	X	0	3-state	Stand-by
X	X	1	X	3-state	Stand-by
X	0	0	1	Data in	Write
1	1	0	1	3-state	Read(2)
0	1	0	1	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH}(min), $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a read cycle. Read access time is measured from the latter of device enable, Output Enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Figure 3b shows Read Cycle 2, the Chip Enable-controlled Access. For this cycle, $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(12:0) is accessed and appears at the data outputs DQ(7:0).

Figure 3c shows Read Cycle 3, the Output Enable-controlled Access. For this cycle, $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable before $\overline{G}$ is enabled. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ less than V_{IL}(max), $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access shown in figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by tWLWH when the write is initiated by $\overline{W}$, and by tETWH when the write is initiated by the latter of $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access shown in figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by the latter of $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

RADIATION HARDNESS

The UT7164 SRAM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

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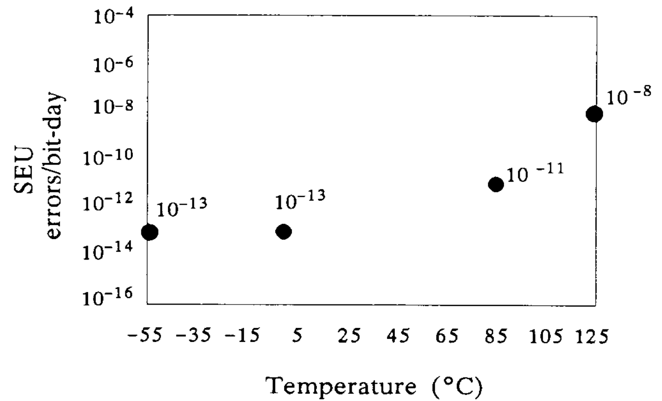
Table 2. Radiation Hardness Design Specifications (1)

Total Dose	1.0E6	rads(Si)
Dose Rate Upset	1.0E9	rads(Si)/s 20ns pulse
Dose Rate Survival	1.0E12	rads(Si)/s 20ns pulse
Single-Event Upset	1.0E-8	errors/bit-day (2)
Neutron Fluence	3.0E14	n/cm²

Notes:
1. The SRAM will not latch up during radiation exposure under recommended operating conditions.
2. 90% Adam's worst case spectrum (-55°C to +125°C).

Table 3. SEU versus Temperature



ABSOLUTE MAXIMUM RATINGS (1)
(Referenced to VSS)

SYMBOL	PARAMETER	LIMITS
VDD	DC supply voltage	-0.3 to 7.0
VI/O	Voltage on any pin	-0.5 to VDD +0.5
TSTG	Storage temperature	-65 to +150°C
PD	Maximum power dissipation	500 mW
TJ	Maximum junction temperature	+175°C
ΘJC	Thermal resistance, junction-to-case (2)	10°C/W
ILU	Latchup immunity (see figure 6b)	+/-150 mA
II	DC input current	+/-10 mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
VDD	Positive supply voltage	4.5 to 5.5	V
TC	Case temperature range	-55 to +125	°C
VIN	DC input voltage	0 to VDD	V

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DC ELECTRICAL CHARACTERISTICS (Post-Radiation)*

(VDD = 5.0V +/-10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
VIH	High-level input voltage		2.2		V
VIL	Low-level input voltage			0.8	V
VOL	Low-level output voltage	IOL = 8mA, VDD = 4.5V		0.4	V
VOH	High-level output voltage	IOH = -8mA, VDD = 4.5V	2.4		V
CIN	Input capacitance (1)	F = 1MHz @ 0V, VDD = 4.5V		15	pF
CIO	Bidirectional I/O capacitance (1)	F = 1MHz @ 0V, VDD = 4.5V		20	pF
IIN	Input leakage current	VIN = VDD and VSS	-10	10	uA
IOZ	Three-state output leakage current TTL outputs	VO = VDD and VSS VDD = 5.5V $\overline{G}$ = 5.5V	-10	10	uA
IOS	Short-circuit output current (2, 3)	VDD = 5.5V, VO = VDD VDD = 5.5V, VO = 0V	 -90	90 	mA mA
IDD(OP)	Supply current operating @1MHz	CMOS inputs (i.e. IOUT = 0) VDD = 5.5V		10	mA
IDD(SB) pre-rad	Supply current standby	CMOS inputs (i.e. IOUT = 0) $\overline{E1}$ = VDD - 0.5 VDD = 5.5V E2 = VSS + 0.5		200	uA

Notes:
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1 x 10^6 rads(Si).

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

(VDD = 5.0V +/-10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	7164-85		7164-70		7164-55		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
tAVAV	Read cycle time	85		70		55		ns
tAVQV	Read access time		85		70		55	ns
tAXQX	Output hold time	5		5		5		ns
tGLQX	$\overline{G}$-controlled output enable time	0		0		0		ns
tGLQV	$\overline{G}$-controlled output enable time (Read Cycle 3)		30		15		15	ns
tGHQZ	$\overline{G}$-controlled output three-state time		15		10		10	ns
tETQX (1)	E-controlled output enable time	0		0		0		ns
tETQV (1)	E-controlled access time		85		70		55	ns
tEFQZ (2)	E-controlled output three-state time		20		15		15	ns

Notes:
1. The ET (enable true) notation refers to the rising edge of E2 or the falling edge of $\overline{E1}$, whichever comes last. SEU immunity does not affect the read parameters.
2. The EF (enable false) notation refers to the falling edge of E2 or the rising edge of $\overline{E1}$, whichever comes first. SEU immunity does not affect the read parameters.

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1 x 10^6 rads(Si).

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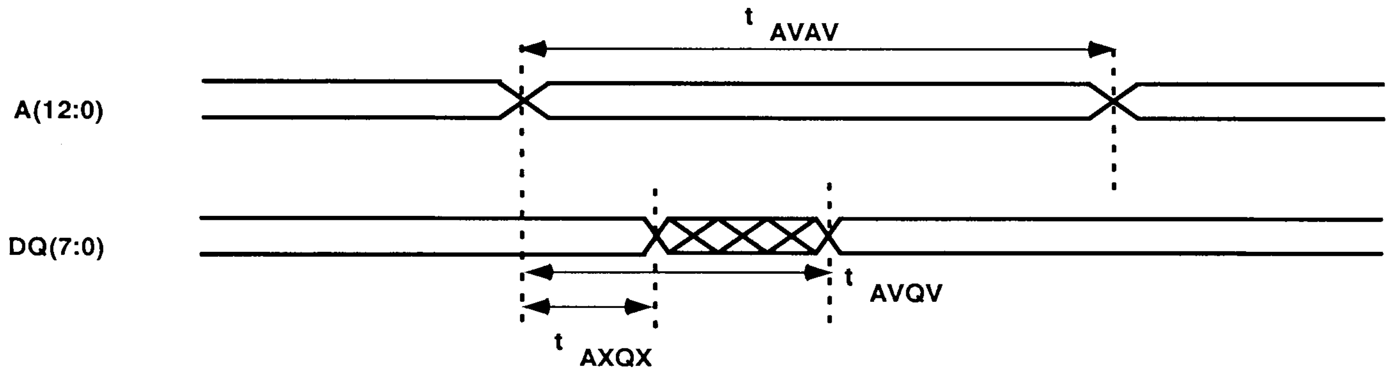
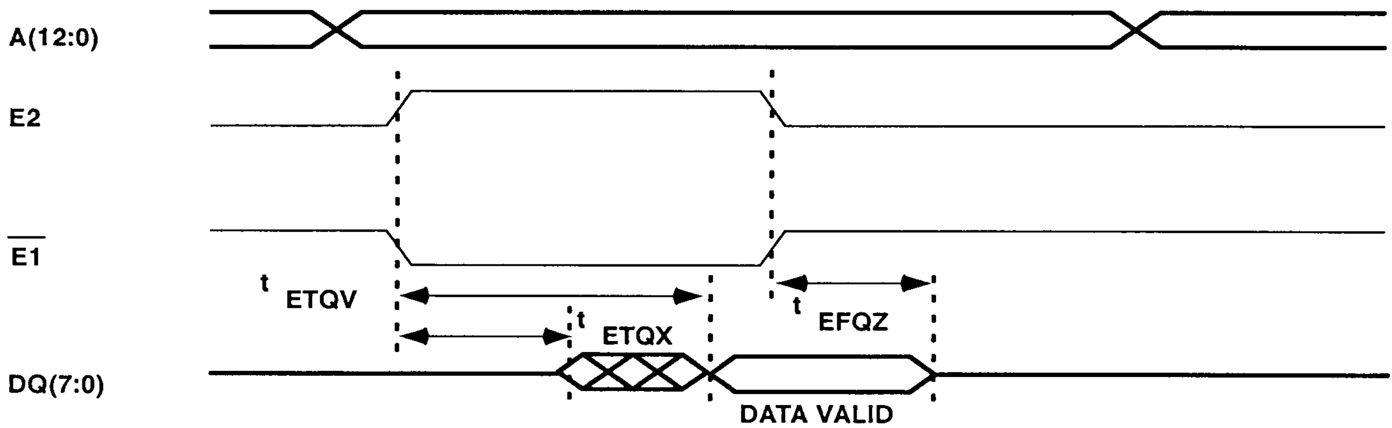


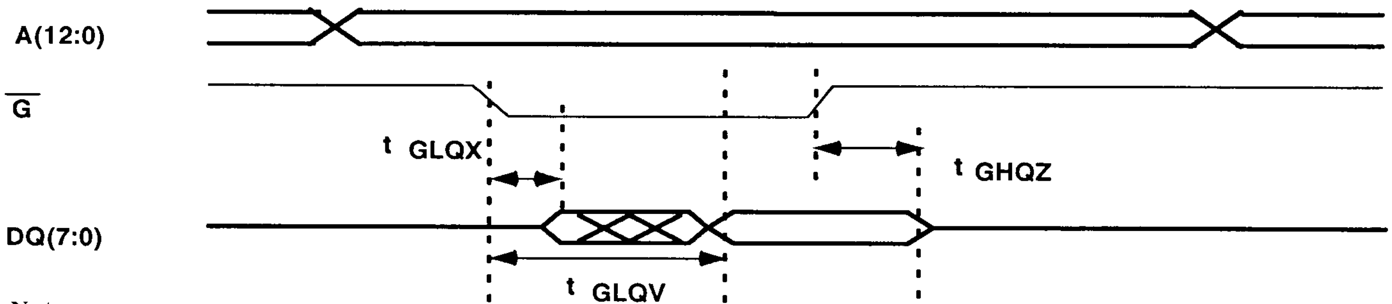
Notes:
1) $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max)
2) E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Note:
$\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Notes:
1) $\overline{E1} \leq V_{IL}$ (max)
2) E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

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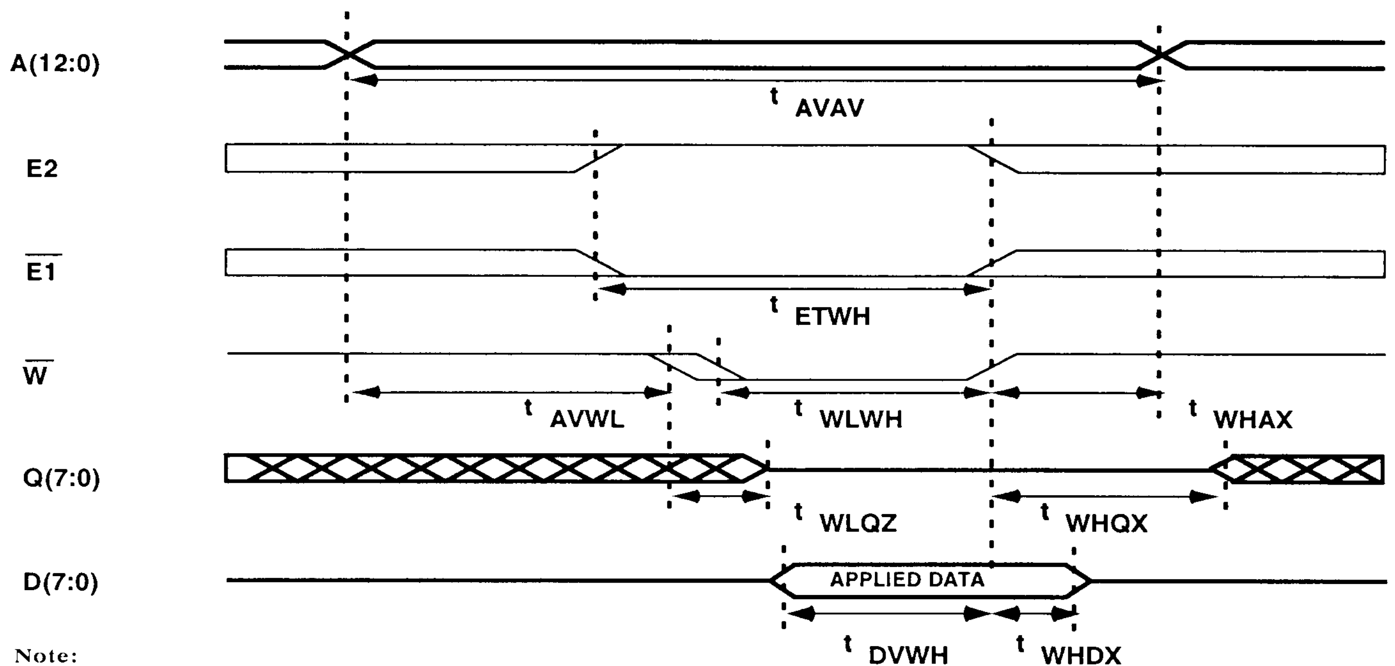
AC CHARACTERISTICS WRITE CYCLE (Post-Radiation)*
(VDD = 5.0V +/-10%; -55°C < TC < +125°C)

SYMBOL	PARAMETER	7164-85		7164-70		7164-55		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
tAVAV	Write cycle time	65		60		50		ns
tETWH	Device enable to end of write	65		60		50		ns
tAVET	Address setup time for write ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
tAVWL	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns
tWLWH	Write pulse width	50		35		35		ns
tWHAX	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns
tEFAX	Address hold time for device enable ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
tWLQZ	$\overline{W}$-controlled three-state time		15		15		15	ns
tWHQX	$\overline{W}$-controlled output enable time	0		0		0		ns
tETEF	Device enable pulse width ($\overline{E1}$ or E2 - controlled)	65		60		50		ns
tDVWH	Data setup time	50		35		35		ns
tWHDX	Data hold time	0		0		0		ns
tWLEF	Device enable controlled write pulse width	65		60		50		ns
tDVEF	Data setup time	50		35		35		ns
tEFDX	Data hold time	0		0		0		ns

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1 x 10^6 rads(Si).



Note:
1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.

Figure 4a. SRAM Write Cycle 1: $\overline{W}$-Controlled Access

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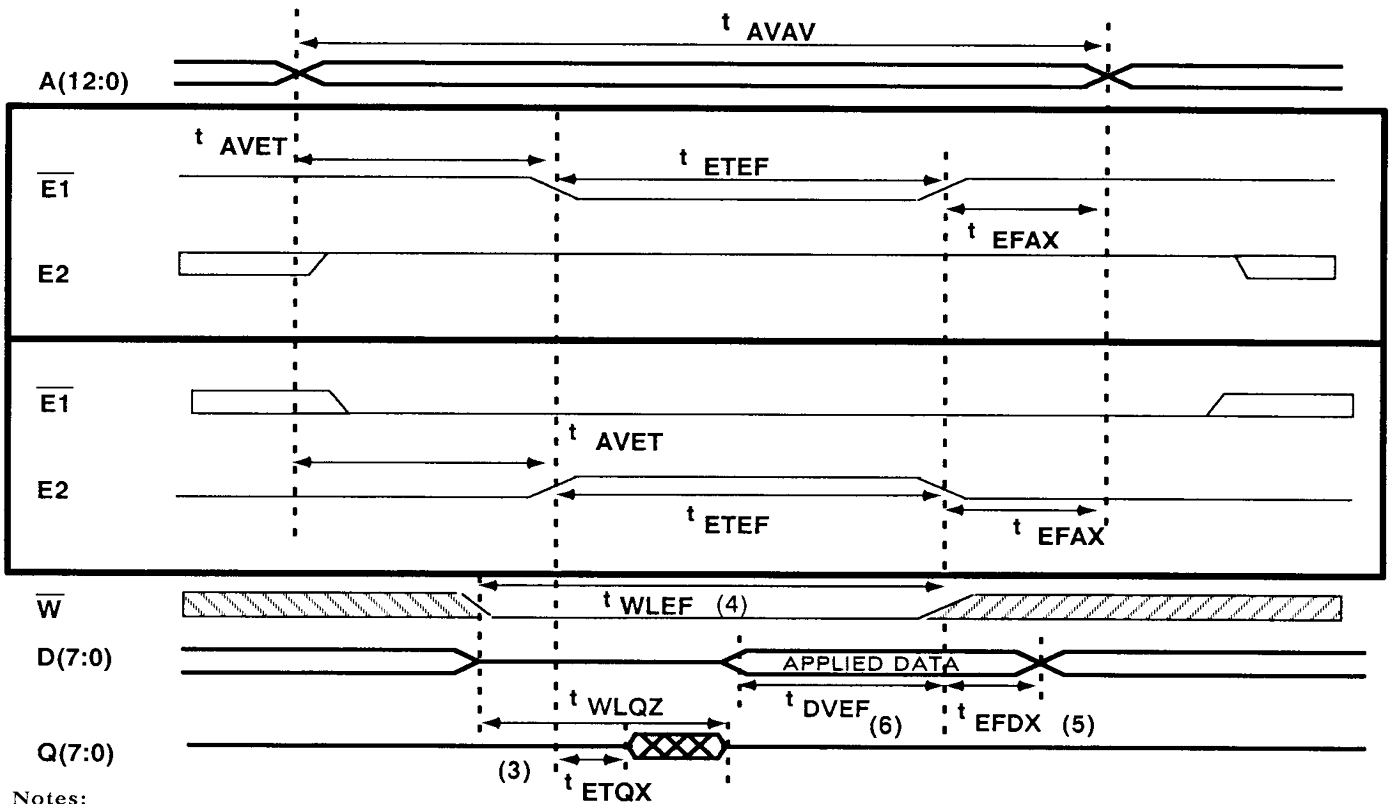

Notes:
1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.
2) Either $\overline{E1}$/E2 scenario above can occur.
3) If $\overline{E1}$ or E2 is asserted simultaneously with or after the $\overline{W}$ low transition, the outputs will remain in a high-impedance state.
4) $t_{WLEF} = t_{ETWH}$
5) $t_{EFDX} = t_{WHDX}$
6) $t_{DVEF} = t_{DVWH}$

Figure 4b. SRAM Write Cycle 2: Enable-Controlled Access

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DATA RETENTION CHARACTERISTICS (Post-Radiation)*
(TC = 25°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM VDD @ 2.0V	MAXIMUM VDD @ 3.0V	UNIT
VDR	VDD for data retention	2.0	--	--	V
IDDDR	Data retention current (1)	--	60	90	μA
tEFR	Chip deselect to data retention time (1)	0			ns
tR	Operation recovery time (1)	tAVAV			ns

Note:
1. a. VLC = 0.2V
VHC = VDD -0.2V
$\overline{E1}$ ≥ VHC, E2 > VHC

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1 x 10^6 rads(Si).

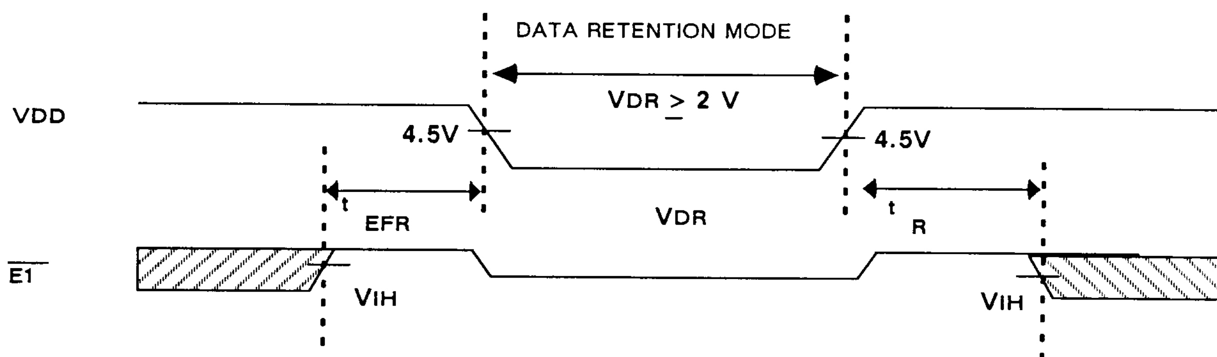

Figure 5. Low VDD Data Retention Waveform

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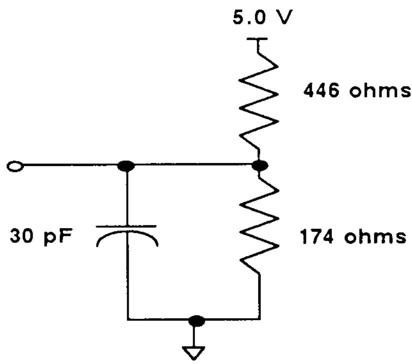

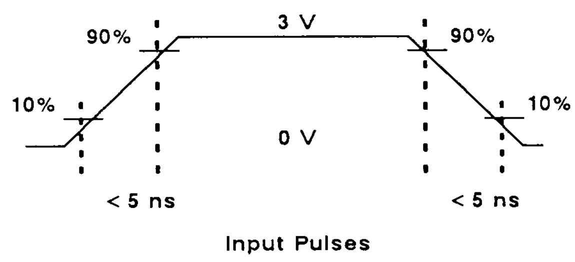

Notes:
1. 30 pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point.

Figure 6a. AC Test Loads and Input Waveforms

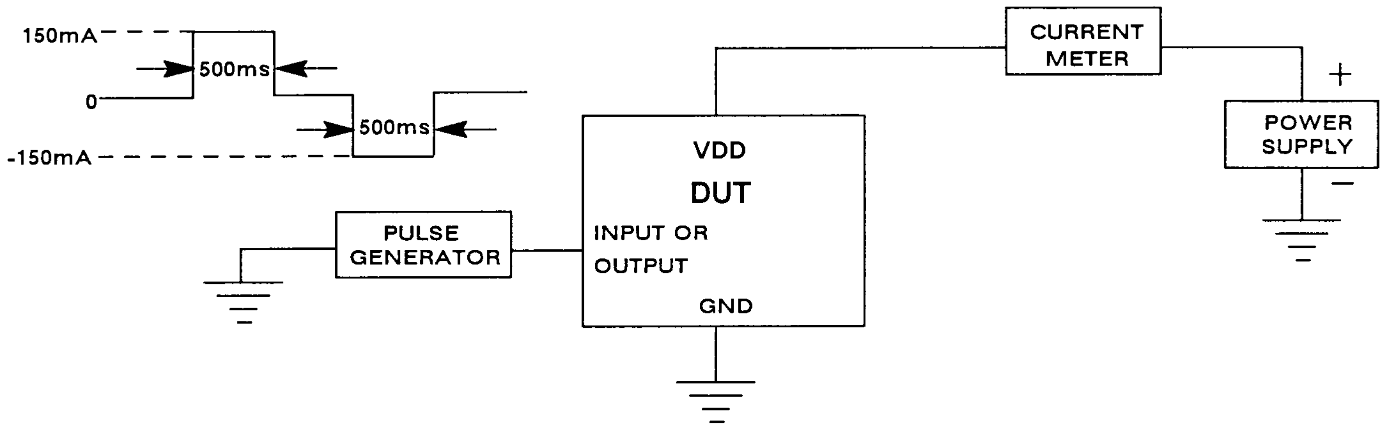

Figure 6b. Latchup Test

LATCHUP TEST CONFIGURATION

Figure 6b shows the latchup test. VDD holds at +5.5 VDC, and VSS holds at ground. The device test is at 125°C. Each type of I/O alternately receives a positive and then negative 150 mA pulse of 500 ms duration. The current is monitored after the pulse for latchup condition. To prevent burnout, the supply current is limited to 400 mA.

The SRAM has latchup immunity in excess of +150 mA for 500 ms.

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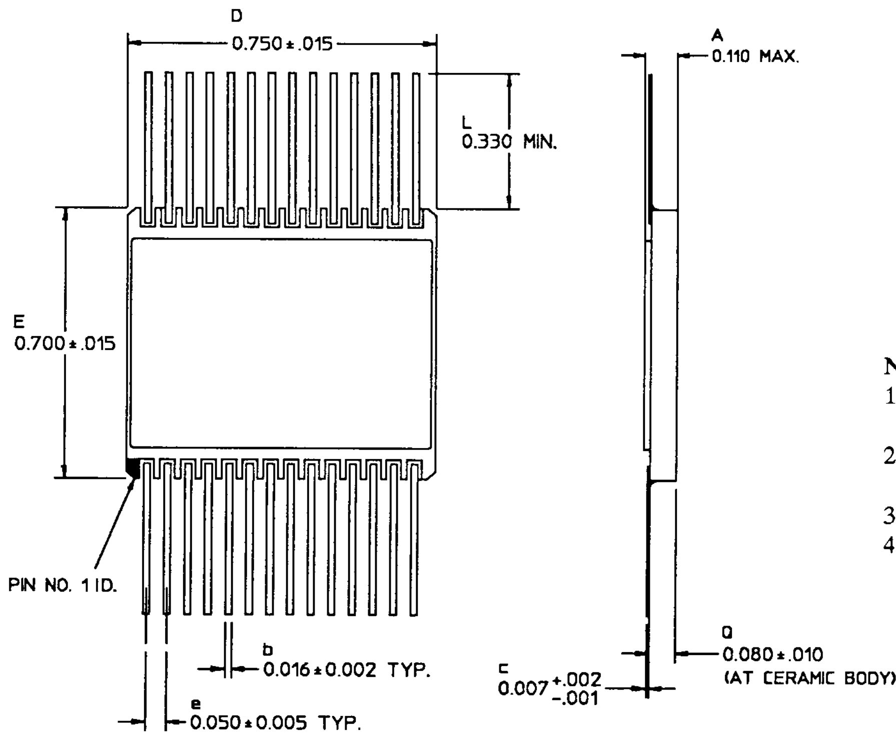
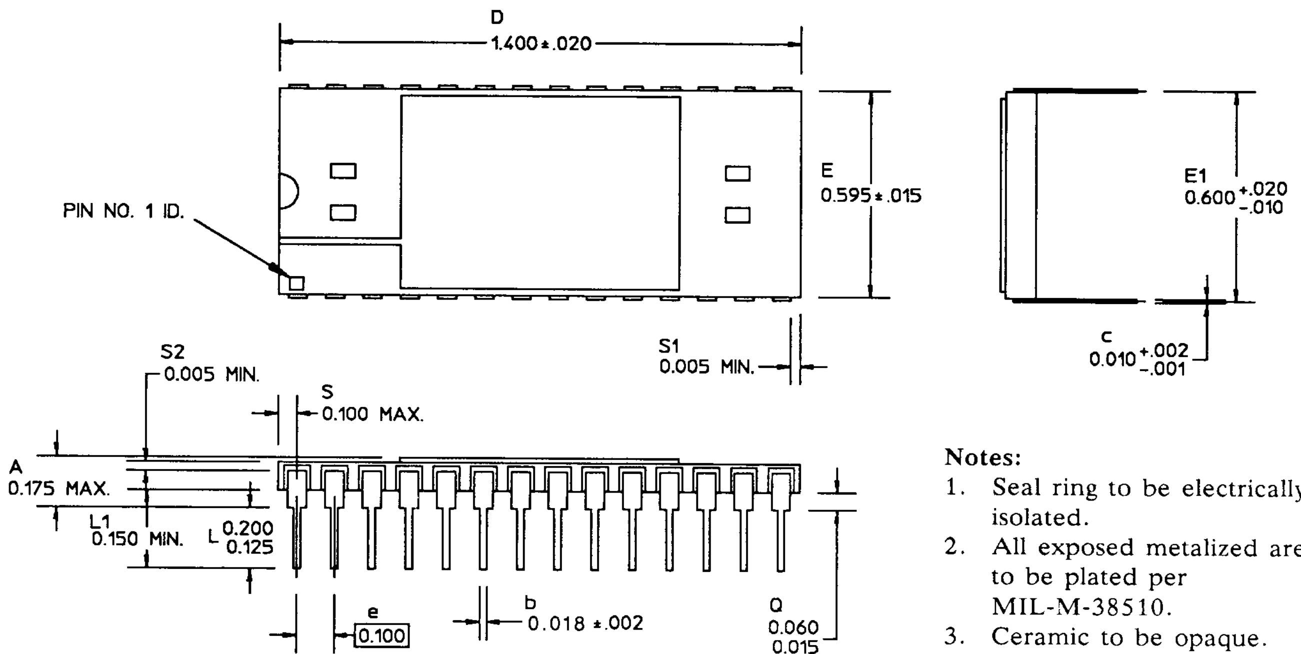


Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-M-38510.

Figure 7a. 28-pin Ceramic Flatpack



Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-M-38510.

Figure 7b. 28-pin Ceramic DIP Package

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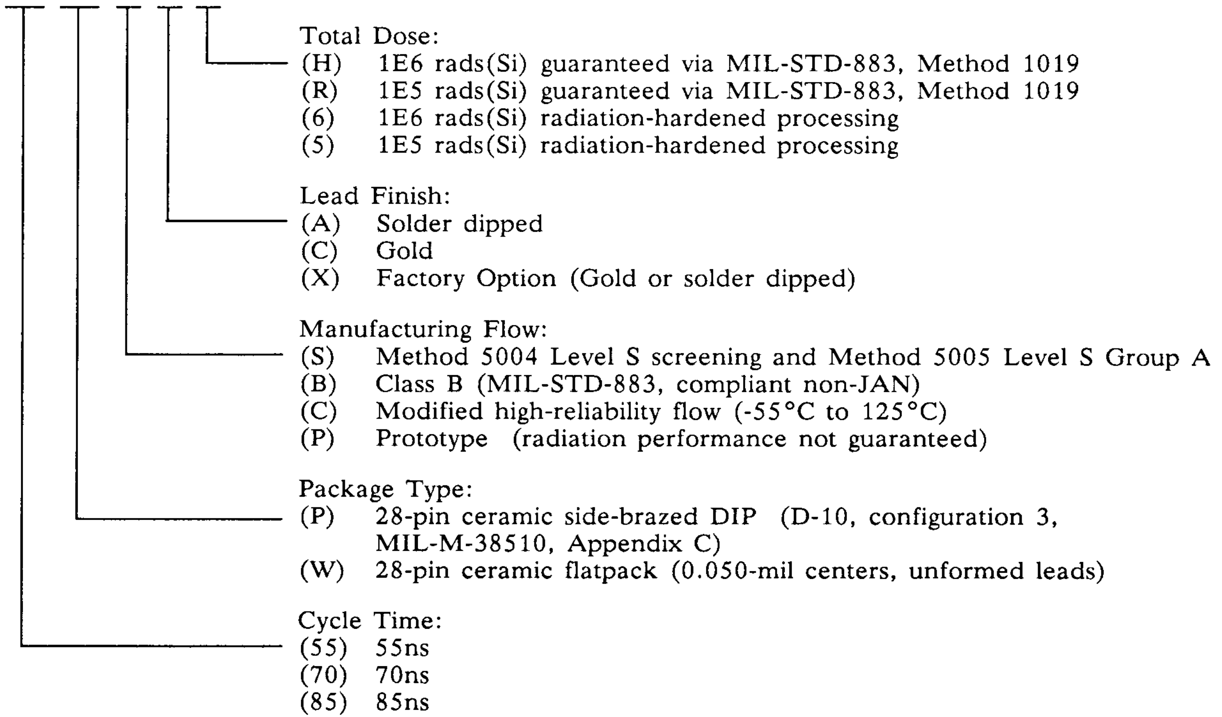
ORDERING INFORMATION

To order the UT7164 SRAM, use the following part number guide:



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