NEC

User's Manual

OSD LSIs

μPD6461
μPD6462
μPD6464A
μPD6465
μPD6466

Document No. S13197EJ1V0UMJ1 (1st Edition)
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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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PREFACE

Target users

This user's manual is intended for users who understand the functions of the μPC6461, μPD6462, μPD6464A, μPD6465, and μPD6466 on-screen character display CMOS LSIs (OSD LSIs) and who will design and develop application systems for them.

Purpose

The purpose of this user's manual is to help users understand the basic functions of OSD LSIs. Hardware configurations that appear in this manual are illustrative examples only, and there is no plan for their mass production.

Configuration

This user's manual consists of the following chapters.

- CHAPTER 1 OVERVIEW
- CHAPTER 2 BASIC OPERATION
- CHAPTER 3 APPLICATION EXAMPLES
- CHAPTER 4 FAQ
- CHAPTER 5 DEVELOPMENT TOOLS

How to read this manual

Readers of this manual should have a general understanding of electrical and logic circuits, microcontrollers, and video signal processing.

Legend

Data significance	:	Higher digits on the left and lower digits on the right
Active low representation	:	$\overline{\times\times\times}$ (overscore over pin or signal name)
Note	:	Footnote for item marked with **Note** in the text
Caution	:	Information requiring particular attention
Remark	:	Supplementary information
Numerical representation	:	Binary ..... ×××× or 0b××××
		Decimal ..... ××××
		Hexadecimal .... 0x××××

Related documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Data sheets

μPD6461	(Document number: S12588E)
μPD6462	(Document number: S12593E)
μPD6464A, μPD6465	(Document number: S11043E)
μPD6466	(Document number: S10991E)

User's manuals

OSD LSIs	(This manual)
OSD LSI Character Pattern Editor for Windows™	(To be prepared)
Character Pattern Editor for On-Screen Display LSI[Note]	(Document number: S10153E)

Note This manual is for MS-DOS™ (for PC-9801) and PC DOS™ (for IBM PC/AT™).

Information

ROM Code Ordering Method	(Document number: C10302J)[Note]

Note This document number is that of Japanese version.

Caution The related documents listed above may be changed without notice. Be sure to use the latest documents for design and other purposes.

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[MEMO]

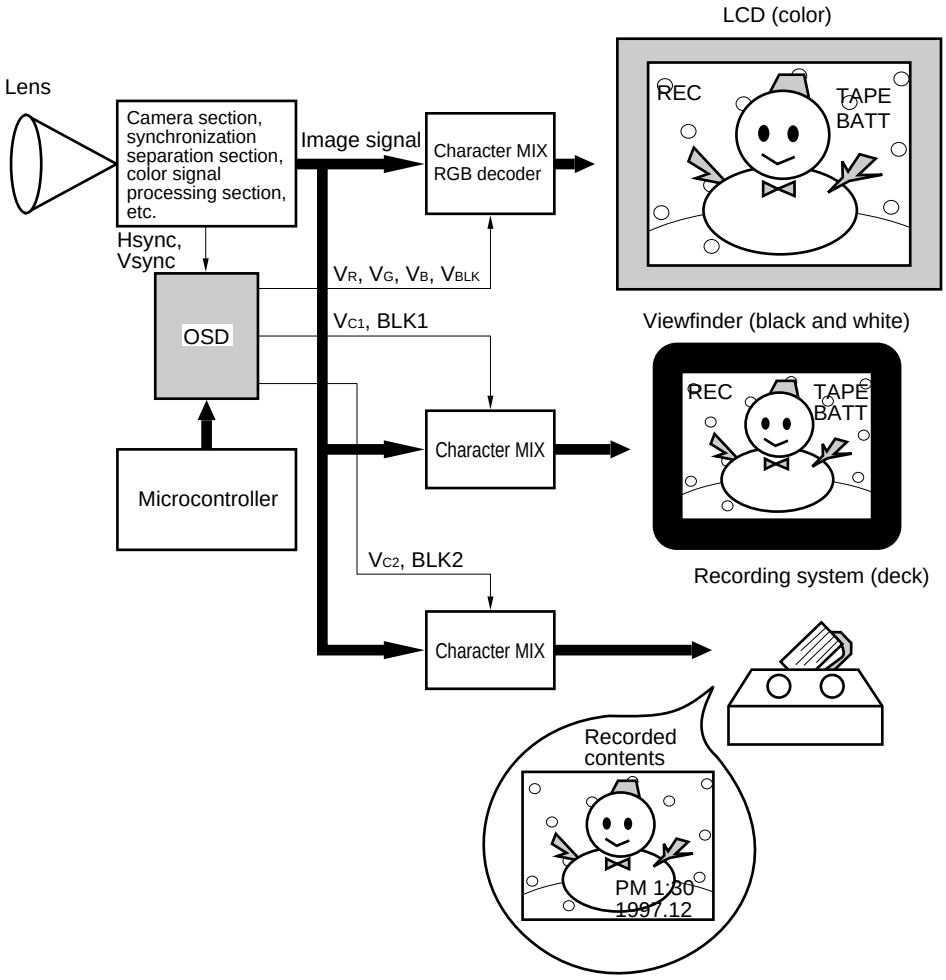
CHAPTER 1 OVERVIEW

The on-screen character display CMOS LSI (OSD LSI) is used to display character data on various types of monitor screens. The size of one character is 12 (horizontal) by 18 (vertical) dots, and up to 12 lines of 24 columns (288 characters) can be displayed. The character types are determined by the ROM capacity of each product. NEC has 128-character (μPD6462, μPD6464A), 256-character (μPD6461, μPD6465), and 512-character (μPD6466) OSD LSIs.

Also, the NEC OSD LSIs are broadly divided into video-system OSD LSIs (μPD6464A, μPD6465) and RGB-system OSD LSIs (μPD6461, μPD6462, μPD6466) according to their use. By combining it with a microcontroller, a video-system OSD LSI controls not only the program screen of a deck-type VCR or LD player, but also various indicators (such as the tape counter). An RGB-system OSD LSI controls the display of the counter, time, date, and other indicators on the viewfinder of a camcorder, the transcription of the time, date, and other indicators on a video tape, and the display of the channel or other indicators on a TV screen.

This user's manual describes the operation of OSD LSIs and presents several practical examples of their use.

Figure 1-1. Sample Uses of OSD LSIs (RGB-System OSD LSI: Camcorder)



1.1 List of OSD LSIs

Table 1-1. List of OSD LSIs

	Video-system		RGB-system		
Sample uses	TV, video, video CD		Camcorder, DVD, LCD TV, digital still camera		
Product name	μPD6464A	μPD6465	μPD6461	μPD6462	μPD6466
Character type	128	256	256	128	512
Number of display characters	12 lines × 24 columns (288 characters)				
Dot matrix	12 (horizontal) × 18 (vertical) dots				
Character color	Single color (white) (select brightness level for the screen from 75IRE/95IRE)		8 colors		
Character size (unit: lines)	1× and 2× (simultaneous horizontal and vertical specification)				1×, 2×, 3×, and 4× (independent horizontal and vertical specifications)
Character color inversion (unit: characters)	None		Black characters (no framing)		Black characters (framing control disabled) White characters (framing control enabled)
Character left-right inversion (unit: characters)	None				Available (cannot be used when blinking is specified)
Blinking (unit: characters)	Blinking ratio is 1:1 (blinking frequency can be selected for the entire screen from the three options corresponding to approximately 0.5, 1, and 2 Hz)				
Internal video signal color	White, black, blue, or green		None		White or blue (effective only for RGB-system output)
Background (unit: screen)	No background, black framing, black-on-white, black filling				
Background color (unit: screen)	Single color (black)		8 colors (RGB-system output) or single color (black: V_{C1} and V_{C2} system output)		
Framing color (unit: screen)	Single color (black)		2 colors (white and black)		
Supported video signal method	NTSC, PSL, PAL-M, SECAM, or PAL-N (μPD6464A only)		—		
Video signal input/output	Composite video signal		No input/output system		
Character signal output	Character signal and blanking signal		RGB + 3BLK or RGB + V_{C1} + V_{C2} (for μPD6461 and μPD6462, select according to mask code option; for μPD6466, select according to command)		
Video RAM data clear	Video RAM data can be cleared by the video RAM batch clear command and the power-ON clear function				
Interface with microcontroller	Serial input type of 8-bit variable word length				
Operation power supply range	4.5 to 5.5 V		2.7 to 5.5 V		
Packages	24-pin SDIP 24-pin SOP		20-pin SSOP 24-pin SOP	20-pin SSOP	20-pin SSOP 24-pin SOP

1.2 Ordering Information

Table 1-2. Ordering Information

	Part Number	Package	NEC standard ROM code number
Video-system	μPD6464ACS-×××	24-pin plastic shrink DIP (300 mils)	001
	μPD6464AGT-×××	24-pin plastic SOP (375 mils)	101
	μPD6465CS-×××	24-pin plastic shrink DIP (300 mils)	001
	μPD6465GT-×××	24-pin plastic SOP (375 mils)	101
RGB-system	μPD6461GS-×××	20-pin plastic shrink SOP (300 mils)	101: MSB first, 3-line unit setting, RBG + 3BLK, option B, LC oscillation 102: MSB first, 3-line unit setting, RBG + V_{C1} + V_{C2}, option B, LC oscillation
	μPD6461GT-×××	24-pin plastic SOP (375 mils)	—
	μPD6462GS-×××	20-pin plastic shrink SOP (300 mils)	001: MSB first, 3-line unit setting, RBG + V_{C1} + V_{C2}, option C, LC oscillation
	μPD6466GS-×××	20-pin plastic shrink SOP (300 mils)	001
	μPD6466GT-×××	24-pin plastic SOP (375 mils)	201

Remarks 1. ××× indicates ROM code suffix.

2. For the μPD6461 and μPD6462, the following are selected according to the mask code option (for the μPD6466, they can be selected according to the initialization command or the CMDCT pin). For details, refer to the data sheet for each product.

- Data transfer : LSB first or MSB first
- Vertical display start position : 3-line unit setting or 9-line unit setting
- Pin selection : RBG + V_{C1} + V_{C2} or RGB + 3BLK
- Output selection : Option A, option B, or option C
- Dot clock : LC oscillation or external clock input

1.3 Pin Configurations

Figure 1-2. μPD6464A or μPD6465 Pin Configuration (Top View)

24-pin plastic shrink DIP (300 mils)

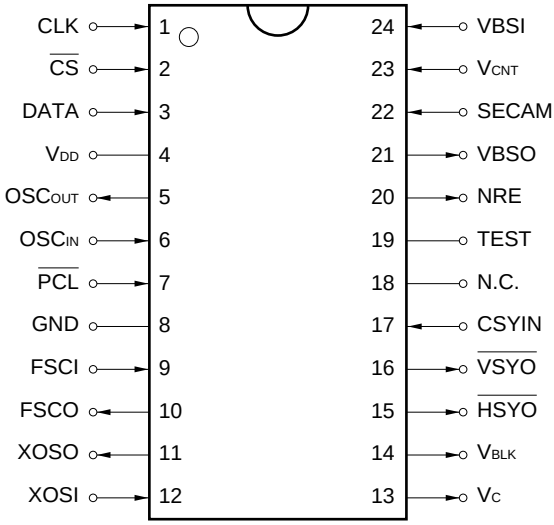
μPD6464ACS-×××

μPD6465CS-×××

24-pin plastic SOP (375 mils)

μPD6464AGT-×××

μPD6465GT-×××



Remark ××× indicates ROM code suffix.

CLK : Clock Input
$\overline{CS}$: Chip Select Input
CSYIN : Composite Synchronization Signal Input
DATA : Serial Data Input
FSCI : f_{SC} Signal Input
FSCO : Frequency Error Output
GND : Ground
$\overline{HSYO}$: Horizontal Synchronization Signal Output
N.C. : No Connection
NRE : Noise Reduction Constant Append
OSC_{IN} : LC Oscillation Input
OSC_{OUT} : LC Oscillation Output
$\overline{PCL}$: Power-on Clear
SECAM : SECAM subcarrier Input
TEST : Test Pin
V_{BLK} : Blanking Signal Output
VBSI : Composite Video Signal Input
VBSO : Composite Video Signal Output
V_C : Character Signal Output
V_{CNT} : Video Signal Output Level Adjustment
V_{DD} : Power Supply
$\overline{VSYO}$: Vertical Synchronization Signal Output
XOSI : Quadruple Oscillation Input
XOSO : Quadruple Oscillation Output

Table 1-3. List of μPD6464A and μPD6465 Pin Functions

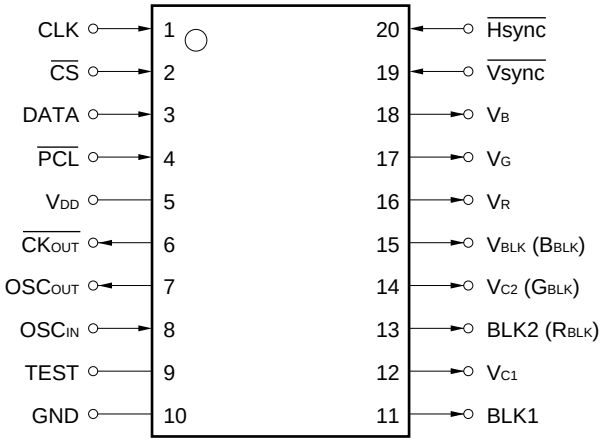
Pin No.	Pin Symbol	Pin Name	Function
1	CLK	Clock Input	Inputs clock for data read. Data input to the DATA pin is read at the rising edge of the clock input to this pin.
2	$\overline{CS}$	Chip Select Input	Serial transfer can be acknowledged by making this $\overline{CS}$ pin low.
3	DATA	Serial Data Input	Inputs control data. Data is read in synchronization with the clock input to the CLK pin.
4	V_{DD}	Power Supply	Supplies power to the IC.
5 6	OSC_{OUT} OSC_{IN}	LC Oscillation Output LC Oscillation Input	These are input and output pins of an oscillator that generates dot clocks. Connect a coil and a capacitor to these pins for oscillation.
7	$\overline{PCL}$	Power-ON Clear	Power-ON clear pin. Make this pin high on power application. It initializes the internal circuitry of the IC.
8	GND	Ground	Ground pin of the IC.
9	FSCI	fsc Signal Input	Inputs color subcarrier signal (fsc) when quadruple oscillation is selected. Connect it to GND or V_{CC} when 4fsc crystal oscillation is selected.
10	FSCO	Frequency Error Output	Frequency error output signal of the ×4 multiplier. Leave it open when 4fsc crystal oscillation is selected.
11	XOSO	Quadruple Oscillation Output	The quadruple oscillator LC for internal video signal generation is connected to these pins. A crystal oscillator also can be connected.
12	XOSI	Quadruple Oscillation Input	
13	V_C	Character Signal Output	Character signal output pin, which is high active.
14	V_{BLK}	Blanking Signal Output	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_C output and is high active.
15	$\overline{HSYO}$	Horizontal Synchronization Signal Output	Outputs a horizontal synchronization signal separated from the composite synchronization signal.
16	$\overline{VSYO}$	Vertical Synchronization Signal Output	Outputs a vertical synchronization signal separated from the composite synchronization signal.
17	CSYIN	Composite Synchronization Signal Input	Inputs a composite synchronization signal for synchronization separation. Always input this signal when external video signal mode is used. The input polarity is positive synchronization.
18	N.C.	No Connection	Free pin. Leave this pin open.
19	TEST	Test Pin	Test mode select pin. Generally, connect this pin to GND.
20	NRE	Noise Reduction Constant Append	Constant append pin for noise reduction.
21	VBSO	Composite Video Signal Output	Outputs a composite video signal with which the character signal is mixed.
22	SECAM	SECAM subcarrier Input	SECAM subcarrier signal mixing pin. When a mode other than SECAM is selected, leave this pin open.
23	V_{CNT}	Video Signal Output Level Adjustment	Adjusts the output level adjustment of the composite video signal and luminance signal.
24	VBSI	Composite Video Signal Input	Inputs a composite video signal. Inputs a signal with the leading edge clamped, consisting of a negative synchronization and positive video signal.

Figure 1-3. μPD6461 or μPD6462 Pin Configuration (Top View)

20-pin plastic shrink SOP (300 mils)

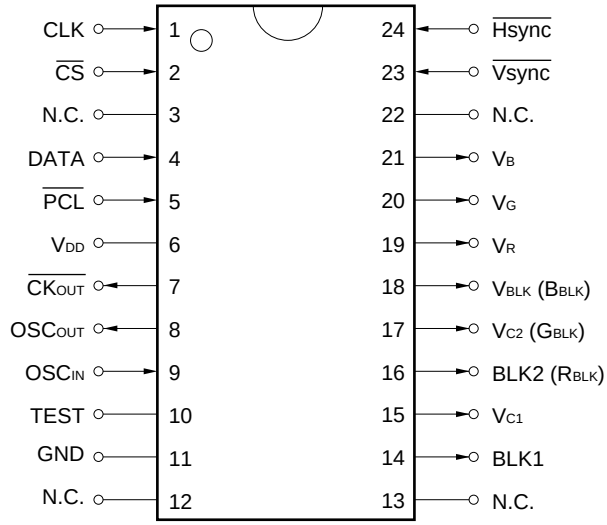
μPD6461GS-×××

μPD6462GS-×××



24-pin plastic SOP (375 mils)

μPD6461GT-×××



Remarks 1. ××× indicates ROM code suffix.

2. The symbols enclosed in parentheses are set by the mask code option (RGB + Blanking corresponding to RGB).

B_{BLK} : Blanking B
BLK1, BLK2 : Blanking Output 1, 2
$\overline{CK_{OUT}}$: Clock Output
CLK : Clock Input
$\overline{CS}$: Chip Select
DATA : Data Input
G_{BLK} : Blanking G
GND : Ground
$\overline{Hsync}$: Horizontal Synchronous Signal Input
N.C. : No Connection
OSC_{IN} : Oscillator Input
OSC_{OUT} : Oscillator Output
$\overline{PCL}$: Power-on Clear
R_{BLK} : Blanking R
TEST : Test
V_B : Character Signal Output
V_{BLK} : Blanking Signal Output for V_R, V_G, and V_B
V_{C1}, V_{C2} : Character Signal output 1, 2
V_{DD} : Power supply
V_G : Character Signal Output
V_R : Character Signal Output
$\overline{Vsync}$: Vertical Synchronous Signal Input

Table 1-4. List of μPD6461 and μPD6462 Pin Functions

Pin No.[Note 1]	Pin Symbol[Note 2]	Pin Name[Note 2]	Function
1	CLK	Clock Input	Inputs clock for data read. Data input to the DATA pin is read at the rising edge of the clock input to this pin.
2	$\overline{CS}$	Chip Select Input	Serial transfer can be acknowledged by making this $\overline{CS}$ pin low.
3 (4)	DATA	Serial Data Input	Inputs control data. Data is read in synchronization with the clock input to the CLK pin.
4 (5)	$\overline{PCL}$	Power-ON Clear	Power-ON clear pin. Make this pin high on power application. It initializes the internal circuitry of the IC.
5 (6)	V_{DD}	Power Supply	Supplies power to the IC.
6 (7)	$\overline{CK_{OUT}}$	Clock Output	Checks the oscillation frequency. It uses N-channel open-drain output.
7 (8) 8 (9)	OSC_{OUT} OSC_{IN}	LC Oscillation Input/Output (OSC_{IN}: External clock input)	These are input and output pins of an oscillator that generates dot clocks. Connect a coil and a capacitor to these pins for oscillation. (When external clock input is selected by the mask option, the external clock (clock synchronized with $\overline{Hsync}$) is input. OSC_{OUT} is left open.)
9 (10)	TEST	Test Pin	IC test pin. Connect this pin to GND.
10 (11)	GND	Ground	Connect this pin to the system GND.
11 (14)	BLK1	Blanking Signal Output 1	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_{C1} output and is high active. (When blanking corresponding to RGB is selected by the mask option, the logical sum of R_{BLK}, G_{BLK}, and B_{BLK} is output.)
12 (15)	V_{C1}	Character Signal Output 1	Outputs the character signal. It is high active. (When blanking corresponding to RGB is selected by the mask option, the logical sum of V_R, V_G, and V_B is output.)
13 (16)	BLK2 (R_{BLK})	Blanking Signal Output 2 (Blanking R)	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_{C2} output and is high active. (The blanking signal corresponding to V_R output is output. It is high active.)
14 (17)	V_{C2} (G_{BLK})	Character Signal Output 2 (Blanking G)	Outputs the character signal. It is high active. (The blanking signal corresponding to V_G output is output. It is high active.)
15 (18)	V_{BLK} (B_{BLK})	Blanking Signal Output (Blanking B)	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_R, V_G, and V_B output and is high active. (The blanking signal corresponding to V_B output is output. It is high active.)
16 (19) 17 (20) 18 (21)	V_R V_G V_B	Character Signal Output	Character signal output pin, which is high active.
19 (23)	$\overline{Vsync}$	Vertical Synchronization Signal Input	Inputs the vertical synchronization signal. Input using negative synchronization.
20 (24)	$\overline{Hsync}$	Horizontal Synchronization Signal Input	Inputs the horizontal synchronization signal. Input using negative synchronization.
(3,12,13,22)	N.C.	No Connection	Free pin.

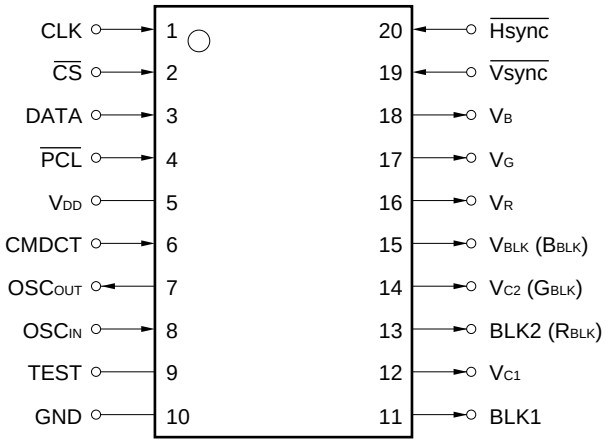
Notes 1. The numbers enclosed in parentheses are pin numbers for the μPD6461GT-×××.

2. The symbols and names enclosed in parentheses are set by the mask code option (RGB + Blanking corresponding to RGB).

Figure 1-4. μPD6466 Pin Configuration (Top View)

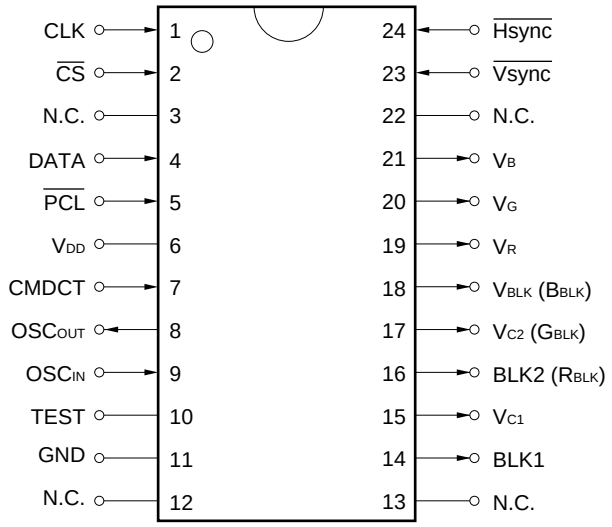
20-pin plastic shrink SOP (300 mils)

μPD6466GS-×××



24-pin plastic SOP (375 mils)

μPD6466GT-×××



Remarks 1. ××× indicates ROM code suffix.

2. The symbols enclosed in parentheses are set by the initialization command (RGB + Blanking corresponding to RGB).

B_{BLK} : Blanking B
BLK1, BLK2 : Blanking Output 1, 2
CLK : Clock
CMDCT : Command Control
$\overline{CS}$: Chip Select
DATA : Data Input
G_{BLK} : Blanking G
GND : Ground
$\overline{Hsync}$: Horizontal Synchronous Signal Input
N.C. : No Connection
OSC_{IN} : Oscillator Input
OSC_{OUT} : Oscillator Output
$\overline{PCL}$: Power-on Clear
R_{BLK} : Blanking R
TEST : Test
V_B : Character Signal Output
V_{BLK} : Blanking Signal Output for V_R, V_G, and V_B
V_{C1}, V_{C2} : Character Signal output 1, 2
V_{DD} : Power supply
V_G : Character Signal Output
V_R : Character Signal Output
$\overline{Vsync}$: Vertical Synchronous Signal Input

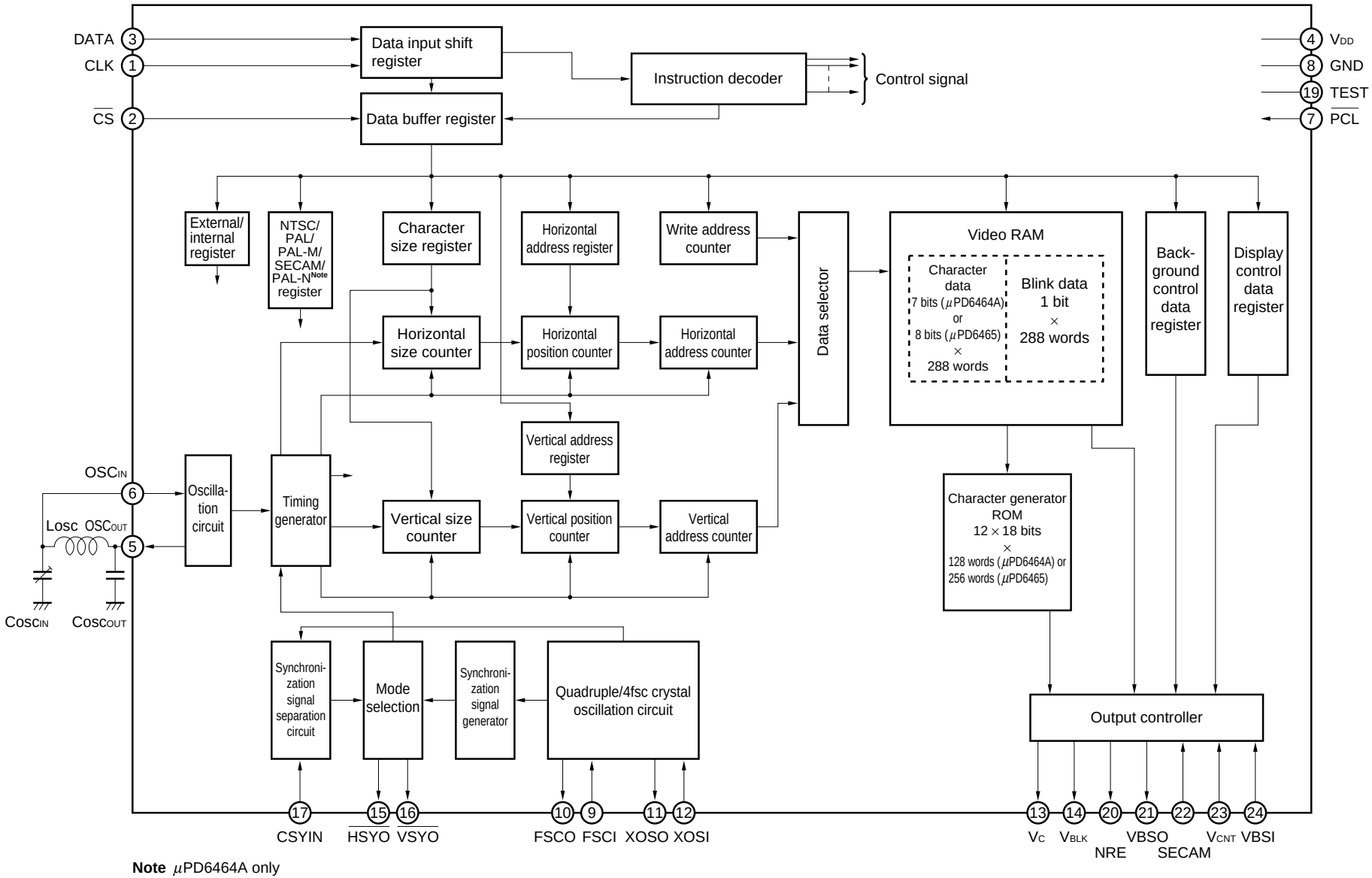
Table 1-5. List of μPD6466 Pin Functions

Pin No.[Note 1]	Pin Symbol[Note 2]	Pin Name[Note 2]	Function
1	CLK	Clock Input	Inputs clock for data read. Data input to the DATA pin is read at the rising edge of the clock input to this pin.
2	$\overline{CS}$	Chip Select Input	Serial transfer can be acknowledged by making this $\overline{CS}$ pin low.
3 (4)	DATA	Serial Data Input	Inputs control data. Data is read in synchronization with the clock input to the CLK pin.
4 (5)	$\overline{PCL}$	Power-ON Clear	Power-ON clear pin. Make this pin high on power application. It initializes the internal circuitry of the IC.
5 (6)	V_{DD}	Power Supply	Supplies power to the IC.
6 (7)	CMDCT	Command Control	Switches between LSB-first and MSB-first input for commands. When this pin is low, LSB-first input is used. When it is high, MSB-first input is used. When using LSB-first input, this pin can be left open.
7 (8) 8 (9)	OSC_{OUT} OSC_{IN}	LC Oscillation Input/Output (OSC_{IN}: External clock input)	These are input and output pins of an oscillator that generates dot clocks. Connect a coil and a capacitor to these pins for oscillation. (When external clock input is selected by the initialization command, the external clock (clock synchronized with $\overline{Hsync}$) is input. OSC_{OUT} is left open.)
9 (10)	TEST	Test	IC test pin. Connect this pin to GND.
10 (11)	GND	Ground	Connect this pin to the system GND.
11 (14)	BLK1	Blanking Signal Output 1	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_{C1} output and is high active. (When blanking corresponding to RGB is selected by the command, the logical sum of R_{BLK}, G_{BLK}, and B_{BLK} is output.)
12 (15)	V_{C1}	Character Signal Output 1	Outputs the character signal. It is high active. (When blanking corresponding to RGB is selected by the command, the logical sum of V_R, V_G, and V_B is output.)
13 (16)	BLK2 (R_{BLK})	Blanking Signal Output 2 (Blanking R)	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_{C2} output and is high active. (The blanking signal corresponding to V_R output is output. It is high active.)
14 (17)	V_{C2} (G_{BLK})	Character Signal Output 2 (Blanking G)	Outputs the character signal. It is high active. (The blanking signal corresponding to V_G output is output. It is high active.)
15 (18)	V_{BLK} (B_{BLK})	Blanking Signal Output (Blanking B)	This pin outputs a blanking signal that cuts the video signal. It corresponds to V_R, V_G, and V_B output and is high active. (The blanking signal corresponding to V_B output is output. It is high active.)
16 (19) 17 (20) 18 (21)	V_R V_G V_B	Character Signal Output	Character signal output pin, which is high active.
19 (23)	$\overline{Vsync}$	Vertical Synchronization Signal Input	Inputs the vertical synchronization signal. Input using negative synchronization.
20 (24)	$\overline{Hsync}$	Horizontal Synchronization Signal Input	Inputs the horizontal synchronization signal. Input using negative synchronization.
(3,12,13,22)	N.C.	No Connection	Free pin.

Notes 1. The numbers enclosed in parentheses are pin numbers for the μPD6466GT-×××.

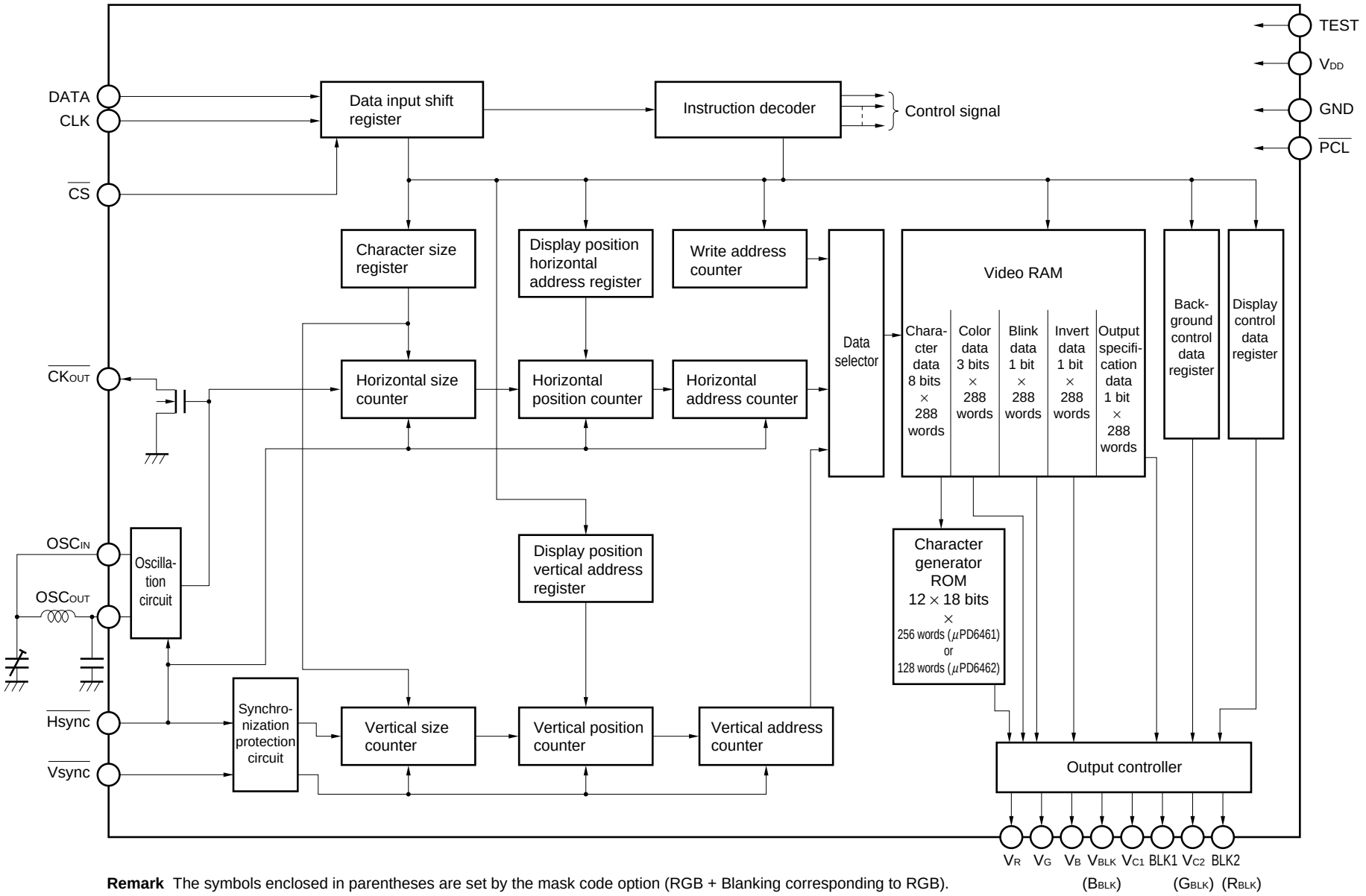
2. The names enclosed in parentheses are set by the initialization command (RGB + Blanking corresponding to RGB).

Figure 1-5. μPD6464A and μPD6465 Block Diagram



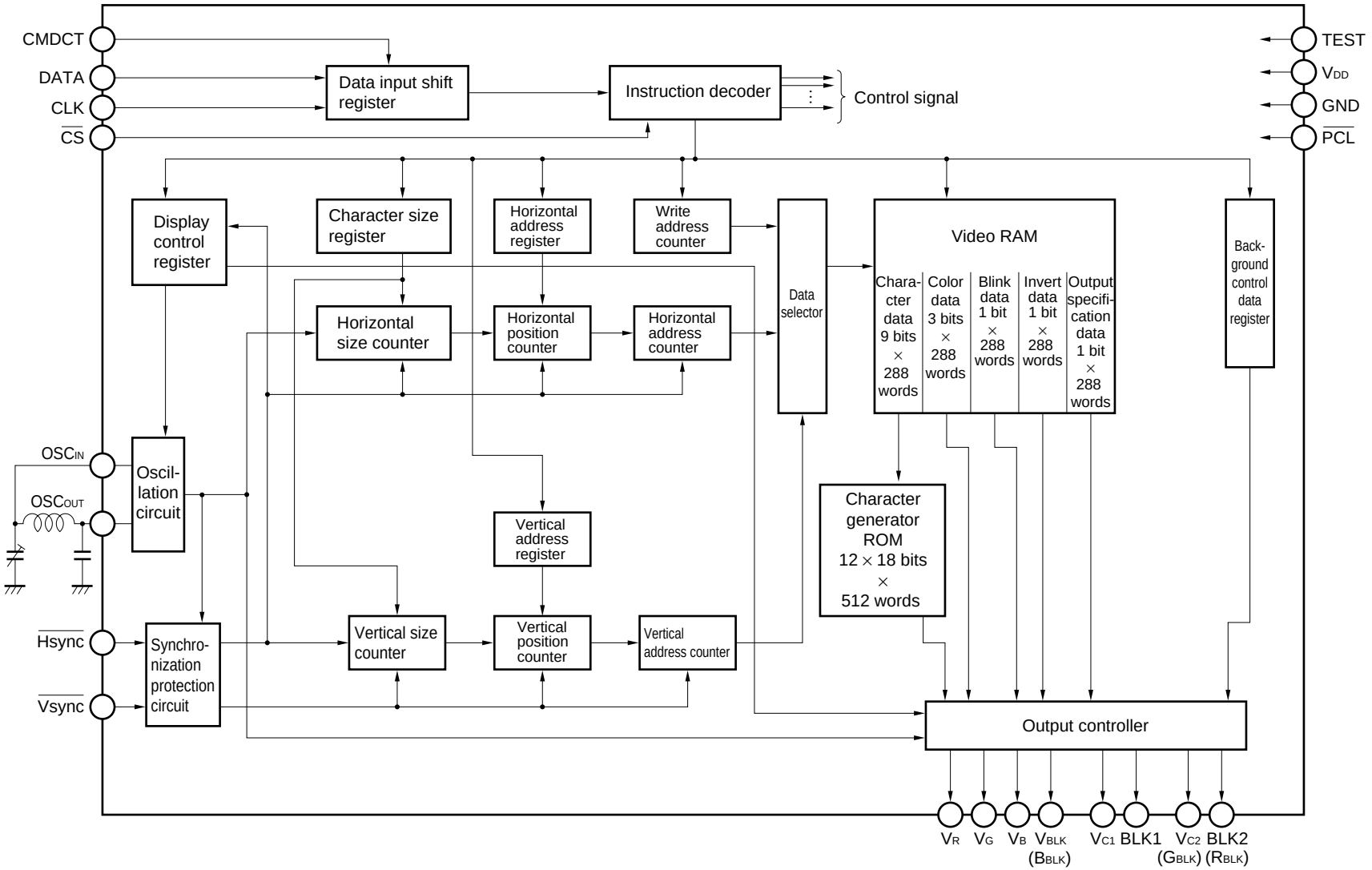
Note μPD6464A only

Figure 1-6. μPD6461 and μPD6462 Block Diagram



Remark The symbols enclosed in parentheses are set by the mask code option (RGB + Blanking corresponding to RGB).

Figure 1-7. μPD6466 Block Diagram



Remark The symbols enclosed in parentheses are set by the initialization command (RGB + Blanking corresponding to RGB).

CHAPTER 2 BASIC OPERATION

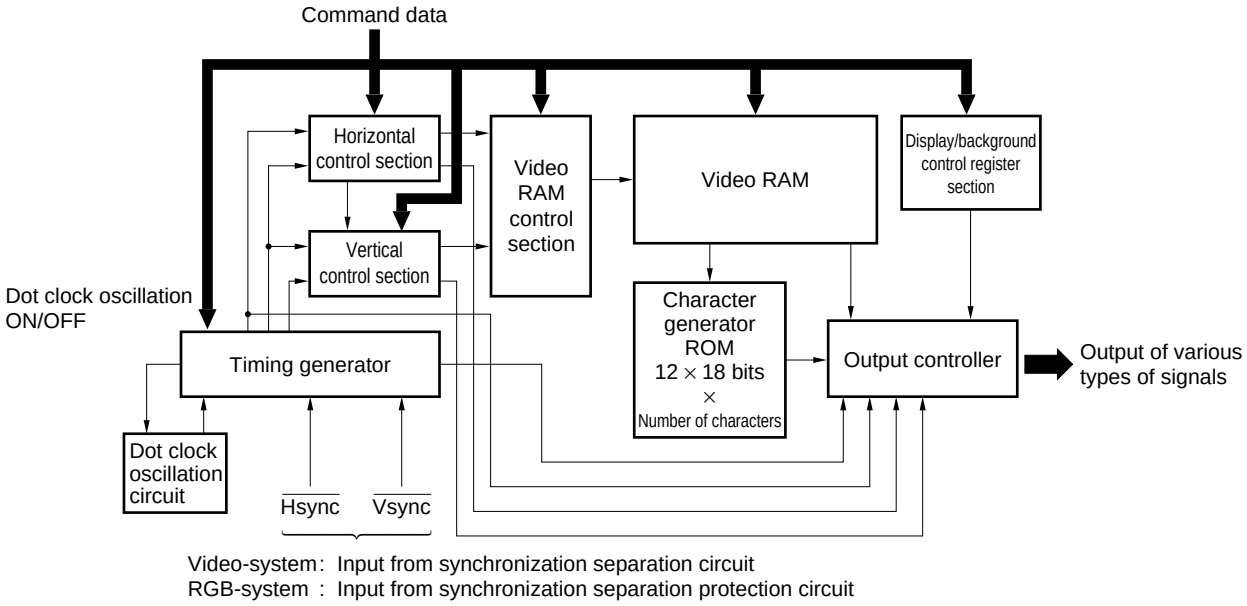
This chapter describes the basic operation of an OSD LSI.

2.1 OSD LSI Configuration

An OSD LSI consists of a dot clock oscillation circuit, timing generator, horizontal control section, vertical control section, video RAM control section, video RAM, character generator ROM, display/background control register section, and output controller.

The OSD LSI, which is controlled by command data sent from a microcontroller, displays the character data stored in the character generator ROM (μPD6462 and μPD6464A: 128 characters; μPD6461 and μPD6465: 256 characters; μPD6466: 512 characters) on the display screen.

Figure 2-1. OSD LSI Basic Block Diagram

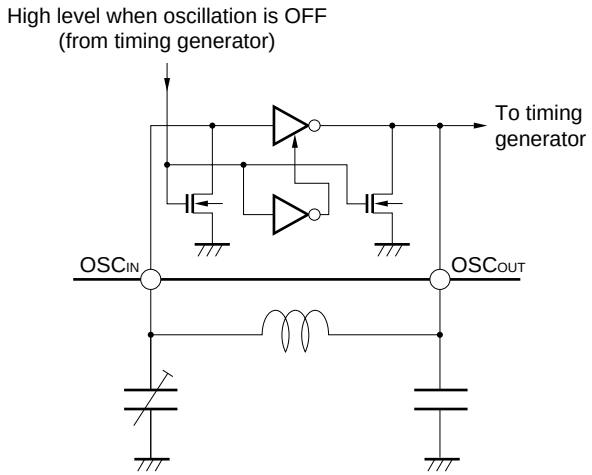


2.1.1 Dot clock oscillation circuit

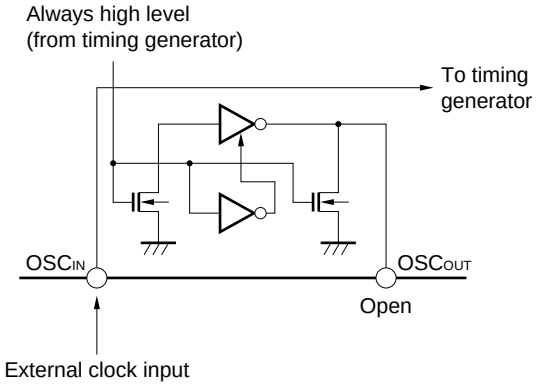
The dot clock oscillation circuit consists of the OSD LSI and an externally connected LC circuit. With an RGB-system OSD LSI, external clock input can be selected (For the μPD6461 and μPD6462, this is selected by the mask code option; for the μPD6466, it is selected by the initialization command).

Figure 2-2. Dot Clock Oscillation Equivalent Circuit

(a) When LC oscillation is selected



(b) When external clock input is selected (μPD6461, μPD6462, or μPD6466)



Remark When LC oscillation is ON, the dot clock oscillation circuit is controlled as follows by the timing generator while $\overline{\text{Hsync}}$ is low.

When display is ON : Dot clock oscillation stopped

When display is OFF : Dot clock oscillation

The dot clock frequency (fosc) when LC oscillation is ON can be calculated using the following formulas.

$$fosc = \frac{1}{(2\pi\sqrt{LC})} \text{ [Hz]}$$

$$C = \frac{C_{in} \bullet C_{out}}{(C_{in} + C_{out})} \text{ [F]}$$

By setting L = 33 μH, C_{in} = 5 to 30 pF (trimmer capacitor), and C_{out} = 30 pF, the circuit can be used in the LC oscillation frequency range (fosc = 6 to 8 MHz) recommended by NEC for operation.

The actual circuit will have a lower frequency than the calculated value due to effects such as the stray capacitance of the pins or delay within the LSI.

2.1.2 Timing generator

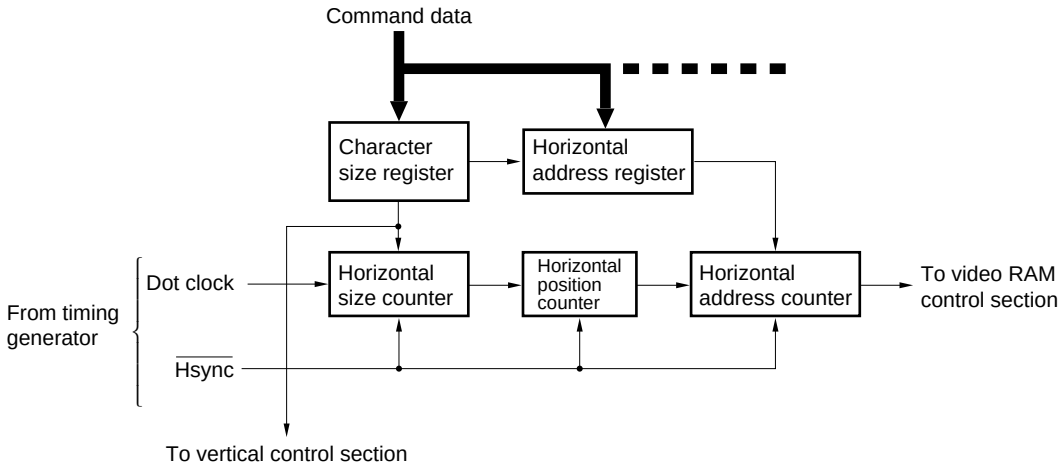
The timing generator generates various types of timing signals according to horizontal/vertical synchronization signals input from the dot clock oscillation circuit, synchronization separation circuit, synchronization signal generator (video-system OSD LSI) or synchronization protection circuit (RGB-system OSD LSI) commands from the microcontroller (such as LC oscillation ON/OFF, crystal oscillation ON/OFF, or display ON/OFF, etc.).

2.1.3 Horizontal control section

The horizontal display start position of a character is determined by counting dot clocks from the rising edge of the horizontal synchronization signal ($\overline{\text{Hsync}}$). The character is displayed at the position corresponding to this horizontal display start position and the specified video RAM column address.

Each block reset is synchronized with $\overline{\text{Hsync}}$. If $\overline{\text{Hsync}}$ is not supplied within the OSD LSI, the character is not displayed correctly, since no reset occurs.

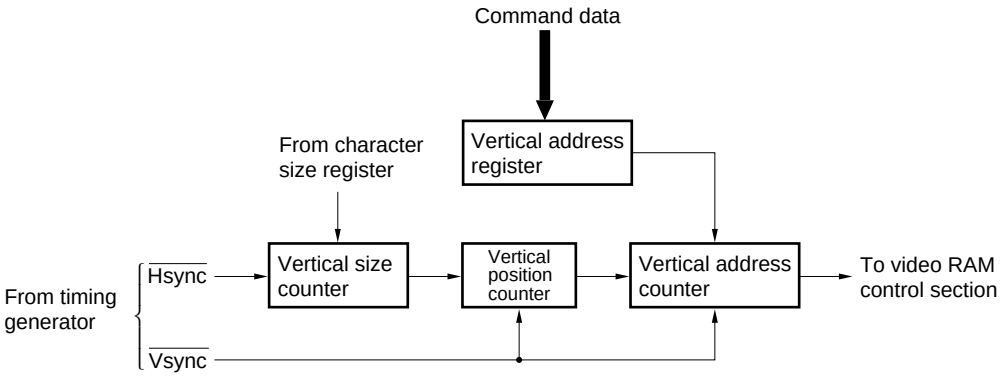
Figure 2-3. Horizontal Control Section



2.1.4 Vertical control section

The vertical display start position of a character is determined by counting rising edges of the horizontal synchronization signal ($\overline{\text{Hsync}}$) from the rising edge of the vertical synchronization signal ($\overline{\text{Vsync}}$). The character is displayed at the position corresponding to this vertical display start position and the specified video RAM line address. The character type to be displayed is set by the character generator ROM line address control.

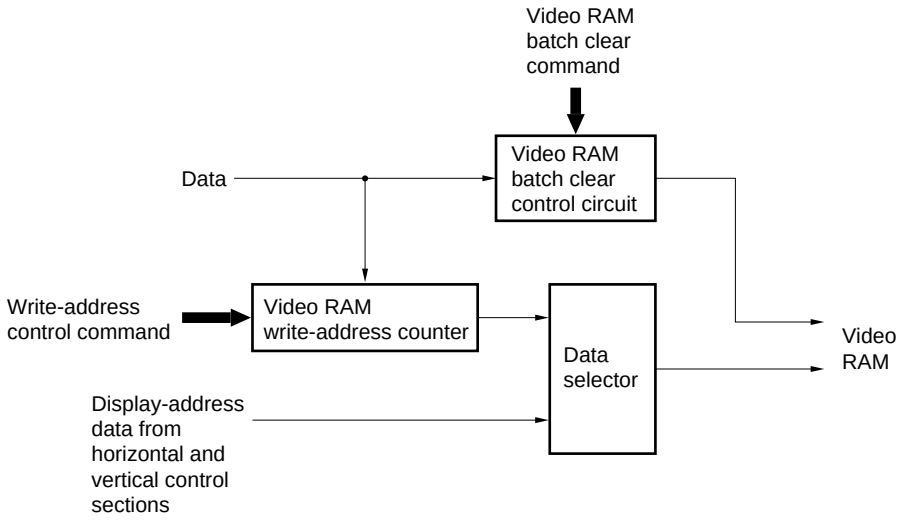
Figure 2-4. Vertical Control Section



2.1.5 Video RAM control section

The video RAM control section controls video RAM addresses. When a video RAM batch clear command is executed, the Display Off Code is written to all addresses (288 words) of video RAM.

Figure 2-5. Video RAM Control Section



2.1.6 Video RAM

The video RAM maintains data set in character units corresponding to a 12 line by 24 column display area.

2.1.7 Character generator ROM

The character generator ROM stores a character font. The number of characters is determined by the ROM capacity. The character generator ROM for a video-system OSD LSI can have a capacity of 128 characters (μPD6464A) or 256 characters (μPD6465). For an RGB-system OSD LSI, can have a capacity of 128 characters (μPD6462), 256 characters (μPD6461), or 512 characters (μPD6466).

2.1.8 Output controller

The output controller controls the display of characters, backgrounds, and other output.

2.2 Basic Operation of a Video-System OSD LSI

This section describes the basic operation of the circuits of a video-system OSD LSI (μPD6464A or μPD6465).

2.2.1 Quadruple/4fsc crystal oscillation circuit

Figure 2-6 shows a block diagram of a quadruple/4fsc crystal oscillation circuit.

With the μPD6464A or μPD6465, quadruple oscillation or 4fsc crystal oscillation is selected according to the externally connected circuit and oscillation mode control command. Since the 4fsc signal generated by the oscillation circuit is used as the reference clock for synchronization signal generation when internal video signal mode is set and the fsc signal is used as the reference clock for internal video signal generation and for synchronization separation in the synchronization separation circuit, a crystal oscillation control command must be used to set crystal oscillation to ON when generating characters.

The operation of this circuit when each mode is selected is explained below.

(1) When quadruple oscillation is selected

The fsc signal must be input from the FSCI pin (pin 9) (see **Figure 3-1 Sample μPD6464A or μPD6465 Application Circuit (When Quadruple Oscillation Is Selected)**). The 4fsc signal is generated by an externally connected LC oscillator and internal circuits of the μPD6464A or μPD6465. Also, the phase of the signal obtained by dividing the 4fsc signal generated by LC oscillation into 4 parts is compared with the phase of the fsc signal input to the FSCI pin, and the phase differential is converted to a voltage value and output from the FSCO pin (pin 10). A 4fsc signal that is synchronized with the external fsc signal is generated by varying the varactor diode capacitance according to this voltage.

Selecting this mode reduces the crystal oscillator and enables the installation area and cost to be reduced.

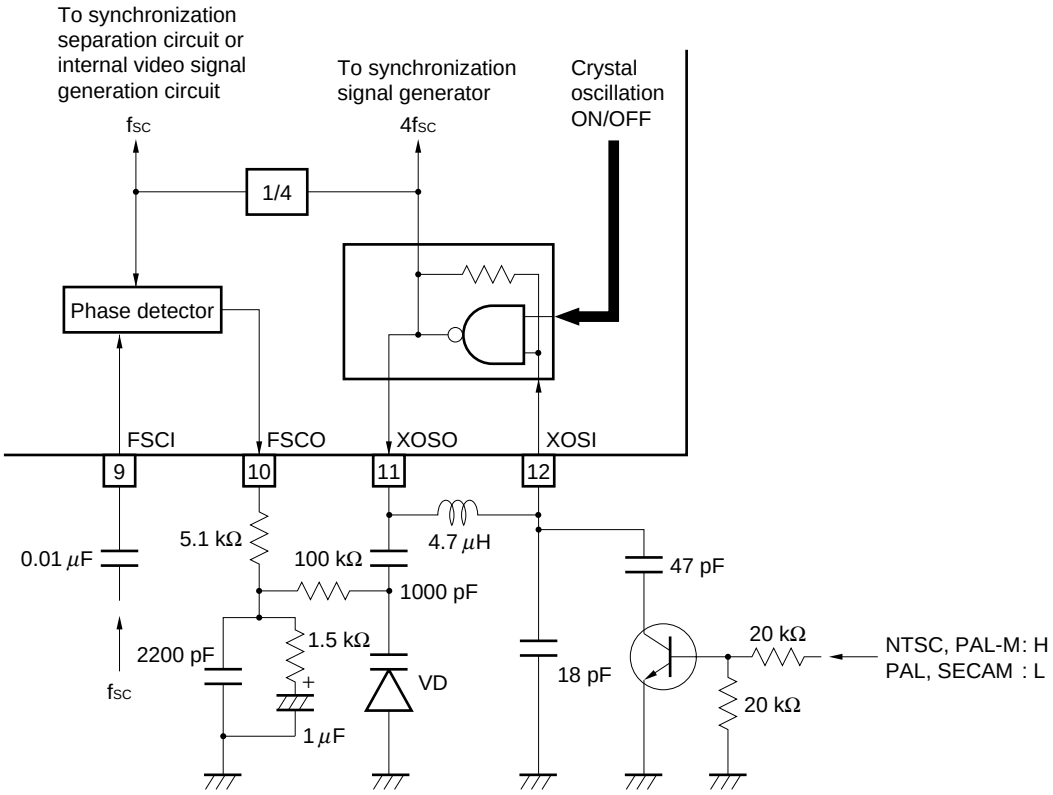
(2) When 4fsc crystal oscillation is selected

Connect a crystal resonator (frequency: 4fsc) between the XOSO pin (pin 11) and XOSI pin (pin 12) and connect a capacitor (approx. 30 pF) between the XOSO pin (pin 11) and ground (GND) and connect a trimmer capacitor (5 to 30 pF) between the XOSI pin (pin 12) and ground (GND) (see **Figure 3-2 Sample μPD6464A or μPD6465 Application Circuit (When 4fsc Crystal Oscillation Is Selected)**).

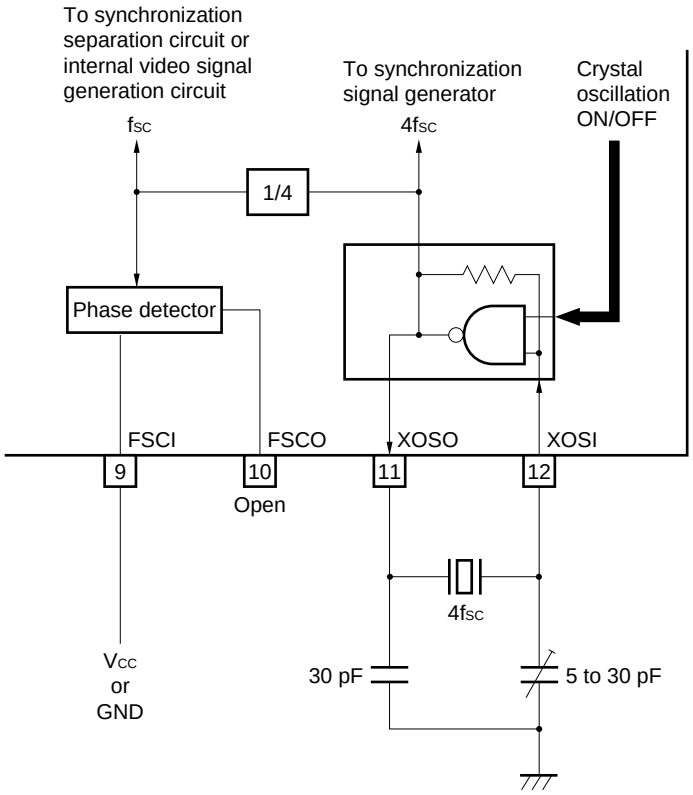
This crystal oscillator generates the 4fsc signal, and the fsc signal is generated by dividing this 4fsc signal into four parts.

Figure 2-6. Quadruple/4fsc Crystal Oscillation Circuit

(a) When quadruple oscillation is selected



(b) When 4fsc crystal oscillation is selected



2.2.2 Synchronization separation circuit

When external video signal mode is selected, the synchronization separation circuit uses the fsc signal generated by the quadruple/4fsc crystal oscillation circuit to separate the horizontal synchronization signal ($\overline{\text{Hsync}}$) and vertical synchronization signal ($\overline{\text{Vsync}}$) from the composite synchronization signal (Csync).

The vertical synchronization signal sampling circuit uses the fsc signal to sample $\overline{\text{Vsync}}$ from Csync by counting down when Csync is high and counting up when it is low.

Also, the horizontal synchronization signal sampling circuit can prevent synchronization signals from being omitted or noise from being generated due to invalid signals because it contains an on-chip horizontal synchronization signal correction ($\overline{\text{Hsync}}$ autogeneration) circuit.

When internal video signal mode is selected, $\overline{\text{Vsync}}$ and $\overline{\text{Hsync}}$ are generated by the synchronization signal generator by using the 4fsc signal generated by the quadruple/4fsc crystal oscillation circuit section.

The operation of the horizontal synchronization signal correction ($\overline{\text{Hsync}}$ autogeneration) circuit is outlined below (see **Figure 2-8** for sample timing charts).

(1) $\overline{\text{Hsync}}$ width

The μPD6464A recognizes a signal of at least 0.2 μsec as $\overline{\text{Hsync}}$, and the μPD6465 recognizes a signal of at least 0.8 μsec. Signals having smaller widths are ignored.

(2) $\overline{\text{Hsync}}$ cycle

No external signal can be sampled for an interval of 61.2 μsec after $\overline{\text{Hsync}}$ is sampled.

(3) $\overline{\text{Hsync}}$ autogeneration

The $\overline{\text{Hsync}}$ cycle is monitored, and if no external $\overline{\text{Hsync}}$ is input in a 61.2 to 64.5 μsec interval after $\overline{\text{Hsync}}$ is sampled, a pseudo $\overline{\text{Hsync}}$ is autogenerated and output. The sampling of signals is not inhibited after the autogeneration of the pseudo $\overline{\text{Hsync}}$. The external signal that is input next is treated as $\overline{\text{Hsync}}$ to accelerate the move back to the regular $\overline{\text{Hsync}}$ (If the sampling of signals were inhibited after the autogeneration of the pseudo $\overline{\text{Hsync}}$, the auto-generation interval would continue, resulting in a loss of synchronization between the external $\overline{\text{Hsync}}$ and the $\overline{\text{Hsync}}$ used for display inside the OSD LSI).

According to the operation described above, the pseudo $\overline{\text{Hsync}}$ is output even if no external Csync is input. However, no pseudo $\overline{\text{Vsync}}$ is autogenerated.

Figure 2-7. Synchronization Separation Circuit Section

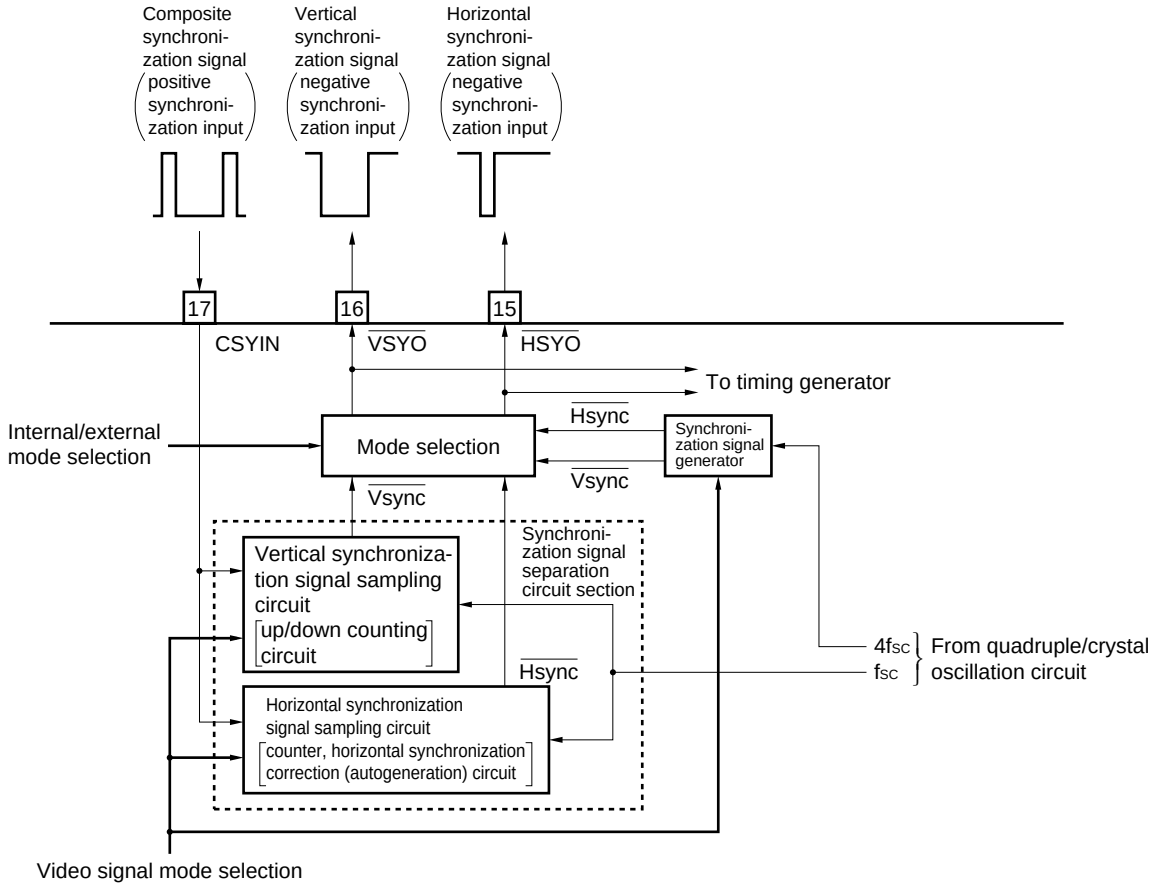
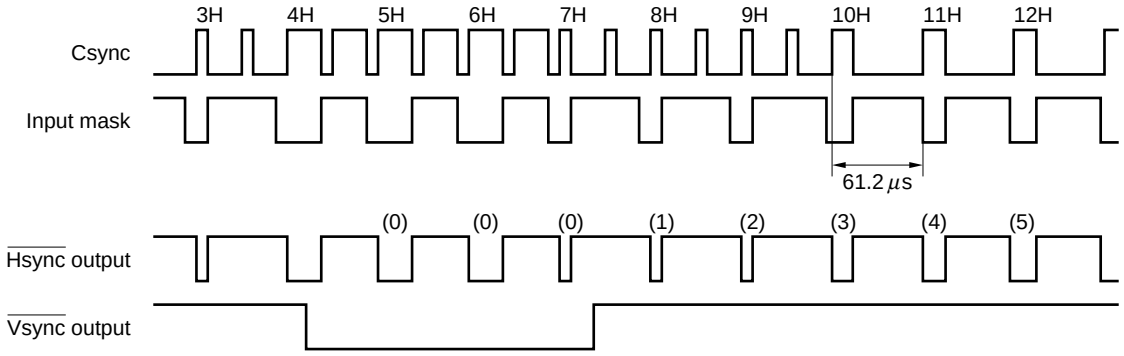


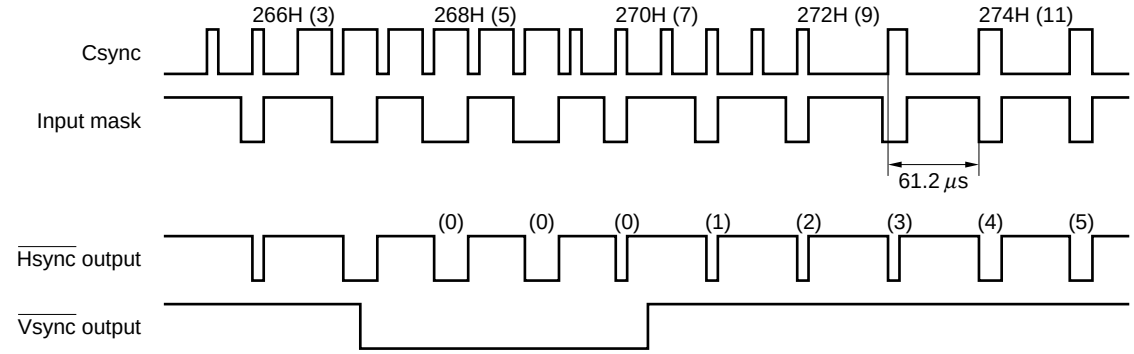
Figure 2-8. Sample Horizontal Synchronization Signal Correction Circuit Timing Charts (1/3)

(a) When regular signals are input

Odd fields



Even fields

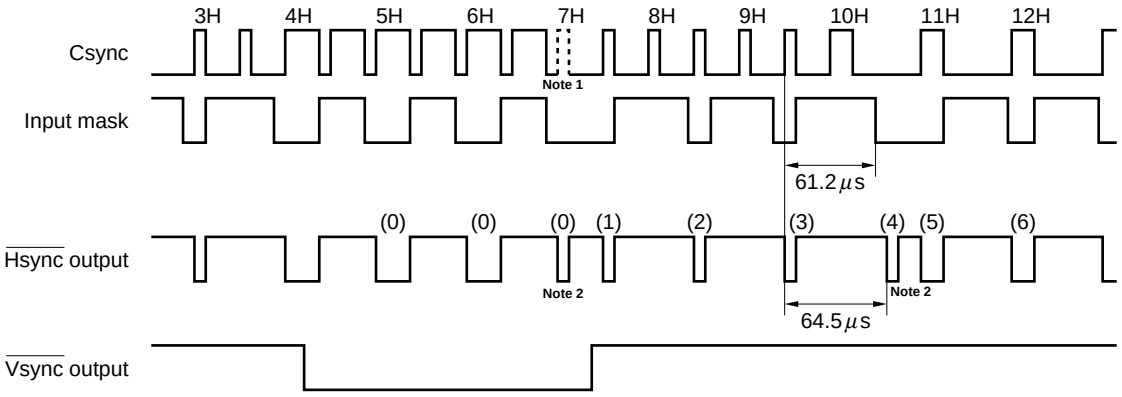


Remark The numbers enclosed in parentheses are vertical display counter values within the μPD6464A or μPD6465.

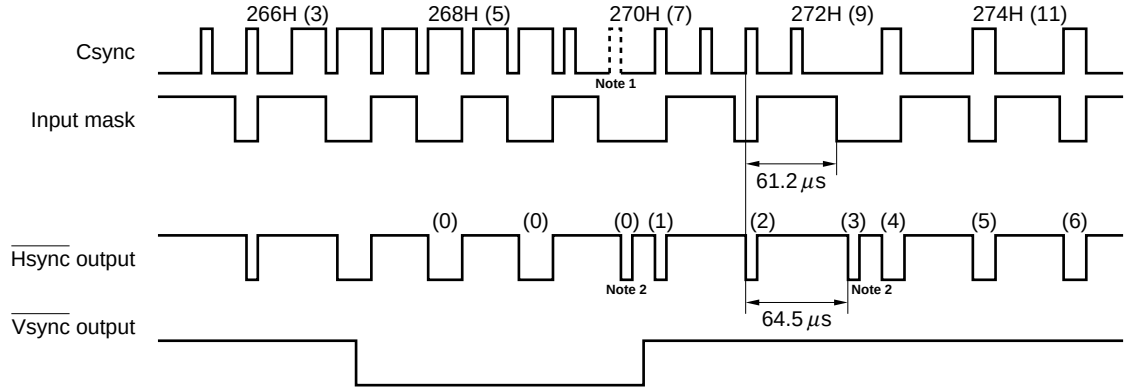
Figure 2-8. Sample Horizontal Synchronization Signal Correction Circuit Timing Charts (2/3)

(b) $\overline{\text{Hsync}}$ autogeneration example

Odd fields



Even fields



Notes 1. Indicates that one pulse within the Csync signal is missing.

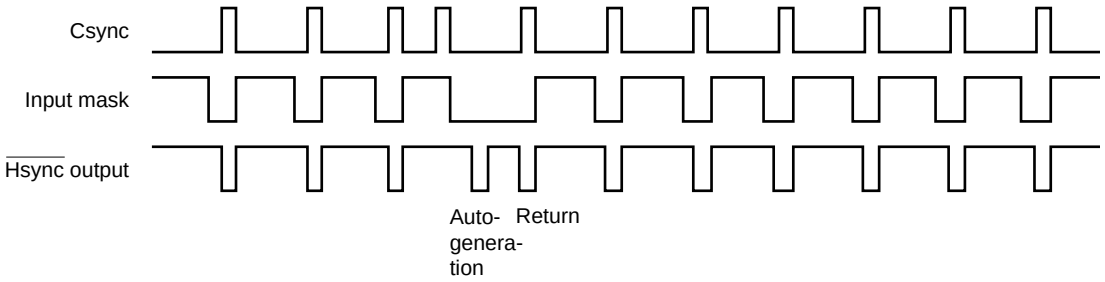
2. This is an autogenerated $\overline{\text{Hsync}}$ signal within the μPD6464A or μPD6465.

Remark The numbers enclosed in parentheses are vertical display counter values within the μPD6464A or μPD6465.

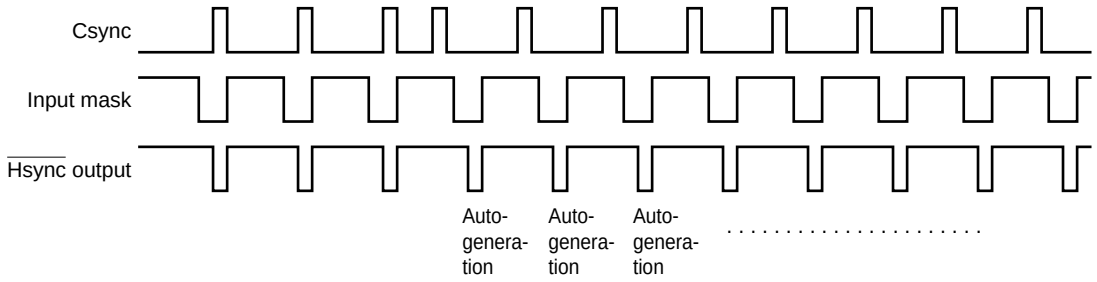
Figure 2-8. Sample Horizontal Synchronization Signal Correction Circuit Timing Charts (3/3)

(c) Change in $\overline{\text{Hsync}}$ output due to input mask after autogeneration

When no masking is performed after autogeneration



when masking is performed after autogeneration



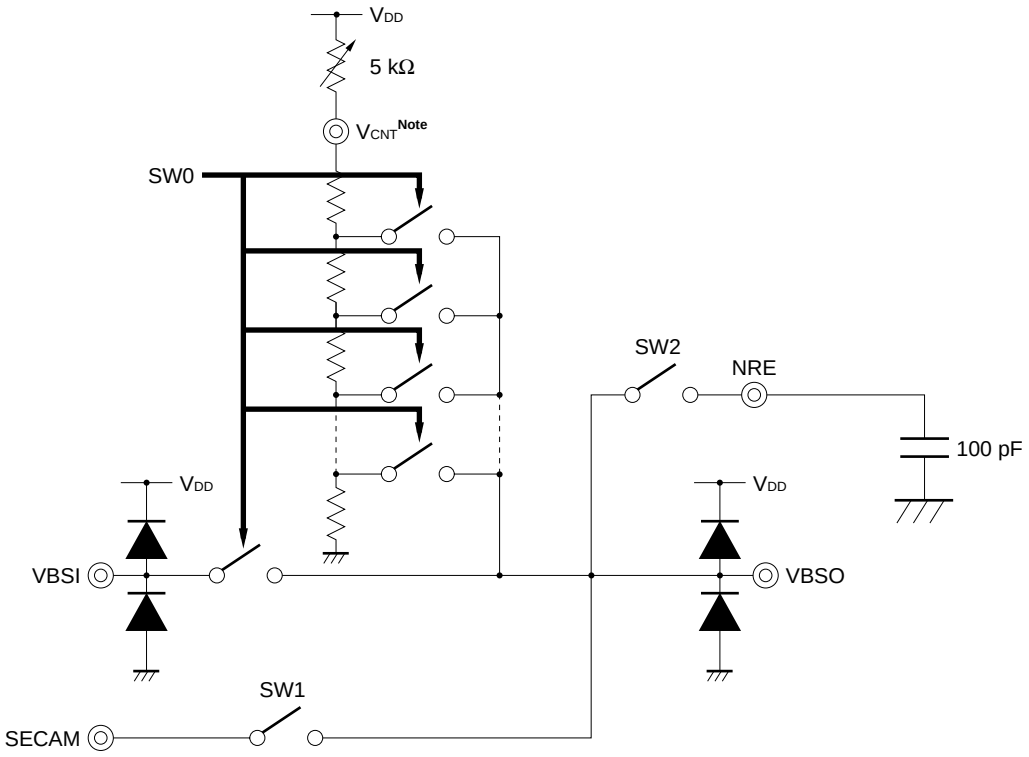
2.2.3 Video signal output section

The video signal output section mixes character information with a video signal input from an external source or with an internally generated video signal and outputs the mixed signal.

With the μPD6464A or μPD6465, set the V_{CNT} pin voltage to 2.5 V to use the internal/external video signal amplitude level at 1 $V_{p\text{-}p}$, and set the V_{CNT} pin voltage to 5 V to use it at 2 $V_{p\text{-}p}$. In addition, the corresponding sync-chip level and pedestal level of the composite video signal input from an external source must match the internal video signal level (see **Table 2-1**). If the video signal amplitude level, sync-chip level, and pedestal level are not matched with the internal/external video signal, the character levels will differ in external video signal mode and internal video signal mode.

For details about the adjustment method, refer to the data sheet.

Figure 2-9. Video Signal Output Section Equivalent Circuit



Note Set the V_{CNT} pin voltage to 5 V when the internal video signal amplitude level is 2 $V_{p\text{-}p}$, and set the voltage to 2.5 V when the amplitude level is 1 $V_{p\text{-}p}$.

Remark The switch operations are as follows.

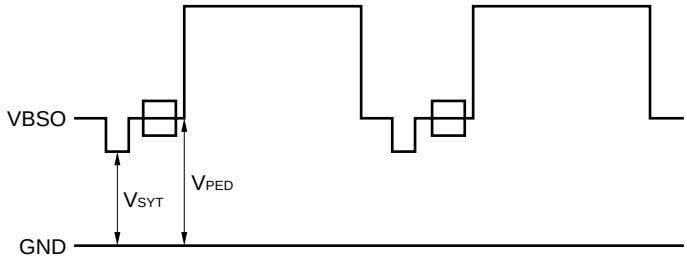
- SW0: Controlled by the output control section according to the character/background level, color burst/color phase (for internal video signal mode), etc.
- SW1: This is ON when the SECAM method is set for the external video signal mode.
- SW2: This is ON during the video signal output interval when internal video signal mode is selected.

Table 2-1. μPD6464A or μPD6465 Internal Video Signal Level

V_{CNT} Pin Voltage	Output Level Control Command	Internal video Signal Amplitude Level	Sync-Chip Level: V_{SYT}	Pedestal Level: V_{PED}
2.5 V	Specifies 1 V_{p-p}	1 V_{p-p}	1 V	1.29 V
5.0 V	Specifies 2 V_{p-p}	2 V_{p-p}	1 V	1.58 V

Remark V_{DD} = 5.0 V

Figure 2-10. V_{SYT} and V_{PED} Levels of Composite Video Signal



2.3 Basic Operation of an RGB-System OSD LSI

This section describes the basic operation of the circuits of an RGB-system OSD LSI (μPD6461, μPD6462, or μPD6466).

2.3.1 Synchronization protection circuit

An OSD LSI determines the vertical display start position of a character by counting rising edges of the horizontal synchronization signal ($\overline{\text{Hsync}}$) from the rising edge of the vertical synchronization signal ($\overline{\text{Vsync}}$).

As shown in Figure 2-11 (a), when the $\overline{\text{Vsync}}$ and $\overline{\text{Hsync}}$ rising edges overlap and $\overline{\text{Vsync}}$ has jitter, the display start position is indefinite depending on whether or not the $\overline{\text{Hsync}}$ rising edge that overlaps $\overline{\text{Vsync}}$ is counted as the first $\overline{\text{Hsync}}$ after the $\overline{\text{Vsync}}$ rising edge.

If a count error occurs, since the display start position shifts 1H, vertical jitter of the display character occurs (the character on the screen shifts in 1H units; see **Figure 2-11 (c)**).

The synchronization protection circuit eliminates $\overline{\text{Hsync}}$ counting errors by autogenerating a pseudo $\overline{\text{Hsync}}$ signal internally so that no vertical jitter of the display character is caused by a shift of the display starting position. This circuit sets certain areas (areas A, B, C, and D[Note] in Figures 2-12 to 2-15) according to the character dot clock after the $\overline{\text{Hsync}}$ rising edge and generates a pseudo $\overline{\text{Hsync}}$ signal to prevent vertical jitter corresponding to the $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ signals input within their range. By counting the pseudo $\overline{\text{Hsync}}$ signal, display output is performed with no vertical jitter (the circuit operates so that the $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ status is always kept fixed).

Note The area widths in the μPD6461, μPD6462, or μPD6466 are as follows.

Area A width: $\overline{\text{Hsync}}$ width + 12/fosc (μPD6461 or μPD6462)

With the μPD6466, the area A width is as follows according to the horizontal display start position.

- $\overline{\text{Hsync}}$ width + 7/fosc (horizontal display start position = 28 + 12n: n = 0,1,2,…)
- $\overline{\text{Hsync}}$ width + 10/fosc (horizontal display start position = 25 + 12n: n = 0,1,2,…)
- $\overline{\text{Hsync}}$ width + 13/fosc (horizontal display start position = 22 + 12n: n = 0,1,2,…)
- $\overline{\text{Hsync}}$ width + 16/fosc (horizontal display start position = 31 + 12n: n = 0,1,2,…)

Area B width: 48/fosc

Area C width: 12/fosc

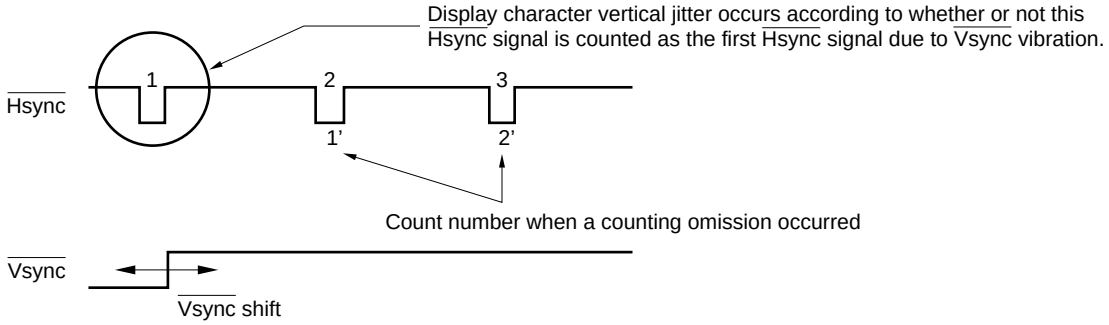
Area D width: Other than areas A, B, and C

fosc: Dot clock frequency

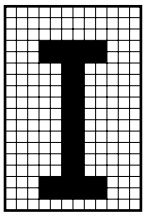
The synchronization protection circuit operates as described below.

Figure 2-11. Display Character Vertical Jitter Generation Mechanism

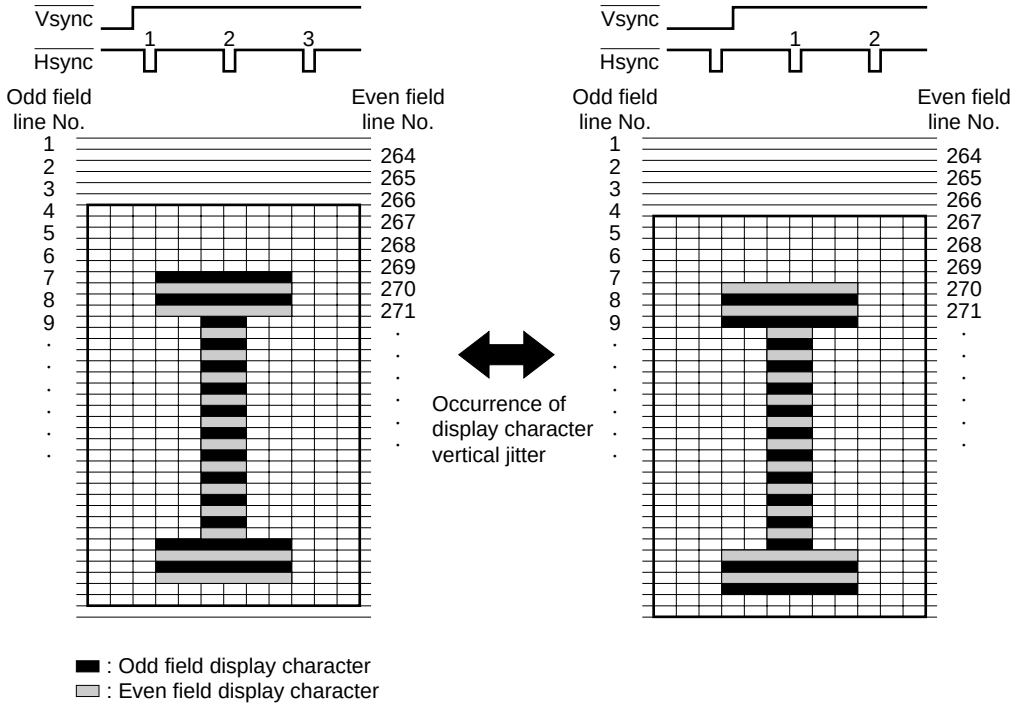
(a) Relationship between $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ when vertical jitter occurs



(b) Character pattern



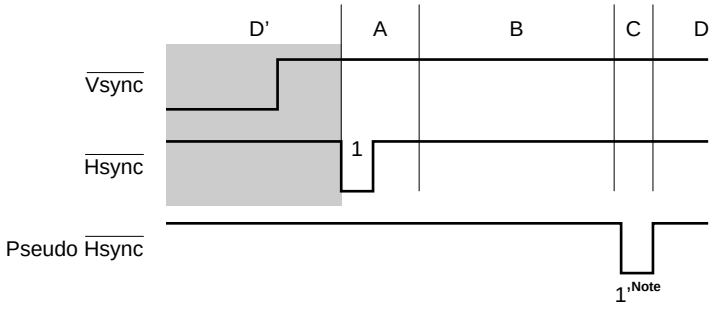
(c) Display character vertical jitter generation model (when the count error occurs at the first of an odd field)



Remark If $\overline{\text{Vsync}}$ shifts in the vicinity of the $\overline{\text{Hsync}}$ rising edge, display character vertical jitter occurs according to whether or not the first $\overline{\text{Hsync}}$ signal of the odd fields is counted as the first signal.

(1) Mode 1

Figure 2-12. Synchronization Protection Circuit Operation (Mode 1)

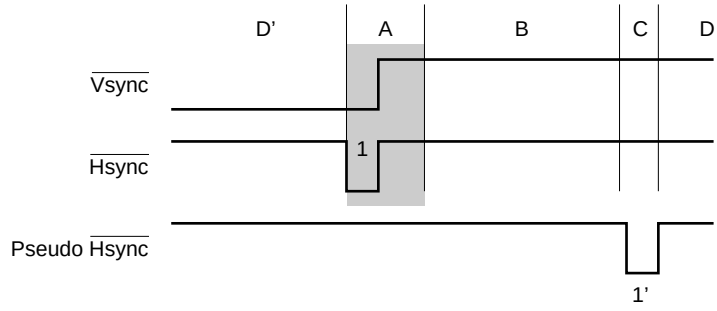


Note This is output only when a pseudo Hsync signal has been output by the previous field.

If the Vsync rising edge is input before the Hsync rising edge (area D'), the count begins with the Hsync(1) rising edge. However, if a pseudo Hsync signal has been output by the previous field, the pseudo Hsync (1') signal is also output by the current field in area C. The count begins with this pseudo Hsync (1') rising edge, and then subsequent Hsync signals are counted.

(2) Mode 2

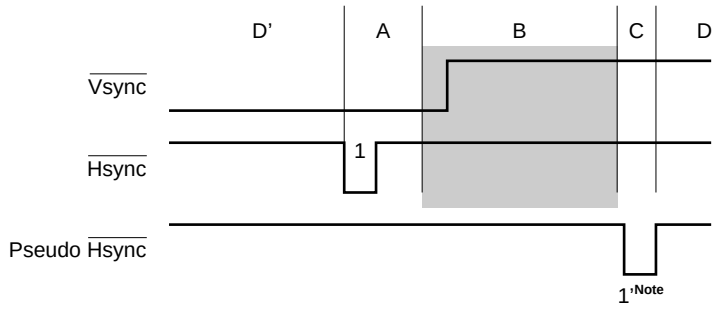
Figure 2-13. Synchronization Protection Circuit Operation (Mode 2)



If a Vsync signal is input in the period (area A) determined by the Hsync Low period and a certain number of dot clocks from Hsync rising edge, a pseudo Hsync (1') signal is output within the internal circuitry of the OSD LSI in area C, the count begins with this rising edge, and then subsequent Hsync signals are counted.

(3) Mode 3

Figure 2-14. Synchronization Protection Circuit Operation (Mode 3)

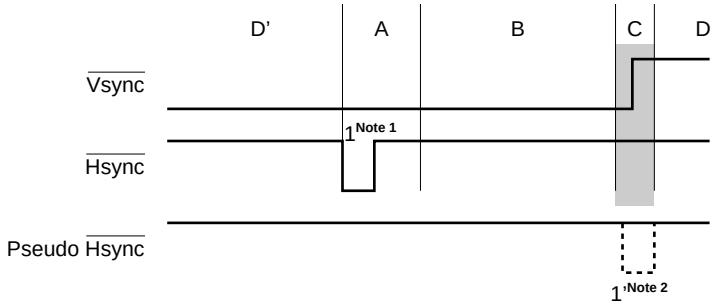


Note This is output only when a pseudo Hsync signal has been output by the previous field.

When the Vsync rising edge is input in area B, if a pseudo Hsync signal has been output by the previous field, the pseudo Hsync(1') signal is also output by this field in area C. The count begins with this pseudo Hsync (1') rising edge, and then subsequent Hsync signals are counted.
However, if a pseudo Hsync signal has not been output by the previous field, no pseudo Hsync signal is output by this field, and the count begins with the next Hsync rising edge that was input.

(4) Mode 4

Figure 2-15. Synchronization Protection Circuit Operation (Mode 4)

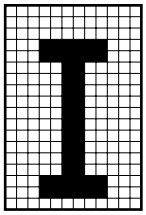


Notes 1. This is not counted. The count begins with the next Hsync.
2. No pseudo Hsync signal is output regardless of the status in the previous field.

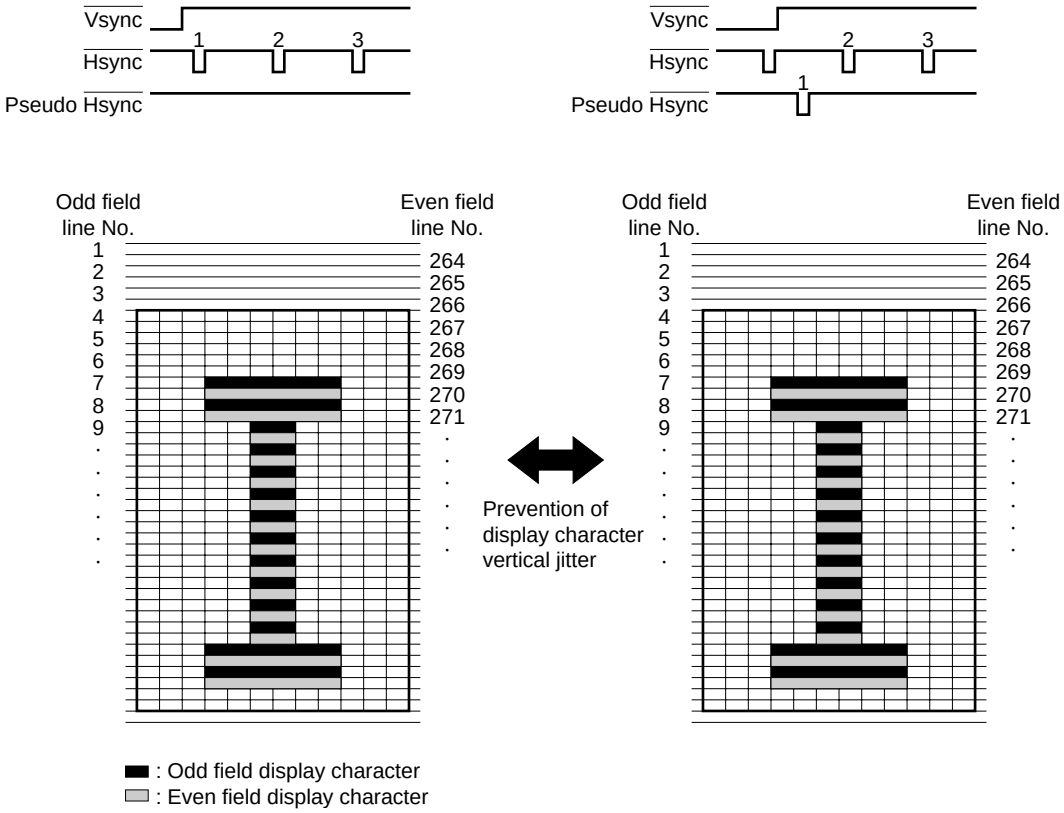
When the Vsync rising edge is input in area C, the pseudo Hsync(1') signal is not output regardless of the status in the previous field, and the count begins with the Hsync rising edge that was input next.

Figure 2-16. Display Character Vertical Jitter Prevention Mechanism

(a) Character pattern



(b) Display character vertical jitter prevention model
(when the $\overline{\text{Vsync}}$ shift occurs at the first of an odd field)

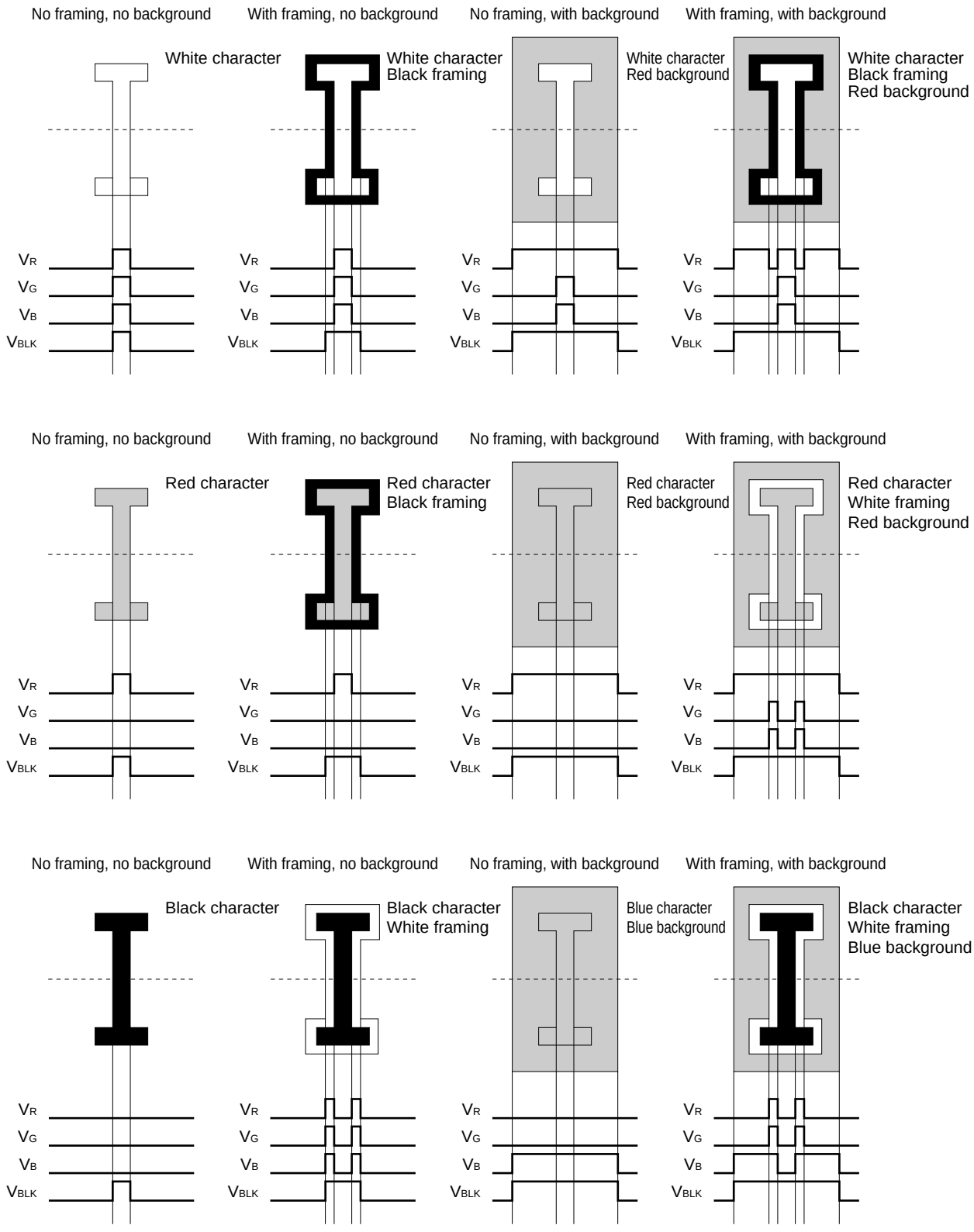


Remark Even if $\overline{\text{Vsync}}$ shifts in the vicinity of the $\overline{\text{Hsync}}$ rising edge, the pseudo $\overline{\text{Hsync}}$ signal is generated by the action of the synchronization protection circuit, and no display character vertical jitter occurs.

2.3.2 R, G, B, and BLK outputs when RGB + V_{C1} + V_{C2} is selected

Figure 2-17 shows the relationships among the R, G, B, and BLK outputs when the mask option (for the μPD6461 or μPD6462) or initialization command (for the μPD6466) is used to set the output pins to RGB + V_{C1} + V_{C2} mode.

Figure 2-17. Output Pins: Sample R, G, B, and BLK Output Images When RGB + V_{C1} + V_{C2} Is Selected

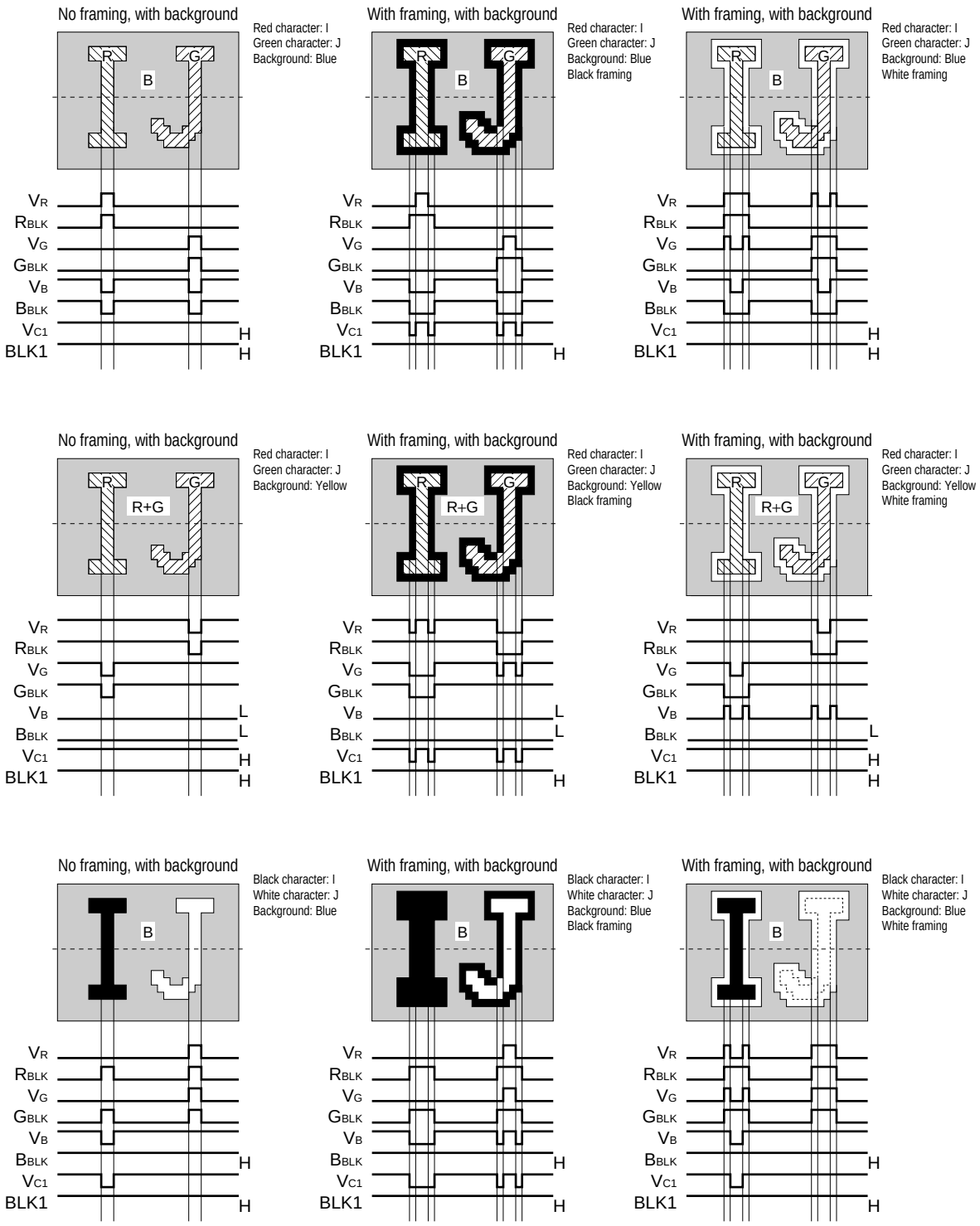


Remark The waveform of each output pin represents the output on the dashed line (horizontal) in the middle of the character.

2.3.3 R, G, B, and BLK outputs when RGB + blanking corresponding to RGB (3BLK) is selected

Figure 2-18 shows the relationships among the R, G, B, and BLK outputs when the mask option (for the μPD6461 or μPD6462) or initialization command (for the μPD6466) is used to set the output pins to RGB + 3BLK mode.

Figure 2-18. Sample R, G, B, and BLK Output Images When RGB + 3BLK Is Selected



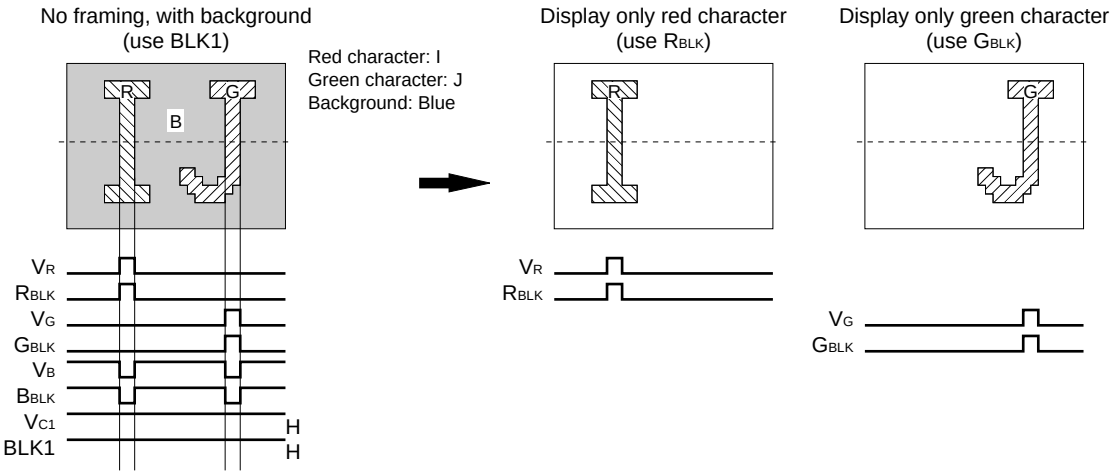
Remarks 1. The waveform of each output pin represents the output on the dashed line (horizontal) in the middle of the character.

2. V_{C1} is the logical sum of V_R, V_G, and V_B, and BLK1 is the logical sum of R_{BLK}, G_{BLK}, and B_{BLK}.

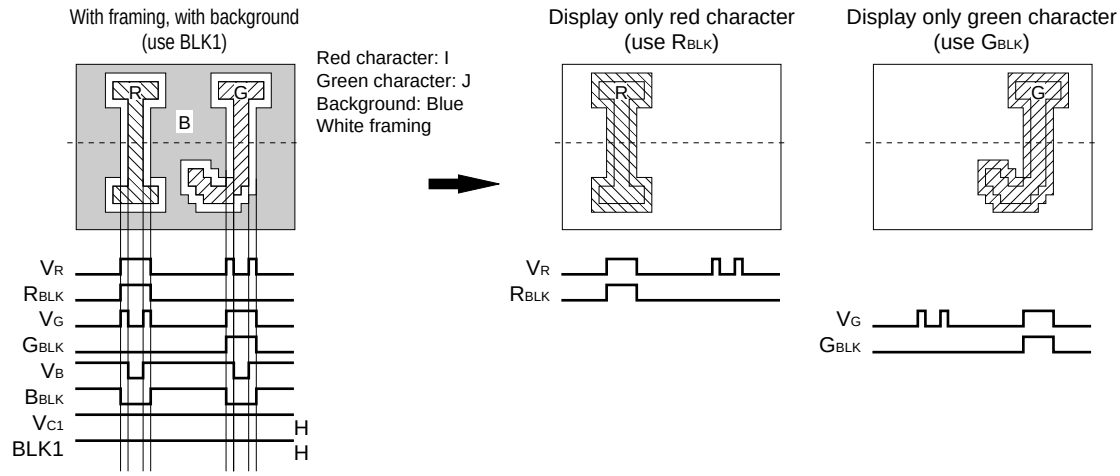
To provide the same image data to two screens and simultaneously display different characters for each of them (such as displaying only red characters on the viewfinder in a camcorder and transcribing only green characters onto the video tape), use blanking signals corresponding to RGB as shown in Figure 2-19 (a). By using blanking signals corresponding to RGB even when white framing is set, you can display only single-color characters. However, the colors of the character portion and framing portion are identical as shown in Figure 2-19 (b).

Figure 2-19. Sample Use of Blanking Signals Corresponding to RGB

(a) When no framing is set



(b) When white framing is set



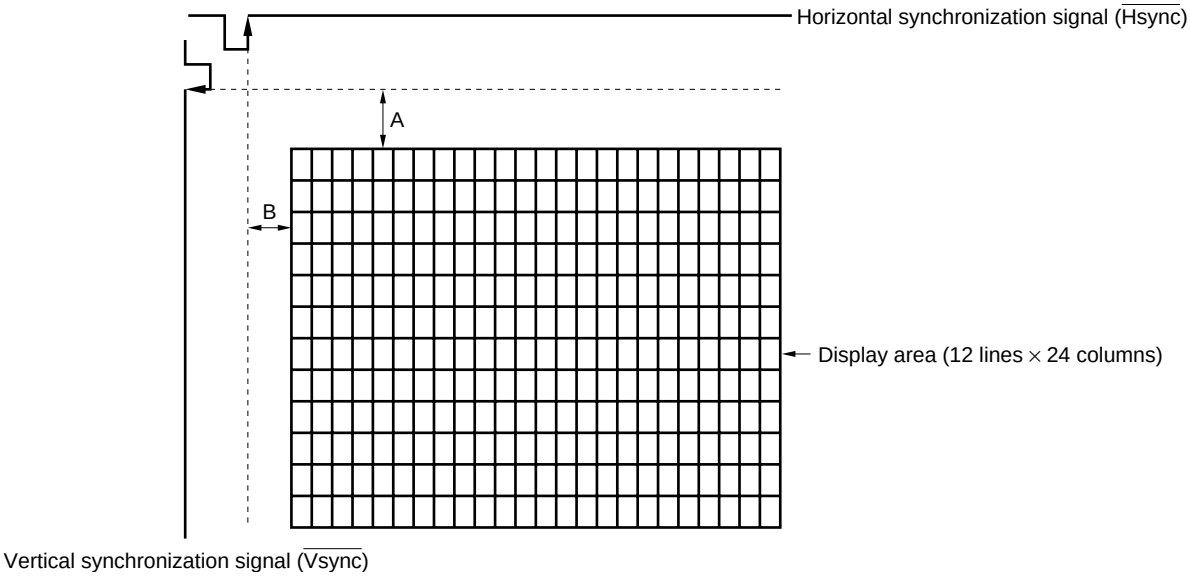
2.4 Characters

2.4.1 Character display

An OSD LSI displays the character generator ROM contents in a 12-line by 24-column display area. Figure 2-20 shows an image of the display area.

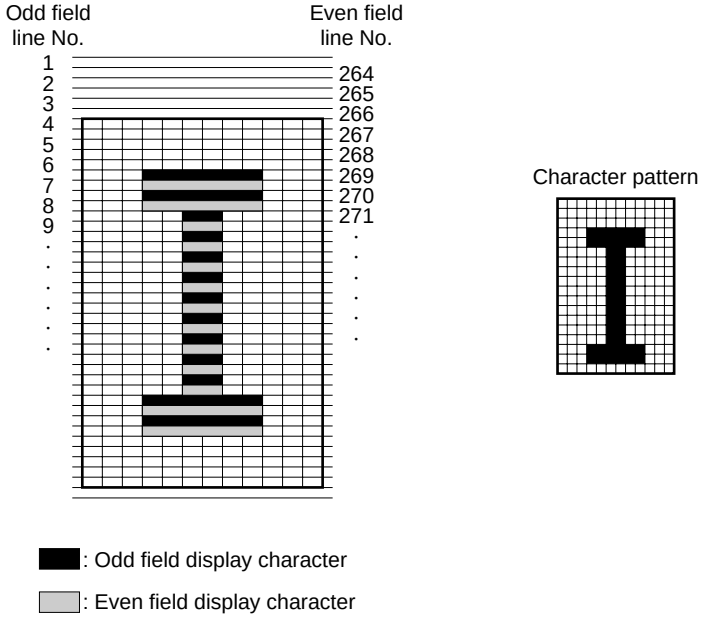
Figure 2-20. Character Display

(a) Character position control



Remark The horizontal display start position (A) and vertical display start position (B) are controlled by the character position control command.

(b) Sample display image when interlace is used (when A = 3H is set)



2.4.2 Character patterns

Characters can be designed by using a character pattern editor (for details, see **CHAPTER 5 DEVELOPMENT TOOLS**) that can be rented from NEC. For inquiries related to character pattern editor rental, contact an NEC distributor or NEC sales representative.

For information about the character patterns of NEC standard products, refer to the data sheet of each product.

2.5 Commands

2.5.1 Command format

OSD LSI control commands are of variable word length in 8-bit units and are input in serial.

Three types of commands are available: 1-byte commands consisting of 8 bits for the instruction and data combined, 2-byte commands, and 2-byte contiguous commands that enable abbreviated input to be performed.

Table 2-2 shows the command data transfer format of each product.

Table 2-2. Command Data Transfer Format

Product Name		Command Data Transfer Format
Video-system	μPD6464A, 6465	MSB first
RGB-system	μPD6461, 6462	MSB first or LSB first can be selected by using mask option
	μPD6466	MSB first or LSB first can be selected by using CMDCT pin

2.5.2 Command list

This section introduces the command tables of each product. For details about commands, refer to the data sheet of each product.

Table 2-3. μPD6464A or μPD6465 Command Tables

1-byte commands

Function	(MSB) D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	0	0	0	1	D0	LC	BL1	BL0
Internal video signal color control	0	0	1	0	R	G	B	0
Background control	0	0	1	1	0	BS1	BS0	0
Internal/external mode control, crystal oscillation control	0	1	0	0	0	E/I	0	XOSC
Video signal method control	0	1	0	0	1	N/P2	N/P1	N/P0
Oscillation method control	0	1	0	1	0	0	Xf_C	0

2-byte commands

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output level control	1	0	0	1	0	0	0	VPD	0	0	0	0	0	1	VC1	VC0
Character size control	1	0	0	1	1	0	0	0	0	S0	0	0	AR3	AR2	AR1	AR0
Test mode[Note]	1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

Note Cannot be used

2-byte contiguous command

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	0	0	0	0	BL	0	C7[Note]	C6	C5	C4	C3	C2	C1	C0

Note Fixed to “0” (μPD6464A)

Table 2-4. μPD6461 or μPD6462 Command Tables (MSB First)

1-byte commands

Function	(MSB) D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Character display control	0	0	0	1	DO	LC	BL1	BL0
Background color/framing color control	0	0	1	0	R	G	B	BFC
3-system independent display ON/OFF	0	1	1	1	0	DOA	DOB	DOC
Character inversion ON/OFF	0	0	1	1	1	0	0	BCRE

2-byte commands

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Character display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output pin control	1	0	0	1	1	1	0	0	V_{C2}	V_{C1}	0	0	AR3	AR2	AR1	AR0
Character size control	1	0	0	1	1	0	0	0	0	S	0	0	AR3	AR2	AR1	AR0
3-system background control	1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC
Test mode[Note]	1	0	1	1	0	0	0	T8	T7	T6	T5	T4	T3	T2	T1	T0

Note Cannot be used

2-byte contiguous command

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	RV	R	G	B	BL	V_{C2}	C7[Note]	C6	C5	C4	C3	C2	C1	C0

Note With the μPD6462, character bit 7 is fixed to “Don’t care.”

Table 2-5. μPD6461 or μPD6462 Command Tables (LSB First)

1-byte commands

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7
Video RAM batch clear	0	0	0	0	0	0	0	0
Character display control	BL0	BL1	LC	DO	1	0	0	0
Background color/framing color control	BFC	B	G	R	0	1	0	0
3-system independent display ON/OFF	DOC	DOB	DOA	0	1	1	1	0
Character inversion ON/OFF	BCRE	0	0	1	1	1	0	0

2-byte commands

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Character display position control	V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2
Write address control	AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AC4	AR0	AR1	AR2
Output pin control	0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	V_{C1}	V_{C2}
Character size control	0	0	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	S	0
3-system background control	BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0
Test mode[Note]	T8	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

Note Cannot be used

2-byte contiguous command

(LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Display character control	V_{C2}	BL	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7[Note]

Note With the μPD6462, character bit 7 is fixed to “Don’t care.”

Table 2-6. μPD6466 Command Tables (MSB First)

1-byte commands

Function	(MSB) D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	0	0	0	1	DO	LC	BL1	BL0
Background color/framing color control	0	0	1	0	R	G	B	BFC
3-system independent display ON/OFF	0	1	1	1	0	DOA	DOB	DOC
Character color inversion ON/OFF	0	1	1	1	1	0	0	BCRE
Blue back ON/OFF	0	1	1	1	1	CLR	0	BB
Character address bank switching	0	1	1	1	1	1	1	BC
Output switch control	0	1	0	S3A	S3B	SW4	SW2	SW1

2-byte commands

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Character display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output pin control	1	0	0	1	1	1	0	0	OD1	OD0	0	0	AR3	AR2	AR1	AR0
Character size control	1	0	0	1	1	0	SV1	SV0	SH1	SH0	0	0	AR3	AR2	AR1	AR0
3-system background control	1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC
Initial settings	1	0	1	1	0	1	0	0	0	BR	RS	OP1	OP0	COC	VST	OSC
Test mode[Note]	1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

Note Cannot be used

2-byte contiguous command

Function	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	RV	R	G	B	BL	V_{C2}	C7	C6	C5	C4	C3	C2	C1	C0

Table 2-7. μPD6466 Command Tables (LSB First)

1-byte commands

Function	D0 (LSB)	D1	D2	D3	D4	D5	D6	D7
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	BL0	BL1	LC	DO	1	0	0	0
Background color/framing color control	BFC	B	G	R	0	1	0	0
3-system independent display ON/OFF	DOC	DOB	DOA	0	1	1	1	0
Character color inversion ON/OFF	BCRE	0	0	1	1	1	0	0
Blue back ON/OFF	BB	0	CLR	1	1	1	1	0
Character address bank switching	BC	1	1	1	1	1	1	0
Output switch control	SW1	SW2	SW4	S3B	S3A	0	1	0

2-byte commands

Function	D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Character display position control	V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2
Write address control	AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AC4	AR0	AR1	AR2
Output pin control	0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	OD0	OD1
Character size control	SV0	SV1	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	SH0	SH1
3-system background control	BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0
Initial settings	0	0	1	0	1	1	0	1	OSC	VST	COC	OP0	OP1	RS	BR	0
Test mode[Note]	0	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

Note Cannot be used

2-byte contiguous command

Function	D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Display character control	V_{C2}	BL	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7

2.6 OSD LSI Power-ON Initialization

Because the internal status of the OSD LSI is indefinite on power application, initialize the OSD LSI by making the $\overline{PCL}$ pin low for a fixed interval and executing a power-ON clear operation. When the power-ON clear operation has been performed, the various control register settings are as follows.

- Test mode is cleared.
- All character data of the video RAM (12 lines by 24 columns) are set to Display Off Data.
- Blinking data are set to OFF.
- Video RAM write address is set to line 0, column 0.
- Character size is set to ×1 (standard size) on all lines.
- Display is set to OFF, and LC oscillation is set to ON.
- The line specification set by output pin control is cleared (μPD6461, μPD6462, or μPD6466).
- Initial defaults are set (μPD6466).
- Display ON/OFF setting of each output system is set to OFF (μPD6466).
- No background and no framing are set for all 3 systems (μPD6466).
- Blue back is set to OFF (μPD6466).
- Character address bank is set to the low-order (0) bank (μPD6466).

The time required for the power-ON clear operation can be calculated by using the following expression.

t (time required for power-ON clear) = t_{PCLL} + {video RAM clear time}
= 10 (μs MIN.) + {10 (μs) + 12/fosc (MHz) × 288 [μs]}

fosc (MHz): LC oscillation frequency or external clock frequency

Remarks 1. Do not input a command during execution of the power-ON clear operation.

2. A dot clock is required to clear video RAM. When external clock input is selected, input a dot clock from the OSC_{IN} pin before executing the power-ON clear or video RAM batch clear operation.

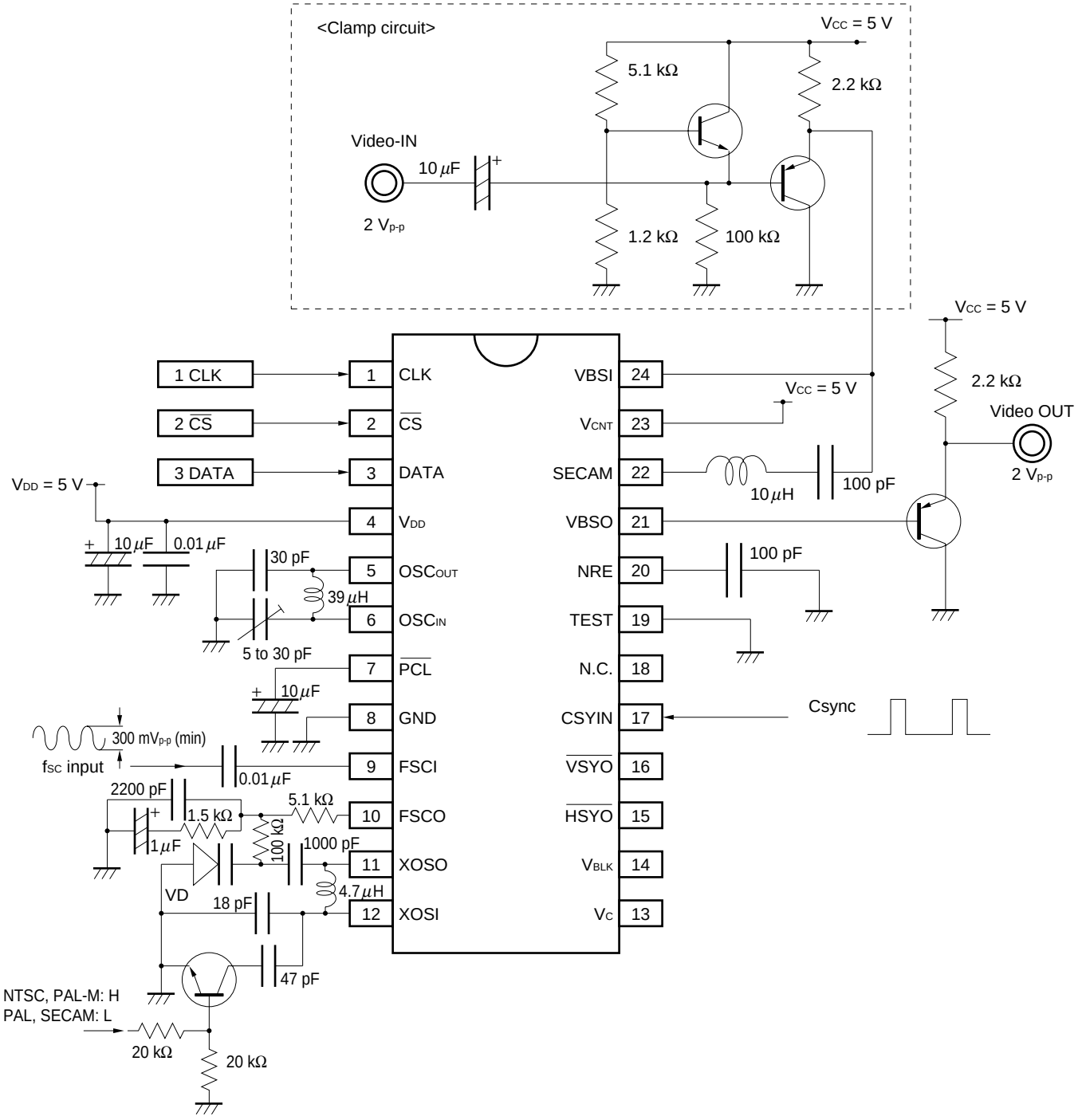
3. The power-ON clear operation, which is a hardware reset due to a signal input to the $\overline{PCL}$ pin, performs initialization that includes video RAM clear and test mode clear operations. In contrast, the video RAM batch clear operation, which is a software reset that performs initialization according to a command (software), does not execute a test mode clear operation.

CHAPTER 3 APPLICATION EXAMPLES

3.1 Video-System OSD LSI Application Examples

3.1.1 Sample μPD6464A or μPD6465 application circuits

Figure 3-1. Sample μPD6464A or μPD6465 Application Circuit (When Quadruple Oscillation Is Selected)



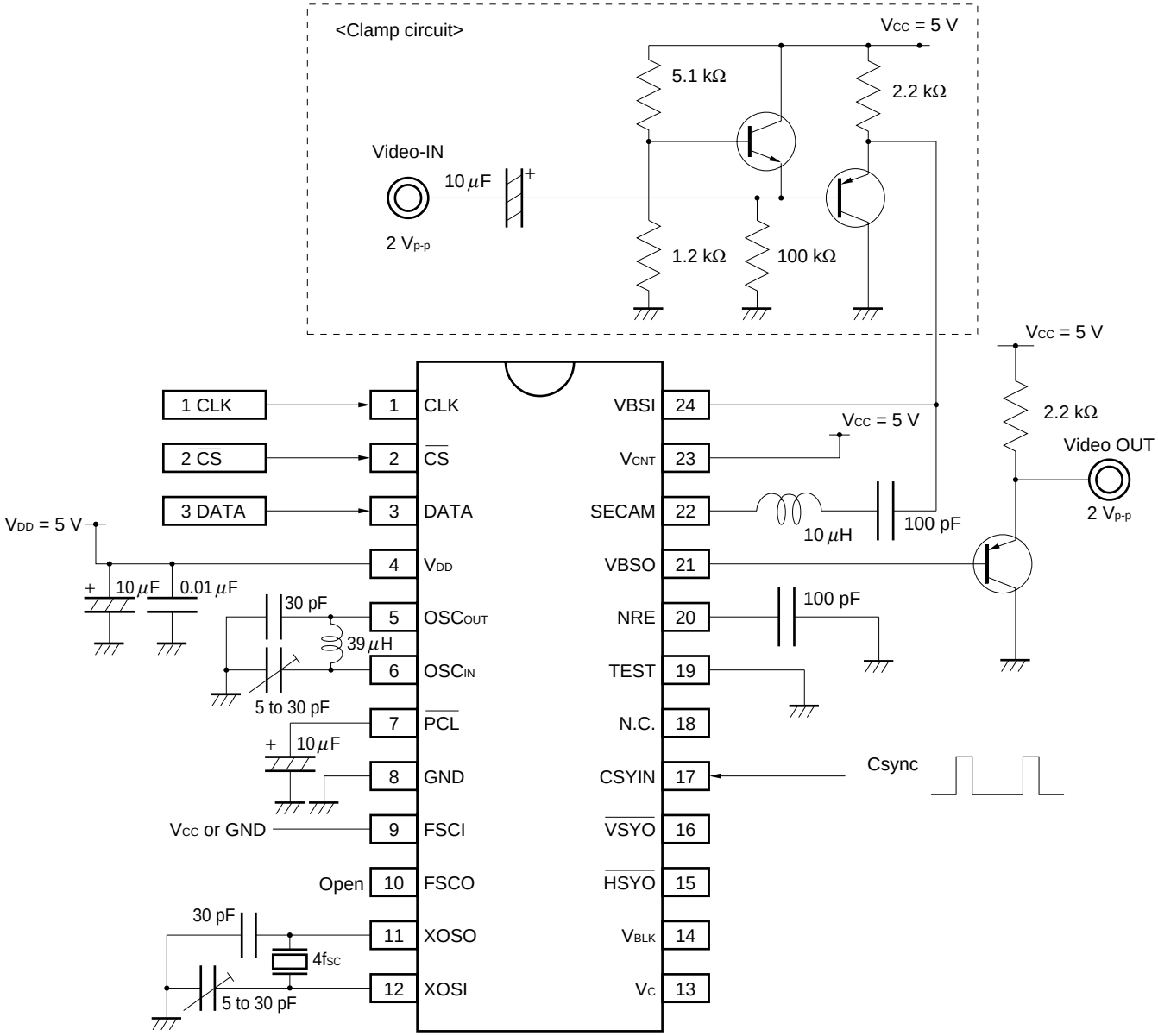
Cautions 1. The clamp circuit is not necessary when the sync-chip level (1 V DC) can be directly input to pin 24.

2. Pin 20 is connected so as to reject unwanted radiation.

3. This application circuit is assumed to input 2-V_{p-p} video signals.

4. A product equivalent to 1SV163 can be used as a VD (varactor diode).

Figure 3-2. Sample μPD6464A or μPD6465 Application Circuit (When 4fsc Crystal Oscillation Is Selected)



Cautions 1. The clamp circuit is not necessary when the sync-chip level (1 V DC) can be directly input to pin 24.

2. Pin 20 is connected so as to reject unwanted radiation.

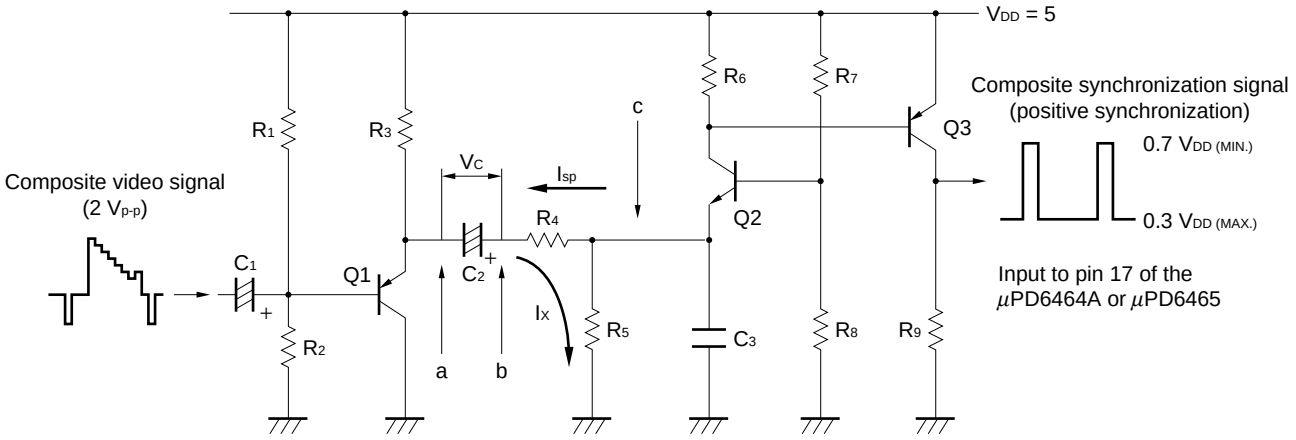
3. This application circuit is assumed to input 2-V_{p-p} video signals.

4. Connect pin 9 to GND or V_{CC} (it cannot be left open). Leave pin 10 open.

3.1.2 Composite synchronization signal (Csync) separation circuit

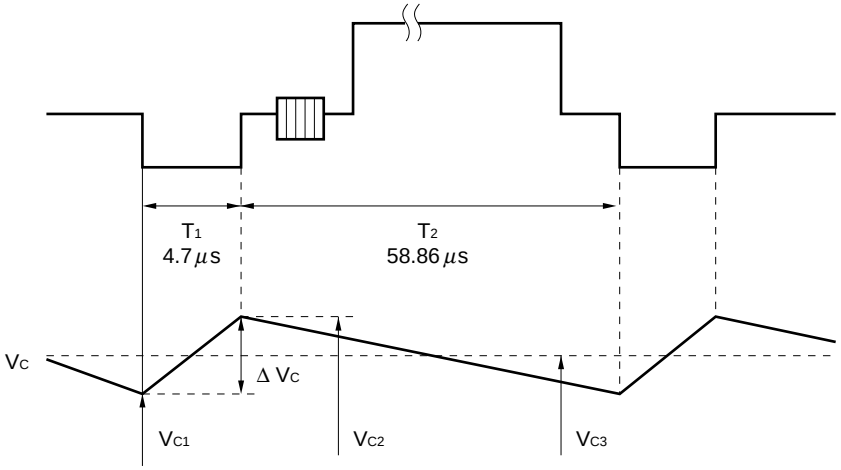
Figure 3-3. Composite synchronization signal separation circuit

(a) Sample composite synchronization signal separation circuit



R_1 = 5.1 kΩ, R_2 = 1.2 kΩ, R_3 = 1 kΩ, R_4 = 220 Ω, R_5 = 100 kΩ, R_6 = 10 kΩ, R_7 = 1 kΩ, R_8 = 2.2 kΩ, R_9 = 10 kΩ, C_1 = 10 μF, C_2 = 1 μF, C_3 = 1000 pF

(b) Composite signal separation waveform image



The operation of the circuit shown in Figure 3-3 and the method of determining the slice level are described below. The voltages at points a, b, and c in Figure 3-3 (a) are given as follows.

$a = V_L$, $b = V_L + V_C$, $c = V_H$

Remark V_L: Sync-chip voltage at point a
V_H: Threshold voltage of Q2

Let $R_5 >> R_4$ and let C_2 be sufficiently large. Then from the relationship $V = \frac{1}{c}\int idt$, the values of ΔV_C when the capacitor is charged and discharged are as follows.

When charged: $\Delta V_C = \frac{V_H - (V_L + V_{C1})}{R_4} \times T_1 \times \frac{1}{C_2}$

When discharged: $\Delta V_C = \frac{V_L + V_{C2}}{R_5} \times T_2 \times \frac{1}{C_2}$

V_C is stabilized at a location where the values of ΔV_C when the capacitor is charged and discharged are the same (let the average voltage of $V_C = V_{C3}$). From a macro viewpoint, the synchronization base is clamped at V_{C3}, and the comparison is performed at the Q2 threshold voltage (V_H). Therefore, the slice level V_S is as follows.

$V_S = V_H - (V_{C3} + V_L)$

Letting the values of ΔV_C be equal here ($V_{C1} \cong V_{C2} \cong V_{C1}$) gives the following equation.

$$\frac{V_H - (V_L + V_{C1})}{R_4} \times T_1 = \frac{V_L + V_{C2}}{R_5} \times T_2$$

Substituting $V_S = V_H - (V_L + V_{C3})$ and eliminating common terms gives the following equation.

$$V_S \left(\frac{1}{R_4} + \frac{T_2}{R_5 T_1} \right) = \frac{V_H}{R_5} \times \frac{T_2}{T_1}$$

Letting $\frac{1}{R_4} >> \frac{T_2}{R_5 T_1}$ here gives the following equation.

$$V_S = V_H \times \frac{R_4}{R_5} \times \frac{T_2}{T_1}$$

In Figure 3-3, since $V_H = 2.7$ V, $R_4 = 220\ \Omega$, $R_5 = 100$ kΩ, since $T_1 = 4.7\ \mu$s and $T_2 = 58.86\ \mu$s, the slice level V_S is as follows.

$$V_S = 2.7 \times \frac{220}{100000} \times \frac{58.86}{4.7}$$

$\cong 74$ mV

Making V_S small is advantageous for horizontal synchronization separation, but disadvantageous for vertical synchronization separation. Conversely, making V_S large causes synchronization aberrations (jitter) due to noise in horizontal synchronization separation. Therefore, the constants must be optimized depending on the signal that is input.

Although a sufficiently large value is selected for the C_2 capacitance value compared with the charge/discharge current, if it is set too large, the transient response characteristic worsens, and it will not be able to follow a sudden APL fluctuation of the input signal.

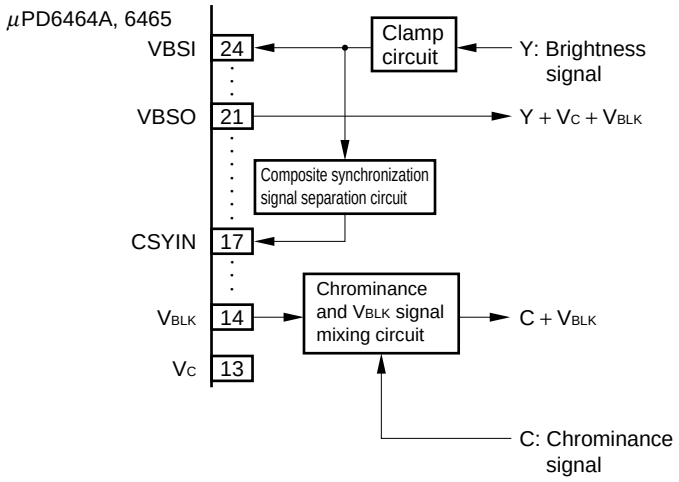
In the circuit shown in Figure 3-3 (a), the input is set to a capacitor combination to simplify measurement. As a result, it is weak relative to APL fluctuation. Therefore, when the circuit is actually configured, using a sync-chip clamp circuit to establish the electric potential of the leading edge of synchronization before inputting it to Q1 in Figure 3-3 (a) makes it strong relative to APL fluctuation.

Caution With the circuit shown in Figure 3-3, the $\overline{\text{Hsync}}$ synchronization signal width after composite synchronization signal separation may be large compared with the input signal due to the circuit configuration. As a result, when calculating the command continuous input enable times according to the formulas shown in the Data Sheet for each product, the $\overline{\text{Hsync}}$ synchronization signal width after composite synchronization signal separation in the circuit shown in Figure 3-3 must be used for the $\overline{\text{Hsync}}$ synchronization signal width (t_{HWL1} or t_{HWL2}).

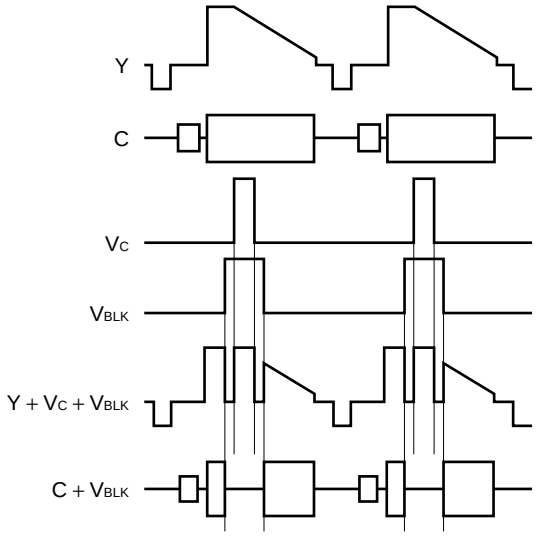
3.1.3 Sample application for separate video signal input

Figure 3-4. Sample Application Circuit for Separate Video Signal Input

(a) Sample application circuit



(b) Pin waveform models



3.1.4 Sample application for NTSC direct mode

For NTSC mode, using the command shown in Table 3-1 sets and clears NTSC direct mode. When NTSC direct mode is used, the IC can be used only with fsc input.

When NTSC direct mode is not used (or is cleared), the IC is in normal mode (quadruple/crystal oscillation).

Figure 3-5 shows a sample application circuit when this command is used. The usage method shown here is a reference example only and is not recommended by NEC.

Table 3-1. NTSC Direct Mode Setting Command

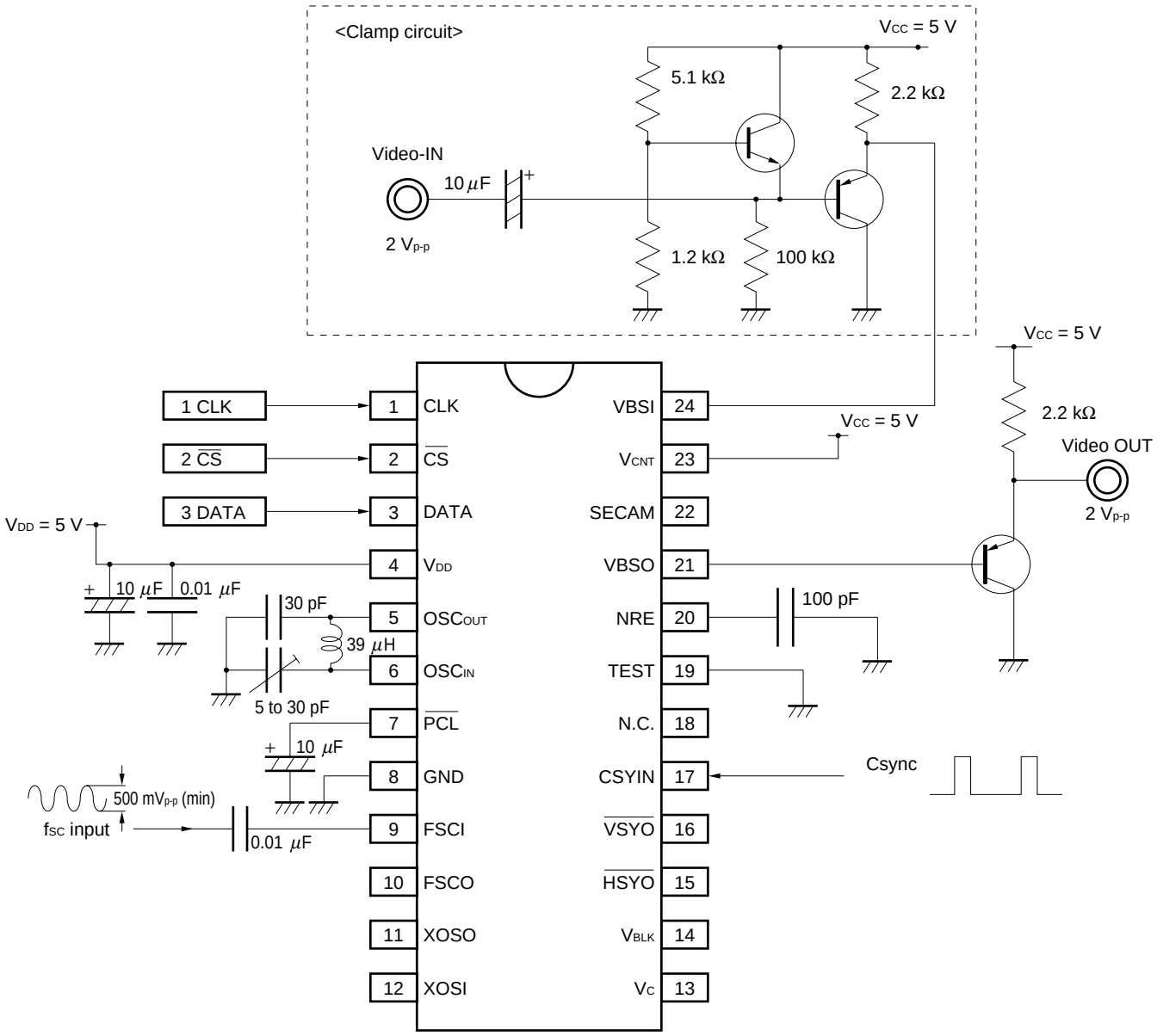
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	1	1	1	1	DI1	DI0	0	0

NTSC direct mode control bits		
DI1	DI0	Function
0	0	Clear NTSC direct mode
1	1	Set NTSC direct mode
0	1	Setting prohibited
1	0	(invalid operation will occur)

Caution Note the following when setting NTSC direct mode.

1. **Set the fsc input amplitude to 500 mV_{p-p} (MIN.).**
2. **Set the crystal oscillation command to oscillation OFF.**
3. **Set the video signal method control command to NTSC.**
4. **The internal video signal colors are the three colors; white, black, and blue (green cannot be displayed).**

Figure 3-5. Sample Application Circuit for NTSC Direct Mode



Cautions 1. The clamp circuit is not necessary when the sync-chip level (1 V DC) can be directly input to pin 24.

2. Pin 20 is connected so as to reject unwanted radiation.

3. This application circuit is assumed to input 2-V_{p-p} video signals.

4. To set NTSC direct mode, the NTSC direct mode control command must be input.

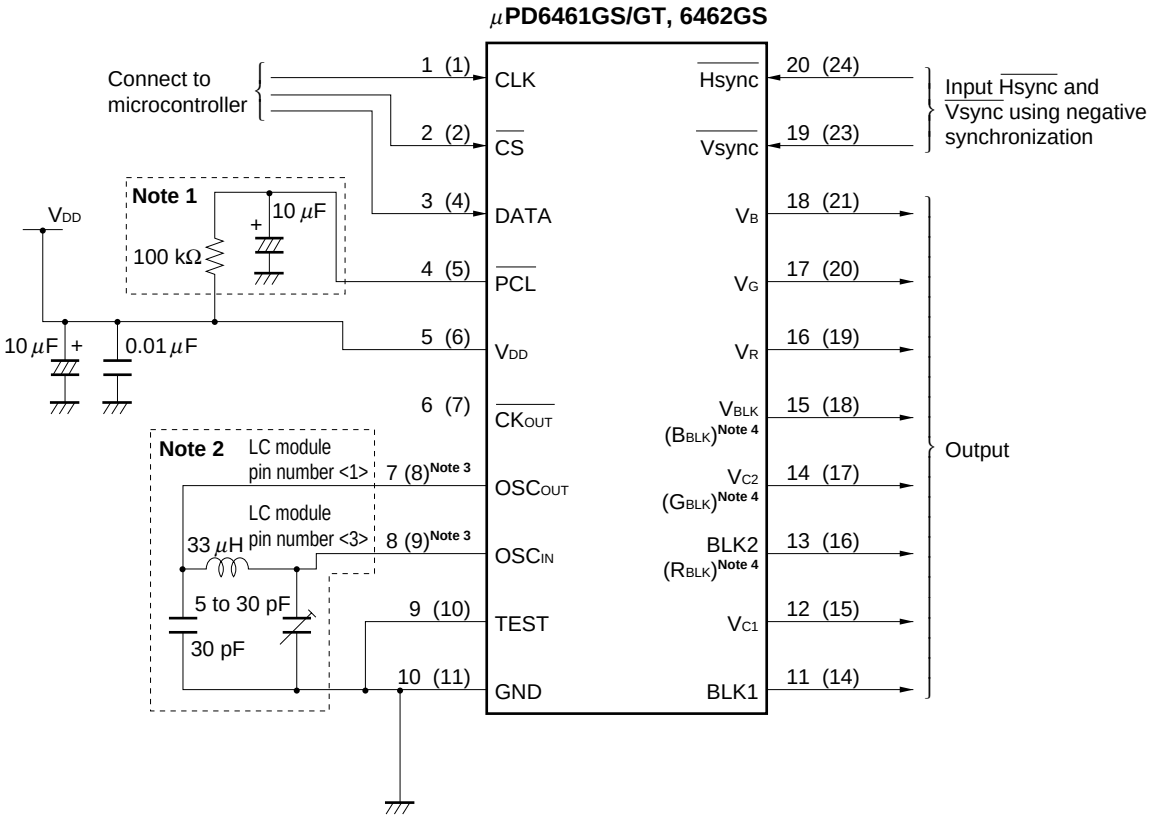
5. For the internal video signal color, select from the three colors; white, black, and blue (green cannot be displayed).

6. Input an fsc signal having an amplitude of at least 500 mV_{p-p} to pin 9.

3.2 RGB-System OSD LSI Application Examples

3.2.1 Sample μPD6461A or μPD6462 application circuit

Figure 3-6. Sample μPD6461 or μPD6462 Application Circuit



Notes 1. Set the CR constant so that the power-ON clear standards are satisfied.

2. This circuit enables the number of external components to be reduced and the oscillation frequency to be easily adjusted by using an LC module manufactured by Toukou Co., Ltd. (Part No.: Q285NCIS-11181).

3. Set the following when using external clock input.
OSCIN pin: External clock input, OSCOUT pin: Open

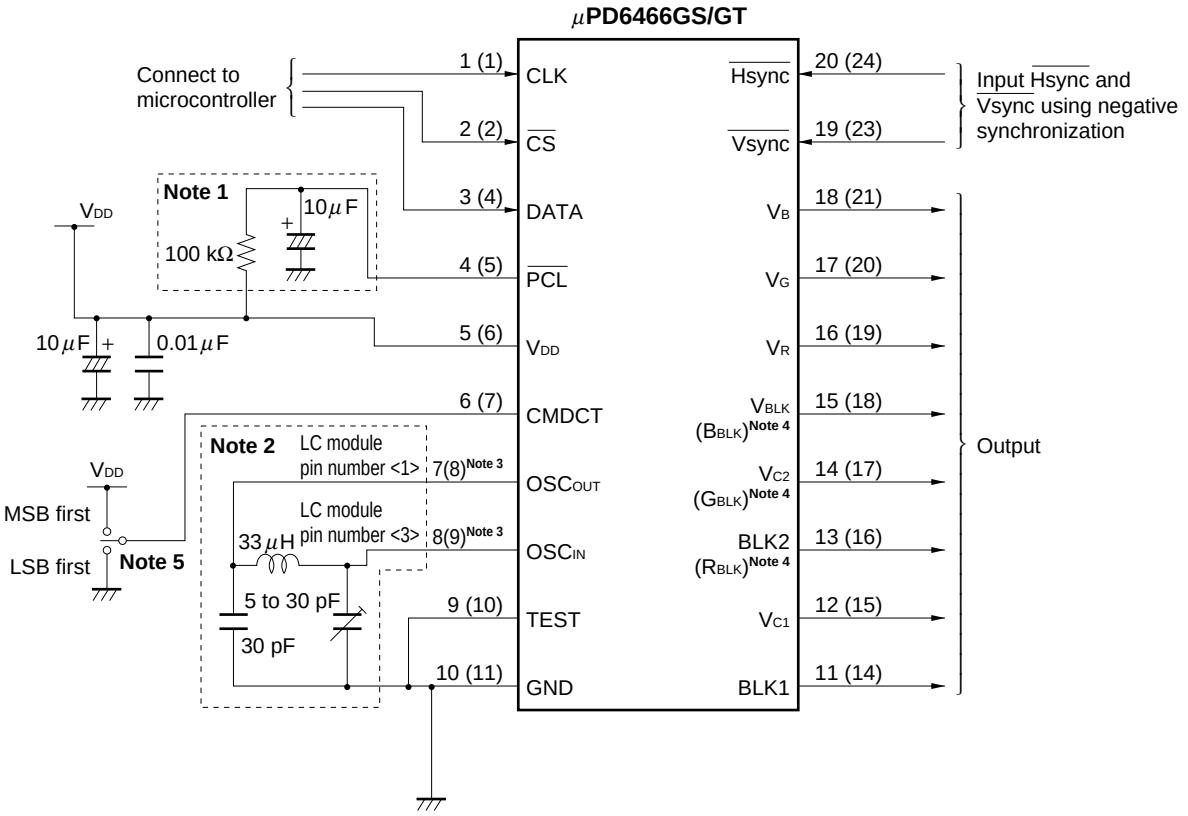
4. The symbols enclosed in parentheses are set by the mask code option (RGB + Blanking corresponding to RGB).

Remarks 1. The numbers enclosed in parentheses are the pin numbers for the μPD6461GT-×××.

2. With the μPD6461GT-×××, the effect of noise through the lead frame can be reduced by connecting the N.C. pins (pin numbers 3, 12, 13, and 22) to GND.

3.2.2 Sample μPD6466 application circuit

Figure 3-7. Sample μPD6466 application circuit



Notes 1. Set the CR constant so that the power-ON clear standards are satisfied.

2. This circuit enables the number of external components to be reduced and the oscillation frequency to be easily adjusted by using an LC module manufactured by Toukou Co., Ltd. (Part No.: Q285NCIS-11181).

3. Set the following when using external clock input.
OSCIN pin: External clock input, OSCOUT pin: Open

4. The symbols enclosed in parentheses are set by the initialization command (RGB + Blanking corresponding to RGB).

5. When this is open, LSB first is used.

Remarks 1. The numbers enclosed in parentheses are the pin numbers for the μPD6466GT-×××.

2. With the μPD6466GT-×××, the effect of noise through the lead frame can be reduced by connecting the N.C. pins (pin numbers 3, 12, 13, and 22) to GND.

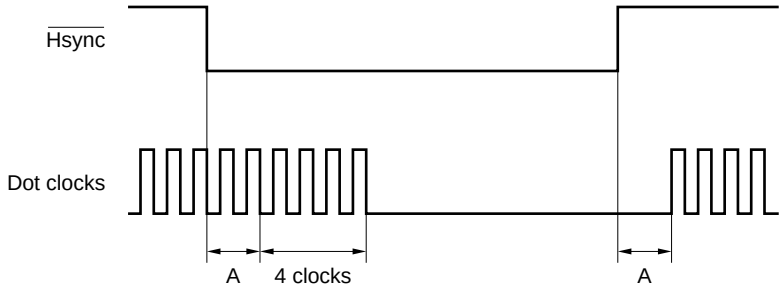
3.3 External Clock Forced Input to LC Oscillation Circuit Section

The external clock input conditions shown in this section are given as a reference example only and are not recommended by NEC.

This is a reference example for using the μPD6461 or μPD6462 with LC oscillation specified by the mask option or for using the μPD6464A or μPD6465. For external clock input conditions when external clock input is selected for the μPD6461 or μPD6462 mask option or when using the μPD6466, refer to the data sheet of each product.

Since an LC oscillation circuit is used to generate dot clocks in an OSD LSI (with an RGB-system OSD LSI, external clock input can be selected), to forcibly input an external clock, you must make the timing similar to when LC oscillation is used (oscillation stopped during $\overline{\text{Hsync}}$ period). Figure 3-8 shows the timing chart when an external clock is forcibly input.

Figure 3-8. Timing Chart for External Clock Forced Input



Cautions The following restrictions apply when an external clock is used.

1. **An interval of period A plus several clocks (4 clocks for the minimum character size) from the $\overline{\text{Hsync}}$ falling edge is required to stop the dot clocks. Typical period A values for each product are as follows.**

   μPD6461, μPD6462, μPD6464A : 200 ns (TYP.)

   μPD6465 : 500 ns (TYP.)

   The number of clocks, excluding period A, from the $\overline{\text{Hsync}}$ falling edge until the dot clocks are stopped depends on the character size in the horizontal direction. For the minimum character size, this value is 4 clocks. For the double character size, this value is 8 clocks.
2. **When the $\overline{\text{Hsync}}$ rising edge occurs, stabilize $\overline{\text{Hsync}}$ with the dot clocks stopped. Start the dot clock oscillation after period A elapses from the $\overline{\text{Hsync}}$ rising edge.**
3. **Make sure the phase relationship between the external clock and $\overline{\text{Hsync}}$ is always fixed.**
4. **Connect the OSC_{IN} and OSC_{OUT} as follows.**

   OSC_{IN} : Input external clock

   OSC_{OUT} : Open

CHAPTER 4 FAQ

4.1 All OSD LSIs

Q1-1. Can external clock input be used?

A1-1. When using the μPD6461 or μPD6462 with LC oscillation specified by the mask option or when using the μPD6464A or μPD6465, NEC does not recommend the input of external clocks.
If continuous external clocks are input, there is a risk that the external buffer that supplies the external clock during the $\overline{\text{Hsync}}$ period and the transistor for forcibly stopping oscillation, which is inside the device, in **(a)** of **Figure 2-2 Dot Clock Oscillation Equivalent Circuit** may short, an abnormal current may flow in this circuit, and the transistor may be damaged.
Dot clock LC oscillation or external clock input can be selected by using the mask option for the μPD6461 or μPD6462 or the initialization command for the μPC6466. For details, see **3.3 External Clock Forced Input to LC Oscillation Circuit Section**.

Q1-2. Must the serial data and $\overline{\text{Hsync}}$ or $\overline{\text{Vsync}}$ be synchronized?

A1-2. The serial data and $\overline{\text{Hsync}}$ or $\overline{\text{Vsync}}$ are not synchronized. However, when transferring video RAM write data, the command continuous input enable time must be strictly observed.
After serial data is transferred, if that data is related to video RAM writing, the data is written to video RAM by using the dot clock. Also, since the dot clock stops and data cannot be written to video RAM during the $\overline{\text{Hsync}}$ period when character display is ON, the data is written to video RAM after the dot clock oscillation begins again after the $\overline{\text{Hsync}}$ period ends.
The time required for writing video RAM data is as follows for the μPD6461 or μPD6462.

$$\text{When display is OFF} : \frac{12}{\text{fosc}} \times \text{Character size}$$

$$\text{When display is ON} : \frac{21}{\text{fosc}} \times \text{Character size} + t_{HWL}$$

For details related to the command continuous input enable time, refer to section about command continuous input enable time (μPD6461, μPD6462, or μPD6465) or BUSY period for command input (μPD6464A or μPD6465) in the Data Sheet of each version.

Q.1-3. Regarding a power-ON reset,

(1) When the $\overline{\text{PCL}}$ pin is connected to V_{DD} before the power is turned on with high level (power-ON clear rating (t_{PCLL}) is not satisfied), and the $\overline{\text{PCL}}$ pin is switched from high level to low level after the power has been turned on, what happens to output from the time the power is turned on until the power-ON clear operation is executed?

(2) Does the OSD LSI have any kind of internal switch so that no invalid data is output when the power is turned on in the situation described in (1)?

A.1-3. (1) The output cannot be predicted. Consider the following examples.

Example 1. If the mode register is PAL internal mode when NTSC is used, the black and white diagonal striped pattern may appear since the power-ON clear operation is not executed.

Example 2. Since the power-ON clear operation is not executed when external video signal mode is established in a video-system OSD LSI, when character display is set to ON, abnormal screen data may appear according to the video RAM contents (which had not been cleared). It may also occur to the output for the background. However, since the external video signal mode display is set to OFF when the $\overline{\text{PCL}}$ pin is at the low level, the character display output is stopped.

(2) The OSD LSI contains no kind of internal switch.
All NEC OSD LSIs are designed so that the power-ON clear operation is executed simultaneously when the power is turned on. Since no abnormal data is output if the power-ON clear operation is executed, we decided that no switch was required.

Q1-4. How do you decide the LC oscillation constants?

A1-4. NEC recommends L = 33 μH, C_{in} = 5 to 30 pF (trimmer capacitor), and C_{out} = 30 pF. For details, see **2.1.1 Dot Clock Oscillation Circuit**.

Q1-5. What is the difference between initialization by the video RAM batch clear command and that by the power-ON clear operation?

A1-5. The video RAM batch clear command is a software reset, and the power-ON clear operation is a hardware reset. For details, see **2.6 OSD LSI Power-ON Initialization**.

Q1-6. Are fields distinguished?

A1-6. An OSD LSI does not distinguish fields.

Q1-7. Is data that has been set in video RAM maintained as long as the setting is not changed?

A1-7. Since an OSD LSI has an on-chip refresh timer, video RAM data is maintained as long as character data is not written to video RAM, the power-ON clear operation or video RAM batch clear command is not executed, or the power is not turned off.

Q1-8. What is a 2-byte contiguous command?

A1-8. A 2-byte contiguous command is a command for writing characters to video RAM. For details, refer to the “Transferring Commands” section of the Data Sheet of each version.

Q1-9. Are there any limitations concerning the $\overline{\text{Hsync}}$ and dot clock timing relationship?

A1-9. As long as the command continuous input enable time is satisfied, there are no specific limitations. For information about the command continuous input enable time, refer to the Data Sheet of each version.

Q1-10 When transferring a 2-byte contiguous command, why does the command continuous input enable time when display is ON include the horizontal synchronization signal ($\overline{\text{Hsync}}$) width?

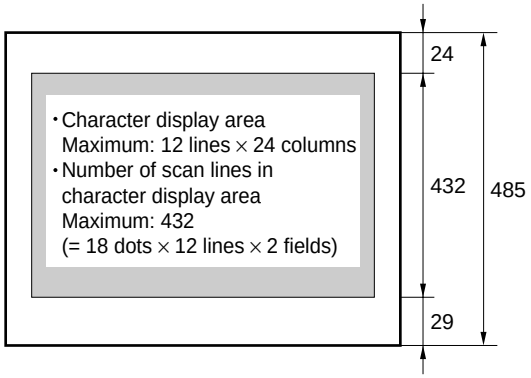
A1-10. In an OSD LSI, when display is ON, $\overline{\text{Hsync}}$ triggers resets for the internal system timing and controls the display position. Since the dot clock oscillation is stopped during the $\overline{\text{Hsync}}$ period due to these operations, no data is written to video RAM. As a result, the command continuous input enable time when display is ON includes $\overline{\text{Hsync}}$ synchronization signal width.

Q1-11. When a PAL signal is input with equivalent settings for the horizontal/vertical display start positions and dot clock frequency as those used for NTSC signal input, the vertical size of the characters is compressed and space appears at the lower portion of the display screen. What causes this? Also, can the same display be output in both the NTSC and PAL signal modes?

A1-11. This occurs because the number of scan lines differs in the NTSC and PAL modes, as shown in Figure 4-1. As a result, when a PAL signal is input, the horizontal/vertical display start positions and dot clock frequency must be adjusted, and the display area must be moved (the horizontal/vertical display start positions and dot clock frequency are adjusted in the signal mode units). Also, since a character non-display area is generated consisting of 53 scan lines per frame (equivalent to approximately 1.5 lines with the smallest size character) when an NTSC signal is input and 143 scan lines per frame (equivalent to approximately 4 lines with the smallest size character) when a PAL signal is input (see **Figure 4-2**), the same display cannot be output in both signal modes.

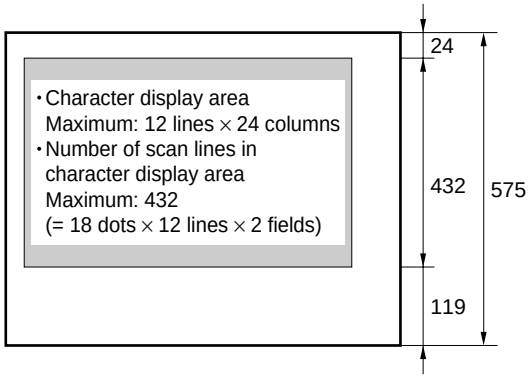
Figure 4-1. Character Display Area Image 1 – When NTSC and PAL Signals Are Input (for Equivalent Display Start Position and Dot Clock Frequency)

When NTSC signal is input
(number of effective scan lines: 485)



Set the display start position and dot clock frequency so that the character is displayed in the center of the screen.

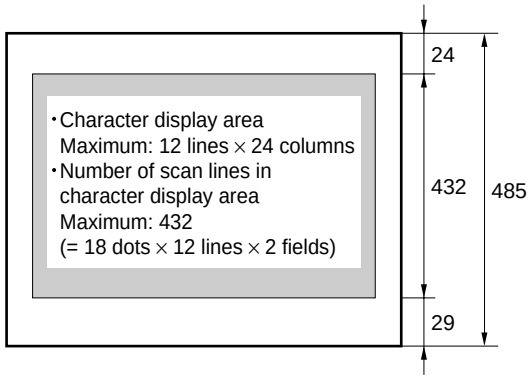
When PAL signal is input
(number of effective scan lines: 575)



Set the display start position and dot clock frequency equivalent to those used for NTSC signal input. Space appears at the bottom and right side, and the characters are compressed in the vertical direction.

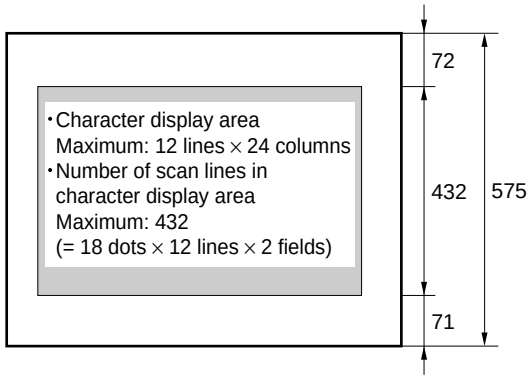
Figure 4-2. Character Display Area Image 2 – When NTSC and PAL Signals Are Input (for Center Display)

When NTSC signal is input
(number of effective scan lines: 485)



Set the vertical display start position to 12H, and set the horizontal display start position and dot clock frequency so that the character display area is in the center of the screen.

When PAL signal is input
(number of effective scan lines: 575)



Set the vertical display start position to 36H, and set the horizontal display start position and dot clock frequency so that the character display area is in the center of the screen.

4.2 Video-System OSD LSIs (μPD6464A and μPD6465)

Q2-1. Is a crystal oscillator required?

A2-1. It is required when 4fsc crystal oscillation is selected according to the oscillation mode control command. This is because the 4fsc signal generated by the oscillator and VCO is used as the reference clock for synchronization signal generation when internal video signal mode is set, and the fsc signal generated by dividing this 4fsc signal into four parts is used as the reference clock for internal video signal generation and for the synchronization separation circuit (when external video signal mode is set). Use the crystal oscillation control command to set crystal oscillation to ON when displaying characters.

Q2-2. Is fsc input required?

A2-2. It is required when quadruple oscillation is selected according to the oscillation mode control command. This is because the 4fsc signal generated according to the fsc input is used as the reference clock for synchronization signal generation when internal video signal mode is set, and the fsc signal generated by dividing this 4fsc signal into four parts is used as the reference clock for internal video signal generation and for the synchronization separation circuit (when external video signal mode is set). Use the crystal oscillation control command to set crystal oscillation to ON when displaying characters.
With the μPD6464A or μPD6465, the on-chip quadruple oscillation circuit enables the mounting area and cost to be reduced by using the LC oscillator instead of an expensive crystal oscillator. Also, in the LC oscillator only, since the oscillation precision is decreased due to the scattering of each element, a phase locked loop (PLL) is formed by inputting fsc, and the 4fsc signal is synchronized with the external fsc signal.

Q2-3. When fsc input is not used, are there limitations concerning the FSCI pin (pin 9) processing?

A2-3. Connect it to GND or V_{DD} and do not leave it open. Also, use the oscillation control command to select 4fsc crystal oscillation.

Q2-4. When SECAM is not used, are there limitations concerning the SECAM pin (pin 22) processing?

A2-4. If the video signal mode control command is used to select an option other than SECAM, the SECAM pin (pin 22) is disconnected from the internal circuits by an internal analog switch. Therefore, it makes no difference whether something (such as GND or V_{DD}) is connected to this pin or it is left open. However, if something is connected, note the absolute maximum rating of the input pin voltage (V_{IN}: –0.3 to V_{DD} + 0.3 V).

Q2-5. Are there limitations concerning pin processing when the V_C, V_{BLK}, $\overline{HSYO}$, $\overline{VSYO}$, CSYIN, and N.C. pins (pins 13 through 18) are not used?

A2-5. Leave them open.

Q2-6. When only the internal video signal is used with the μPD6464A or μPD6465, must the composite synchronization signal (Csync) be input?

A2-6. The composite synchronization signal (Csync) need not be input when internal video signal mode is used. With the μPD6464A or μPD6465, the synchronization signal is autogenerated by using the 4fsc signal generated according to $4f_{SC}$ crystal oscillation or quadruple oscillation.

Q2-7. What is the scanning method when internal video signal mode is used?

A2-7. When internal video signal mode is used, the scanning method is not interlaced.
The number of horizontal scan lines is 263 lines per field for NTSC or PAL-M mode and 312 lines per field for PAL or PAL-N mode.

Q2-8. What are the voltage levels of the composite synchronization signal (Csync) input to the CSYIN pin (pin 17)?

A2-8. The CSYIN pin (pin 17) has normal logic input. Therefore, the input levels are as follows according to CMOS input regulations.

Input high level voltage : 0.7 V_{DD} (MIN.)
Input low level voltage : 0.3 V_{DD} (MAX.)

Q2-9. When display is set to OFF in the μPD6464A or μPD6465, is the VBSI→VBSO status data through?

A2-9. When display is OFF in external video signal mode, the status is data through. Also, when display is OFF in internal video signal mode, a single screen color is displayed of the color used as the screen background color.

Q2-10. If the CSYIN pin (pin 17) is at high level when external video signal mode is used, what is the output status of the $\overline{\text{HSYO}}$ pin (pin 15: horizontal synchronization signal output) and the $\overline{\text{VSYO}}$ pin (pin 16: vertical synchronization signal output)? Also, if a 2-byte contiguous command is transferred at this time, is the data written correctly to video RAM if the command continuous input enable time (TB2, TB2') is observed?

A2-10. The $\overline{\text{HSYO}}$ pin and $\overline{\text{VSYO}}$ pin both remain at low level. Also, when a 2-byte contiguous command is transferred, if the CSYIN pin is at high level, since the IC is always in SYNC status, the t_{HWL} of the command continuous input enable time becomes infinitely large, and data cannot be written if display is ON (since LC oscillation stops, no clock for writing is supplied). Therefore, in this situation, data writing to video RAM stops when display is ON and operates when display is OFF.

Q2-11. What kind of drive capacity does the VBSO pin (pin 21: composite video signal output) have?

A2-11. Since the VBSO pin of the μPD6464A or μPD6465 only performs through output via an analog switch of the video signal that has been input to the VBSI pin (pin 24: composite video signal input pin), the VBSO pin has no drive capacity. Therefore, an emitter/follower circuit (buffer) according to a transistor must be added to the VBSO pin as shown in **3.1.1 Sample μPD6464A or μPD6465 Application Circuits** so that it can drive subsequent circuits.

Q2-12. What criteria are used when selecting a varactor diode?

A2-12. Use a varactor diode for which the capacitance changes in the range of approximately 2 to 10 pF with a voltage range on the order of 1 to 4 V. Also, since the capacitance of the capacitor connected to pin 12 in **Figure 3-1 Sample μPD6464A or μPD6465 Application Circuit (When Quadruple Oscillation Is Selected)** is the value when 1SV163 is used, be sure to re-evaluate the capacitance of the capacitor when the varactor diode is changed.

Q2-13. How do the μPD6464 and μPD6464A differ?

A2-13. The μPD6464A has PAL-N mode in addition to the video signal modes (NTSC, PAL, PAL-M, and SECAM) corresponding to the μPD6464.

Q2-14. Is a pull-up resistor required for the $\overline{PCL}$ pin (pin 7)?

A2-14. It is not required. The μPD6464A or μPD6465 has an on-chip resistor of approximately 50 kΩ between the $\overline{PCL}$ pin and V_{DD}.

Q2-15. If display is set to ON after a power-ON clear operation is executed and no characters are displayed on the screen even when various types of commands are transferred, what adjustments should be made?

A2-15. Check the following points and make the corresponding adjustments.

- Is the dot clock oscillating?
  An OSD LSI uses the dot clock when writing data to video RAM. If the dot clock oscillation is stopped, since the data that is supposed to have been transferred is not written to video RAM, the characters are not displayed normally.
- Is a composite synchronization signal (Csync) being input?
  In external video signal mode, the μPD6464A or μPD6465 timing generator resets the horizontal control section, vertical control section, and output controller by using the horizontal synchronization signal ($\overline{Hsync}$) and vertical synchronization signal ($\overline{Vsync}$) obtained by synchronization separation of Csync. It also generates reference signals for counting. If no Csync is being input, since the timing generator is not generating these reference signals, the characters are not displayed normally.
  In internal video signal mode, since $\overline{Hsync}$ and $\overline{Vsync}$ are autogenerated within the device, the characters are displayed even if no Csync is being input.
- Is 4fsc oscillation occurring?
  In the μPD6464A or μPD6465, the 4fsc or fsc signal generated by 4fsc crystal oscillation or quadruple oscillation is used for synchronization separation of Csync (when external video signal mode is selected) or for generation of the internal video signal and internal synchronization signal (when internal video signal mode is selected). If no 4fsc oscillation is occurring, since signal separation or generation is not being performed, the characters are not displayed normally.

4.3 RGB-System OSD LSIs (μPD6461, μPD6462, and μPD6466)

Q3-1. Can the dot clock be checked in the μPD6466?

A3-1. Although the dot clock frequency can be measured by using the CLK_{OUT} pin in the μPD6461 or μPD6462, the μPD6466 does not have this kind of pin.
With the μPD6466, the dot clock can be output from the BLK1 pin by connecting the TEST pin to V_{DD} and transferring the test mode command shown below.

2-byte command (MSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0

2-byte command (LSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0

Caution Use this command only for checking the dot clock.

Q3-2. When external clock input timing is used, what happens if t_{H-C} is less than 30 ns (MIN.) (for example, when the $\overline{\text{Hsync}}$ rising edge and the external clock falling edge overlap ($t_{H-C} \cong 0$ ns))?

A3-2. An OSD LSI uses $\overline{\text{Hsync}}$ for the horizontal control counter reset signal and uses the external clock for the horizontal control counter clock.
If the $t_{H-C} \geq 30$ ns rating cannot be satisfied, the $\overline{\text{Hsync}}$ rising edge and the external clock falling edge may overlap within the horizontal control counter depending on the arrival delay time difference of $\overline{\text{Hsync}}$ and the clock to the horizontal control counter (due to manufacturing variations and conditions of the usage environment such as power source voltage or temperature).
If the edges overlap, the timing of the cancellation of a counter reset due to $\overline{\text{Hsync}}$ and the count increment will overlap. Therefore, an unstable condition occurs in which the edge overlapped by the clock may or may not be counted as the first edge.
Actually, since both $\overline{\text{Hsync}}$ and the clock have a slight amount of jitter, the condition in which that edge is or is not counted is repeated. As a result, the horizontal display position shifts by one clock (one-dot horizontal jitter occurs).

Q3-3. What does the synchronization protection circuit do?

A3-3. The synchronization protection circuit prevents vertical jitter of the display character by generating a pseudo $\overline{\text{Hsync}}$ signal. For details, see **2.3.1 Synchronization Protection Circuit**.

Q3-4. In the μPD6461 or μPD6462, when the dot clock's external clock input is selected by using the mask option, can LC oscillation occur?

A3-4. When the dot clock's external clock input is selected by using the mask option, no dot clock LC oscillation can occur. When external clock input is selected, since the oscillation stage of the LC oscillation circuit is completely disconnected from the pin (see **(b)** in **Figure 2-2 Dot Clock Oscillation Equivalent Circuit**), even if an external LC oscillator is attached, it cannot be made to oscillate.

Q3-5. Are there any limitations concerning the clocks that are input when an external clock is selected?

A3-5. As criteria for the external clock, input the following amplitude and duty rate.

Input amplitude : Input high level voltage = 0.7 V_{DD} (MIN.)
Input low level voltage = 0.3 V_{DD} (MAX.)
Duty rate : Set at 50% (TYP.) Also, make the dispersion range within 40 to 60%.

For information about the external clock fall→Synchronization signal rise time (t_{C-H}), Synchronization signal rise→external clock fall time (t_{H-C}), and rise slew rate (ts), refer to the Electrical Specifications in the Data Sheet.

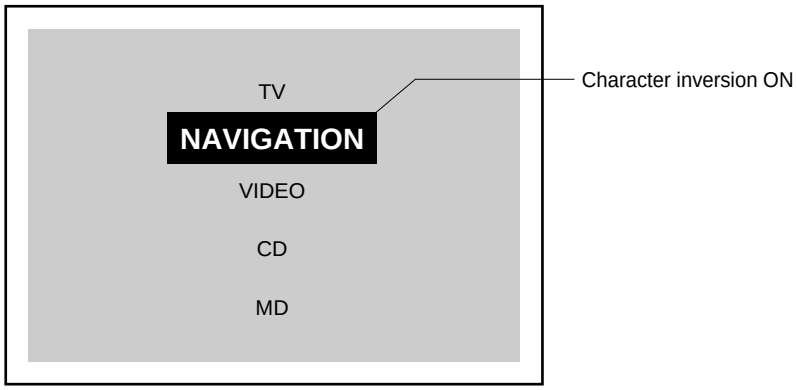
Q3-6. What is the approximate output impedance of each output pin?

A3-6. The μPD6461, μPD6462, and μPD6466 have a CMOS configuration, and the output impedance is approximately 100 Ω or less.

Q3-7. Is it possible to change the background color of a specific area?

A3-7. It is possible. Since the background color is set in terms of screens, first set the character inversion ON/OFF specification command (which is set in terms of screens; for the μPD6466, character color inversion ON/OFF specification command), to ON. Then, set the character inversion specification bit (for the μPD6466, character color inversion specification bit) of the display character control command, which is set in terms of characters, to ON (See **Figure 4-3**).

Figure 4-3. Sample Display Using Character Inversion



Remark The background color of the characters for which inversion is ON will be the character color (which can be set in terms of characters). The character color when inversion is ON is black (for or the μPD6466, white also can be specified).

Q3-8. If the character display is corrupted or if no character is displayed, what adjustments should be made?

A3-8. Check the following points and make the corresponding adjustments.

- Is the dot clock oscillating?
  An OSD LSI uses the dot clock when writing data to video RAM. If the dot clock oscillation is stopped, since the data that is supposed to have been transferred is not written to video RAM, the characters are not displayed.
- Are the $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ input?
  The timing generator resets the horizontal control section, vertical control section, and output controller by using the $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ that were input, and generates reference signals for counting. If $\overline{\text{Hsync}}$ and $\overline{\text{Vsync}}$ are not being input, since the timing generator is not generating reference signals, the characters are not displayed.
- Is the command executed within the command continuous input enable time?
  If the command continuous input enable time is not observed, the data that is supposed to have been transferred is not written to video RAM, and the character display is corrupted.

CHAPTER 5 DEVELOPMENT TOOLS

5.1 Overview of Development Tools

NEC provides the OSD LSI development tools introduced below. These all are available for short-term rental. When necessary, contact an NEC distributor or NEC sales representative.

- Character Pattern Editor for Windows
- Character ROM Verification and Evaluation Board
- OSD LSI Evaluation Board

Overviews of each tool are presented below.

(1) Character Pattern Editor for Windows

This is a tool for creating the character data to be installed in the character generator ROM. Its main features are described below. For details, refer to the **OSD LSI Character Pattern Editor User's Manual**.

- Supports Windows 3.1 and Windows 95

- Supports FD order reception

  Floppy disks are used for the mask ROM code ordering media. Use *.out for data save files. The following table shows the floppy disk physical format when ordering mask ROM code from NEC.

Size	Number of recording surfaces	Number of tracks	Number of sectors	Record length	Recording capacity
3.5 inch	Double sided	77 tracks/side	8 sectors/track	1024 bytes/sector	1261568 bytes

Remarks MS-DOS : Floppy disk formatting capacity: Select 1 MB (FORMAT d: /M)
PC DOS : Floppy disk formatting capacity: Select 1.2 MB (FORMAT12)[Note]
Windows 3.1 : Floppy disk formatting (F) capacity (C): Select 1 MB
Windows NT™ : Floppy disk formatting (F) capacity (C): Select 1.25 MB
Windows 95 : Floppy disk formatting (F) capacity (C): Select 1.2 MB

Note The floppy disk drive must support 1.2-MB diskettes. Register $FDD12.SYS in CONFIG.SYS. For details, refer to a PC DOS manual.

For details related to mask ROM code ordering, refer to the information document, **"ROM Code Ordering Method"**.

- **Maintains upward compatibility with DOS-version environment**

  Data save files (*.out and *.sav) created by the conventional DOS-version editor can be used, and compatibility with the DOS-version editor is maintained.

- **Provides simple operations and an excellent user interface**

  By using the toolbar, you can execute frequently used functions by clicking a single button. Also, by using multi-document interface (MDI) mode, you can manipulate multiple files (data) on the same screen.

(2) Character ROM verification and evaluation board

This is a tool for verifying the character that was created by the character pattern editor (using *.out for data files) on an actual monitor screen before ordering the mask ROM. Use this board with the connections shown in Figures 5-1 and 5-2.

Remark MS-DOS 3.3 is required to run the character ROM verification and evaluation board system software. In addition, the character ROM verification and evaluation board must be connected to a personal computer by using the supplied interface (I/F) board. When evaluating character data, a PC-98 or PC-98-compatible computer (equipped with an expansion slot) must be used as the personal computer where this software can be activated and this I/F board can be connected.

Figure 5-1. ROM Verification Board Connection Diagram for RGB Display

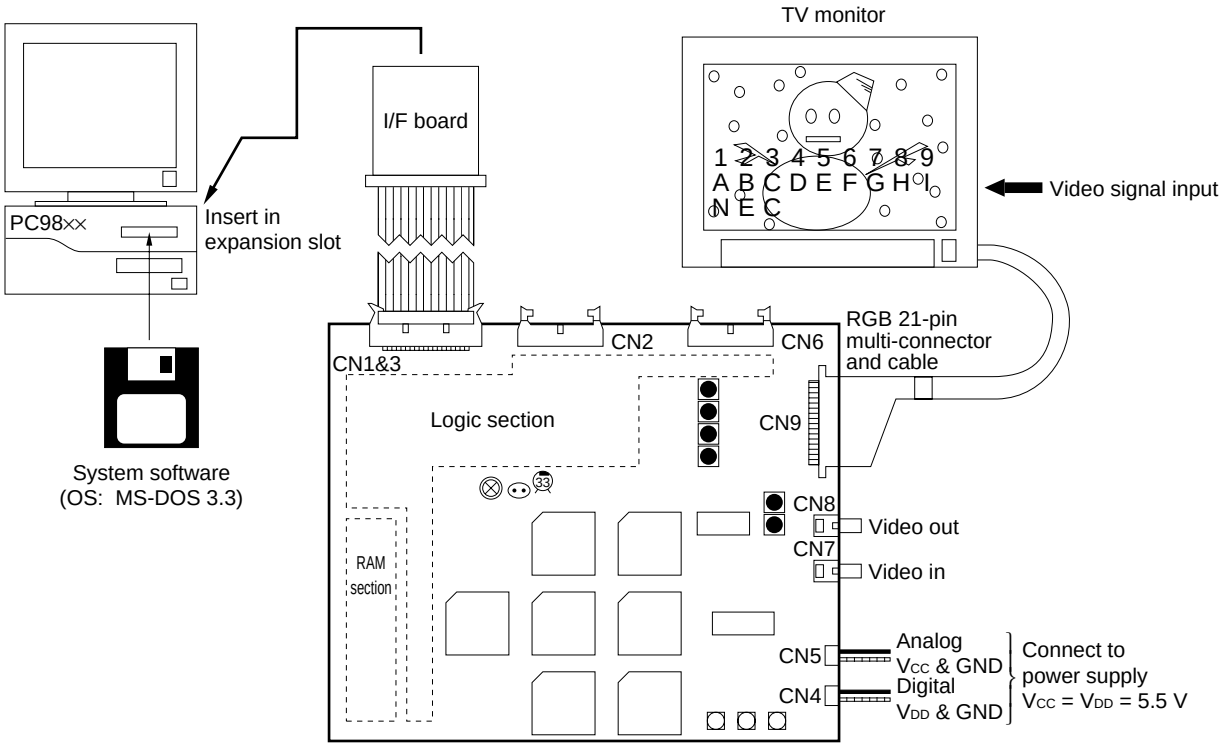
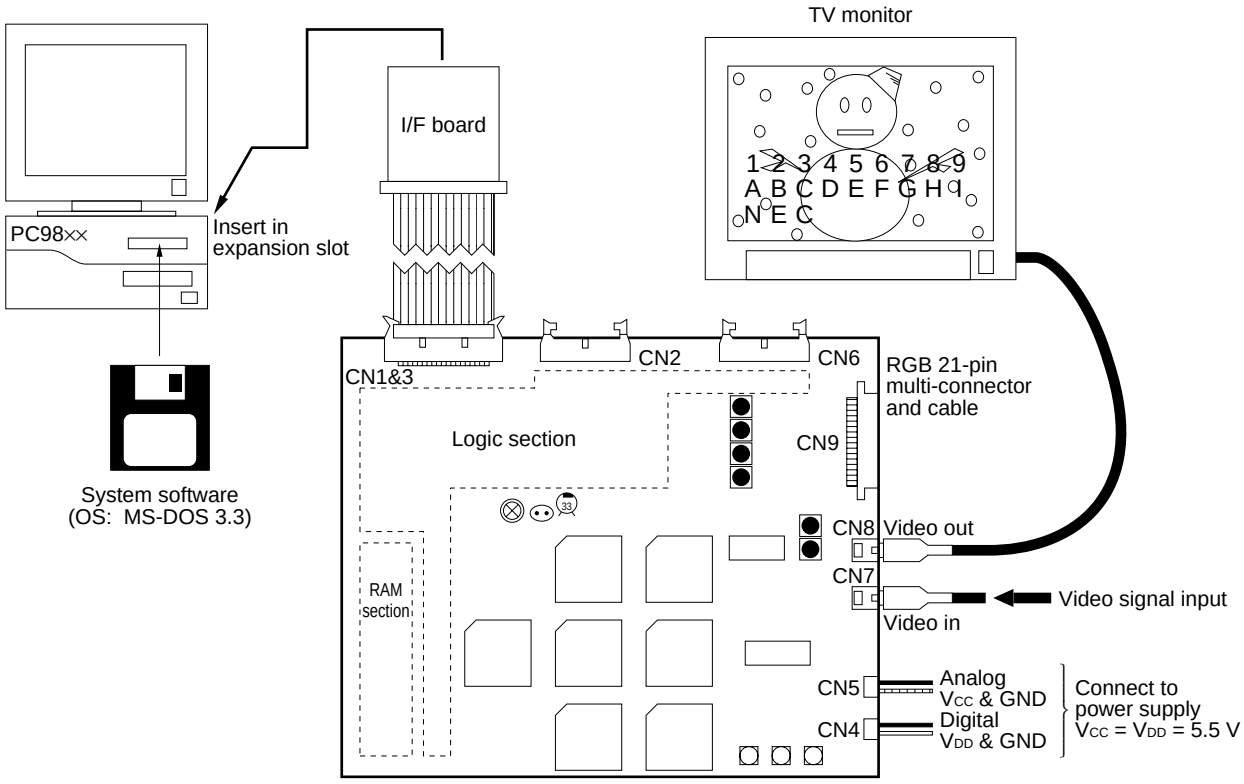


Figure 5-2. ROM Verification Board Connection Diagram for VCR Display



(4) OSD LSI evaluation board

This is a tool for evaluating the functions of NEC standard products or of engineering samples (ES), etc. after the mask ROM has been ordered.

There are two types of OSD LSI evaluation boards. The μPD6464A and μPD6465 evaluation board is for video-system OSD LSIs and the μPD6461, μPD6462, and μPD6466 evaluation board is for RGB-system OSD LSIs. Use these boards with the connections shown in Figures 5-3 and 5-4.

Remark MS-DOS 3.3 is required to run the OSD LSI evaluation board system software. When evaluating OSD LSIs, a PC-98 or PC-98-compatible computer must be used as the personal computer where this software can be activated.

Figure 5-3. Video-System OSD LSI Evaluation Board Connection Diagram

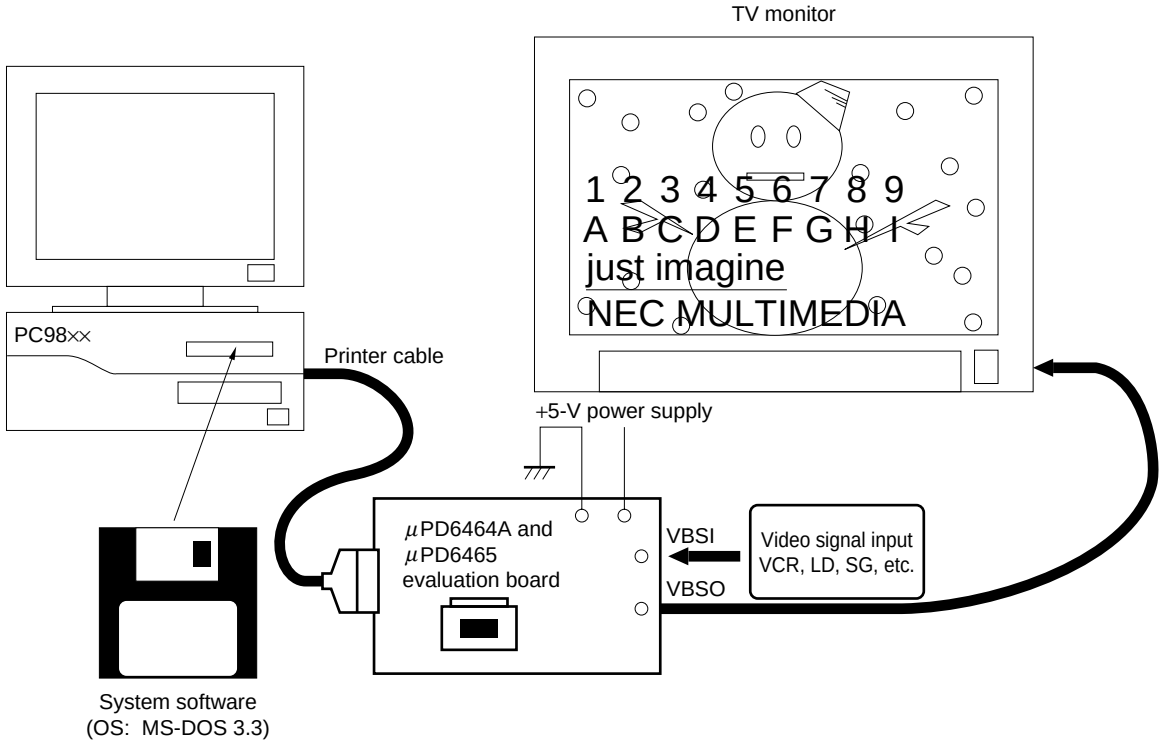
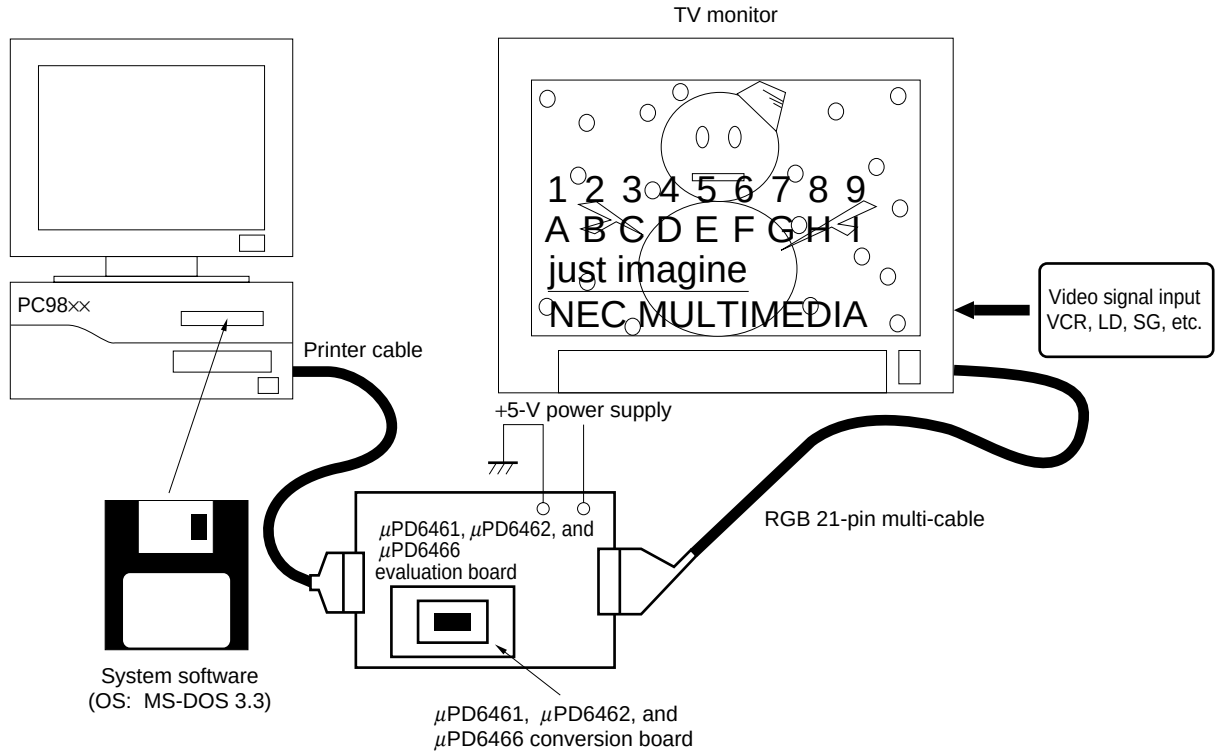


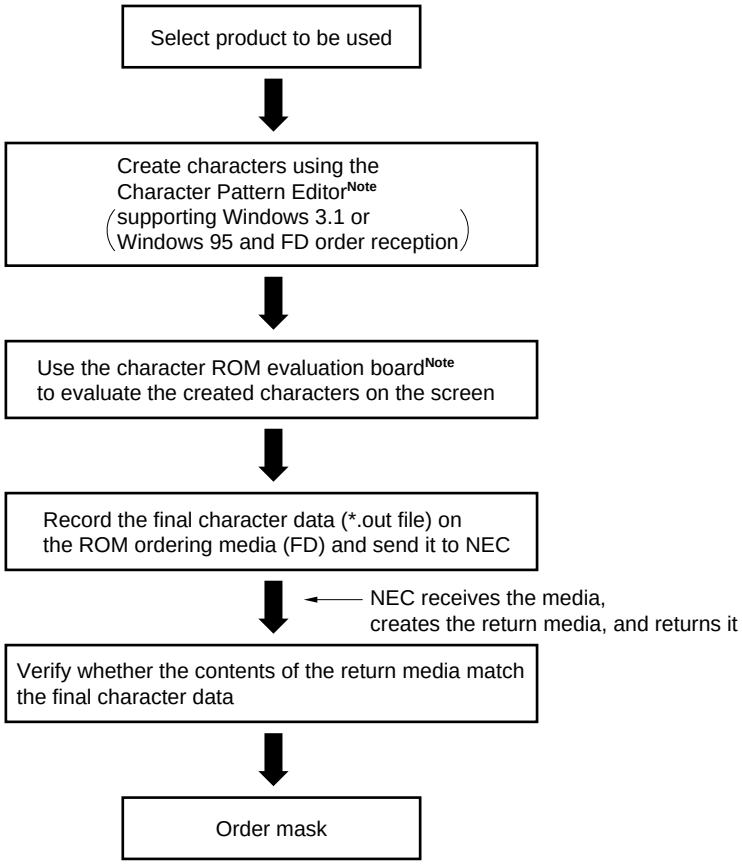
Figure 5-4. RGB-System OSD LSI Evaluation Board Connection Diagram



5.2 Concerning OSD LSI Mask ROM Ordering

The tools described in **5.1 Overview of Development Tools** can be used for ordering mask ROM code according to the procedure shown in Figure 5-5. For details related to mask ROM code ordering, refer to the information document, **"ROM Code Ordering Method"**.

Figure 5-5. OSD LSI Mask ROM Code Ordering Procedure (for FD Order Reception)



Note These tools are rented. For details, contact an NEC distributor or NEC sales representative.

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