silicon systems®

SSI 75T957/957A
DTMF Receiver with Dial Tone Reject Filter

T-75-27-07

May, 1989

DESCRIPTION

The SSI 75T957/957A combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four bit binary data. Dial tone rejection and 60 Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low power CMOS processing, the SSI 75T957/957A is packaged in a 22-pin DIP or 24-pin SO. The SSI 75T957A will operate with a supply range of 5 to 12 volts; the 75T957 is for 5V-only operation. An inexpensive 3.58 MHz television crystal and a resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

(Continued)

FEATURES

- Complete DTMF receiver in 22-pin DIP or 24-pin SO
- Decodes all 16 DTMF digits
- Excellent dial tone and speech immunity
- Meets telephone impulse noise immunity standards
- Digitally selectable sensitivity to -38 dBm
- Selectable 4-bit hexadecimal or binary-coded 2-of-8 output
- Fabricated using low-power CMOS technology
- Operates at 5V (75T957) or 12V (75T957A)
- Second source of Teltone M-957

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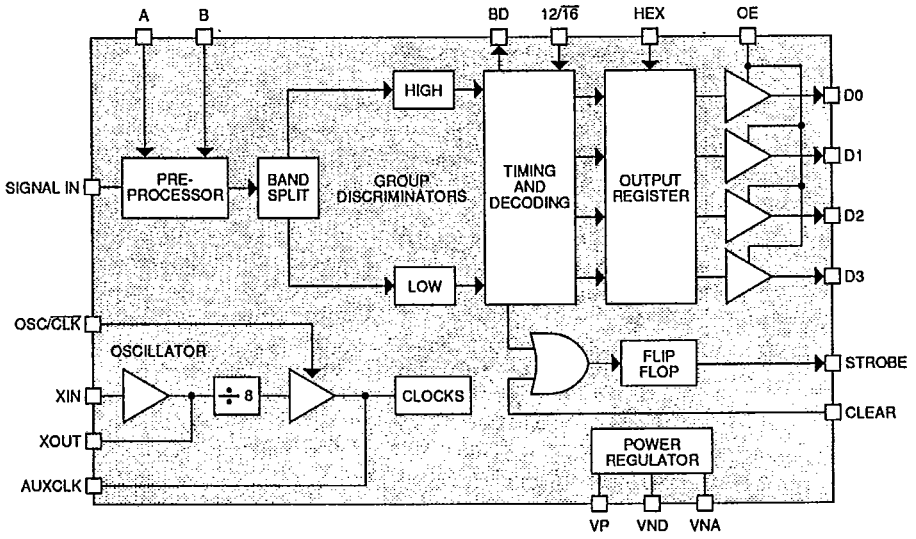
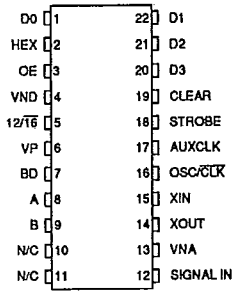
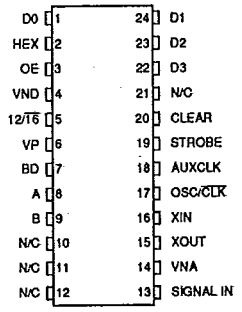
BLOCK DIAGRAM



PIN DIAGRAMS



22-pin DIP



24-pin SO

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 75T957/957A DTMF Receiver with Dial Tone Reject Filter

DESCRIPTION (Continued)

The SIGNAL IN input to the SSI 75T957/957A interfaces readily to telephone lines, radio receivers, tape players and other DTMF signal sources. Inputs A and B control sensitivity to a maximum of -38 dBm, while the 12/$\overline{16}$ input determines the signals to be detected. The pre-processing stages of the SSI 75T957/957A filter out dial tone and noise, split the signal into its high frequency group and low frequency group components, and hard limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Post-processing stages of the SSI 75T957/957A time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors and are three-state enabled to facilitate bus-oriented architectures.

PIN DESCRIPTION

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
SIGNAL IN	12	13	I	DTMF input. Timings are shown in Figure 1. Internally biased so that the input signal may be AC coupled. SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 3. See Table 1 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	5	5	I	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1," the SSI 75T957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0," the SSI 75T957 detects all 16 DTMF signals (1 through D).
A, B	8, 9	8, 9	I	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of -38 dBm.
D3, D2 D1, D0	20, 21 22, 1	22, 23 24, 1	O	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 1. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 1.
OE	3	3	I	Output enable. When OE is at logic "1," the data outputs are in the CMOS push/pull state and represent the contents of the output register. When OE is driven to logic "0," the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 1.

PIN DESCRIPTION (Continued)

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
HEX	2	2	I	Binary output format control. When HEX is at logic "1" the output of SSI 75T957 is full, 4-bit binary. When HEX is at logic "0," the output is binary coded 2-of-8. Table 1 shows the output codes.
STROBE	18	19	O	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1," whichever is earlier. Once cleared, STROBE will not rise to a logic "1" until a new valid tone (preceded by a valid pause) is detected. Timings are shown in Figure 1.
CLEAR	19	20	I	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0." When CLEAR is at logic "0," STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	7	7	O	Button down. A logic "1" BD indicates a signal has been detected and is being validated. BD precedes STROBE and data outputs.
XIN, XOUT	15, 14	16, 15	I	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1." See Figure 4.
OSC/$\overline{CLK}$	16	17	I	Time base control. When OSC/$\overline{CLK}$ is at logic "1," the output of the SSI 75T957's internal oscillator is selected as the time base. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the time base.
AUXCLK	17	18	O	Auxiliary clock input. When OSC/$\overline{CLK}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the SSI 75T957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the SSI 75T957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	13, 4	14, 4	-	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	6	6	-	Positive power supply connection.
N/C	10, 11	10-12, 21	-	Not connected. These pins have no internal connection and may be left floating.

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SSI 75T957/957A TIMING (-40°C ≤ TA ≤ +85°C; 4.5V ≤ VP ≤ 13.2V. Refer to Figure 1.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
tcl	Strobe Clear Time		-	160	250	ns
t_{PW}	Clear Pulse Width		200	-	-	ns
t_{BD}	BD Detect Time		7	-	22	ms
t_{BR}	BD Release Time		2	-	18	ms
	Output Enable Time	C_L = 50pF, R_L = 1KΩ	-	200	300	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	150	200	ns
	Output Rise Time	C_L = 50pF	-	200	300	ns
	Output Fall Time	C_L = 50pF	-	160	250	ns

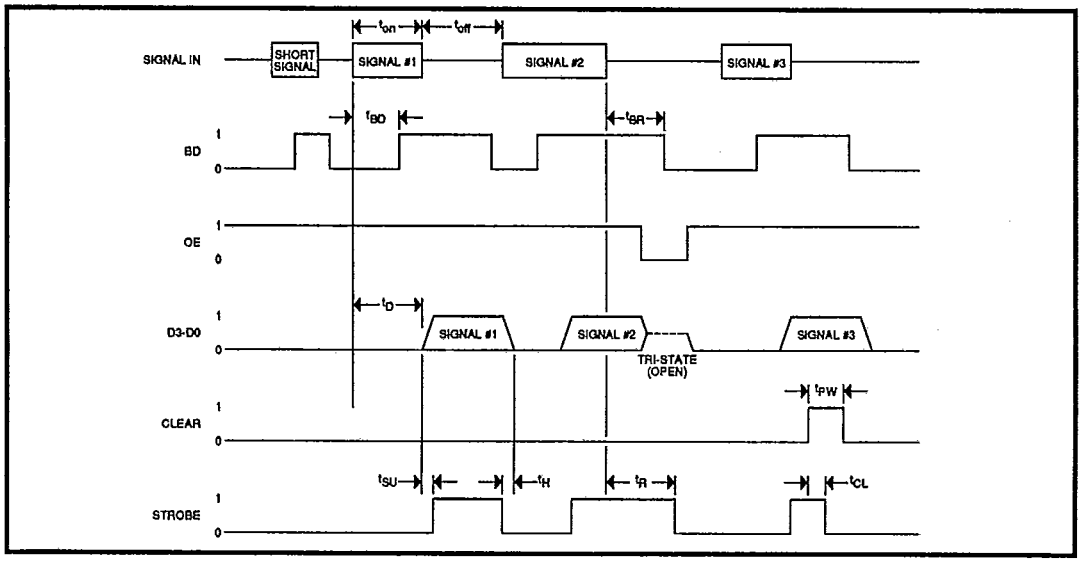


FIGURE 1: Timing Diagram

TABLE 1: DTMF TO BINARY DECODING

DIGIT	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT	BINARY CODED 2-OF-8 OUTPUT
			D3 D2 D1 D0	D3 D2 D1 D0
1	697	1209	0001	0000
2	697	1336	0010	0001
3	697	1477	0011	0010
4	770	1209	0100	0100
5	770	1336	0101	0101
6	770	1477	0110	0110
7	852	1209	0111	1000
8	852	1336	1000	1001
9	852	1477	1001	1010
0	941	1336	1010	1101
*	941	1209	1011	1100
#	941	1477	1100	1110
A	697	1633	1101	0011
B	770	1633	1110	0111
C	852	1633	1111	1011
D	941	1633	0000	1111

Note: The SSI 75T957 detects signals A through D when the 12/$\overline{16}$ input is at logic "0."

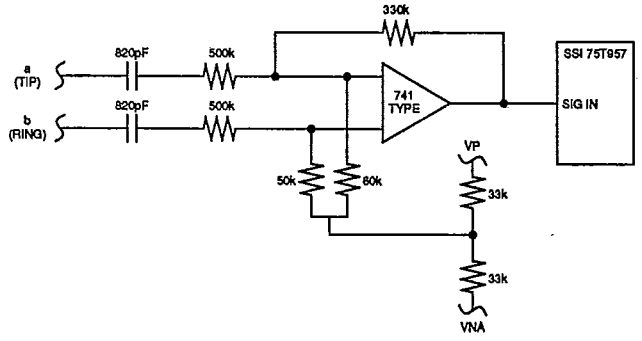
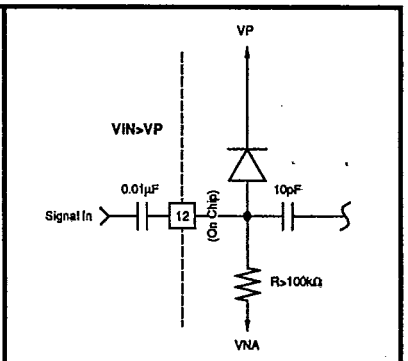


FIGURE 2: Telephone Line Differential Input Interface



NOTE: Coupling capacitor needn't be used when VIN is less than VP.

FIGURE 3: Input Signal Configuration

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ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P	VND=VNA=0V	16.0V
Input Voltage	All inputs except SIGNAL IN	(V_P + 0.5V) to (VND - 0.5V)
SIGNAL IN Voltage		(V_P + 0.5V) to (V_P - 22V)
Storage Temperature		-65° to 150°C
Operating Temperature		-40° to 85°C
Lead Temperature	Soldering, 5 sec.	260°C
Power Dissipation		1W

ELECTRICAL CHARACTERISTICS
(-40°C ≤ T_A ≤ +85°C)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
SIGNAL IN Input Requirements						
Signal Level (per tone) (See Note 1)	V_P=12V	A=0, B=0	-24	-	+6	dBm
		A=1, B=0	-27	-	+3	dBm
		A=0, B=1	-30	-	0	dBm
		A=1, B=1	-	-32	-	dBm
	V_P=5V	A=0, B=0	-32	-	-2	dBm
		A=1, B=0	-35	-	-5	dBm
		A=0, B=1	-38	-	-8	dBm
		A=1, B=1	-	-40	-	dBm
Signal Frequency Deviation with Detection			±(1.5% +2)	±2.5%		Hz
Signal Frequency Deviation without Detection			±3.5%	±3.0%	-	Hz
Twist	See Note 2		-	±10	dB	
Gaussian Noise	See Note 3		12	A-7	dB	
Dial Tone Level (per tone)	F ≤ 480 Hz; see Note 4		-	-	A+22	dB
Digital Input Requirements (See Note 5)						
Logic 0 Voltage	V_P=12V	0	-	3.6	V	
	V_P=5V	0	-	1.5	V	
Logic 1 Voltage	V_P=12V	8.4	-	12.0	V	
	V_P=5V	3.5	-	5.0	V	

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ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Output Characteristics (See Note 5)					
Logic 0 Voltage	V_P=12V, Io = 1.0mA	0	-	1.2	V
	V_P=5V, Io = 0.4mA	0	-	0.5	V
Logic 1 Voltage	V_P=12V, Io = -0.5mA	10.8	-	12.0	V
	V_P=5V, Io = -0.2mA	4.5	-	5.0	V
Three-State Leakage		-	-	10.0	µA
Miscellaneous Characteristics					
CMOS Latch-up Voltage	See Note 7	20	-	-	V
SIGNAL IN Input Impedance	F=1kHz||15pF	100k	-	-	Ω
Power Requirements					
Supply Current	V_P=12V	-	20	40	mA
	V_P=5V	-	9	18	mA
Power Dissipation	V_P=12V, see Note 6	-	204	480	mW
(outputs open)	V_P=5V, see Note 6	-	30	90	mW
Power Supply Wide Band Noise	A=0, B=0				
	V_P=12V	-	-	25	mVpp
	V_P=5V	-	-	10	mVpp

Notes:
1. With an ambient temperature of 25°C, the signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, -24dBm equals 49mVrms.)
2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.
3. With an ambient temperature of 25°C, the signal level is at A+5, the signal frequency deviation and twist are at 0, and the signal applied is 50ms off and 50ms on. The A level is the minimum detect level selected.
4. The signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The A level is the minimum detect level selected.
5. Logic levels shown are referenced to VND.
6. For an ambient temperature of 25°C.
7. Power supply excursions above this value can cause device damage.

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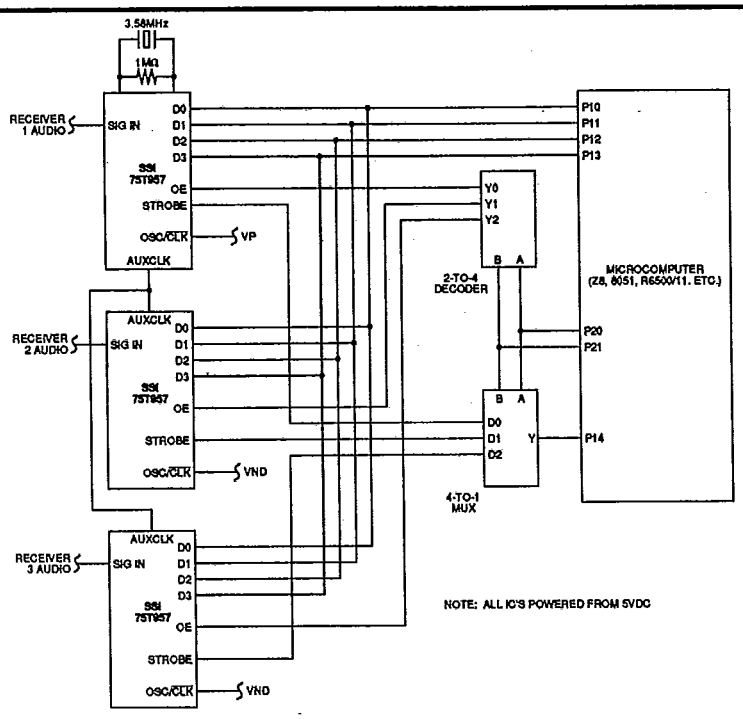

FIGURE 4: Multiple Receiver/Microprocessor Interface

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T957 22-pin Plastic DIP, 5V-only	SSI 75T957-IP	75T957-IP
SSI 75T957 24-pin SOL, 5V-only	SSI 75T957-IL	75T957-IL
SSI 75T957A 22-pin Plastic DIP, 5-12V operation	SSI 75T957A-IP	75T957A-IP
SSI 75T957A 24-pin SOL, 5-12V operation	SSI 75T957A-IL	75T957A-IL