PMC1632/PMC1632L
ULTRA HIGH SPEED 16K x 32
STATIC CMOS RAM (SCRAM) MODULE

PRELIMINARY

FEATURES

- Super-fast CMOS 512k Module
- High speed (Equal Access and Cycle Times)
  - 17/20/25/35 ns (Commercial)
- Low Power Operation (Commercial)
  - 5.5W Active – 17/20
  - 4.0W Active – 25/35
  - 880 mW Standby (TTL Input)
  - 660 mW Standby (CMOS Input)
  - 22 mW Standby (CMOS Input) PMC1632L
- 5V±10% Power Supply
- 2V Data Retention, 100 µA Typical Current from 2.0V.
- Output Enable and Chip Enable Control Functions
- Common Inputs and Outputs
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE Technology™
- Low Profile—Max Height 0.50 in.
- Jedec Compatible Standard Pinout

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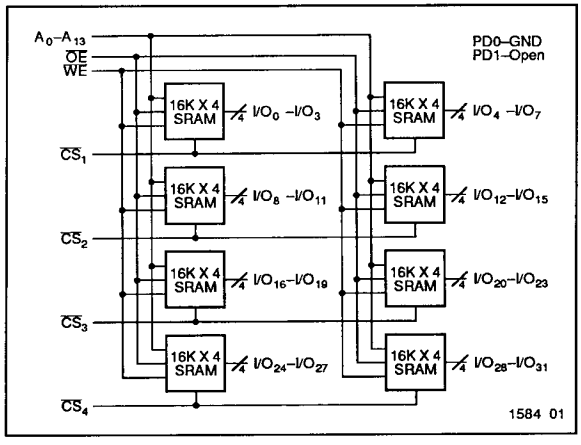
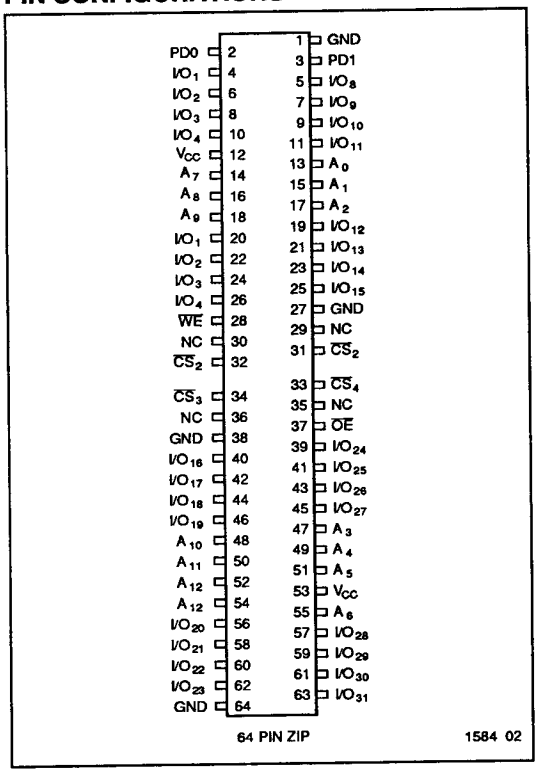
DESCRIPTION

The PMC1632 and PMC1632L are superfast 512K modules organized as 16k words by 32 bits. The module features an active low Output Enable control to eliminate data bus contention. Access times as fast as 17ns are available permitting high clock frequency system operating speeds. The module operates from a single 5V±10% tolerance power supply. In CMOS standby mode current drain is a low 4mA worst case at 5V and typically 100µA from a 2V supply for the L version. The module is manufactured with eight Performance 16k x 4 SOJ packaged SCRAMS mounted on an epoxy laminate board with ZIP configured pins. Four separate Chip Enable inputs permit independent or multiple byte reads and writes to the module. The eight P4C198 SCRAMs used are manufactured with PACE Technology and fully tested in SOJ and module form by Performance. The module is available in a space saving 64 pin ZIP with JEDEC compatible pinout. The module is also available in 16, 24 and 28 bit configurations.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions	PMC1632 PMC1632L		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC}–0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage		–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.		0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.	V_{CC}–0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max. Com'l. V_{IN} = GND to V_{CC}	–20	+20	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, Com'l. V_{OUT} = GND to V_{CC}	–20	+20	µA

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CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	70	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		PMC1632		PMC1632L		Unit
				Min	Max	Min	Max	
I_{CC}	Dynamic Operating Current – 17, 20	V_{CC} = Max., f = Max., Outputs Open	Com'l.	—	1000	—	—	mA
I_{CC}	Dynamic Operating Current 25, 35	V_{CC} = Max., f = Max., Outputs Open	Com'l.	—	720	—	720	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, V_{CC} = Max., f = Max., Outputs Open	Com'l.	—	160	—	160	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1 \geq V_{HC}$ or $CE_2 \leq V_{LC}$, V_{CC} = Max., f = 0, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Com'l.	—	120	—	4	mA

n/a = Not Applicable

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DATA RETENTION CHARACTERISTICS (PMC1632L Only)

Symbol	Parameter	Test Condition	Min	Typ.* V_{CC}= 2.0V	Typ.* V_{CC}= 3.0V	Max V_{CC}= 2.0V	Max V_{CC}= 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	Mil. Com'l.		.1	.15	1.2	2	mA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

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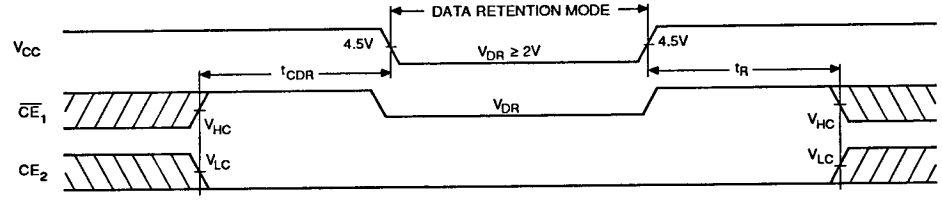
*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



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AC CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-17		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	17		20		25		35		ns
t_{AA}	Address Access Time		17		20		25		35	ns
t_{AC}	Chip Enable Access Time		17		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		7		10		10		14	ns
t_{OE}	Output Enable Low to Data Valid		10		12		15		25	ns
t_{OLZ}	Output Enable to Output in Low Z	2		2		3		3		ns
t_{OHZ}	Output Disable to Output in High Z		7		8		10		14	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		17		20		25		30	ns

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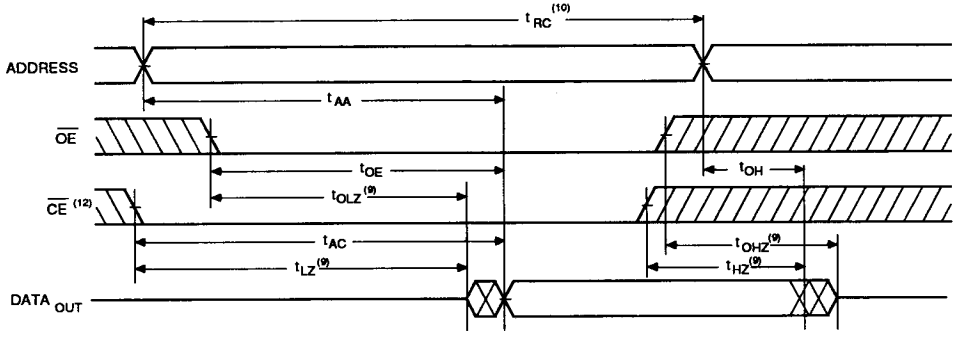
READ CYCLE NO.1 ($\overline{OE}$ controlled) [5]



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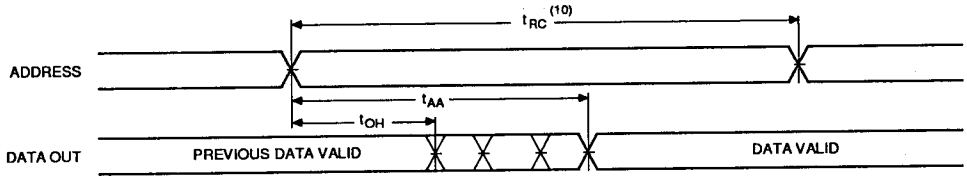
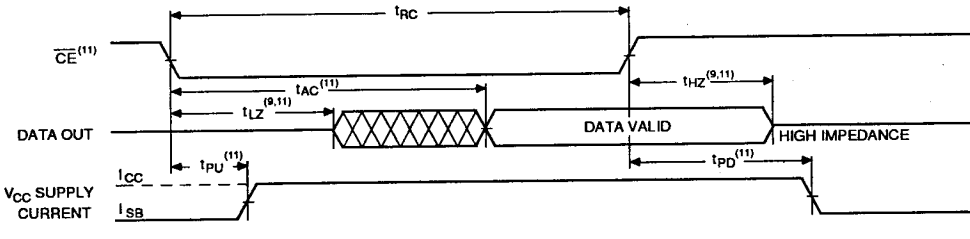
Notes:
5. $\overline{WE}$ is high for READ cycle.

READ CYCLE NO.2 (ADDRESS controlled) [5,6]



READ CYCLE NO.3 ($\overline{CE}$ (12) controlled) [5,7,8]



Notes:

6. $\overline{CE}$, and $\overline{OE}$ are low READ cycle.
7. $\overline{OE}$ is low for the cycle.
8. ADDRESS must be valid prior to, or coincident with, $\overline{CE}$ ($\overline{CE}_1$ and $\overline{CE}_2$ for PMC1632L) transition low.
9. Transition is measured ±200mV from steady state voltage prior to change, with loading as specified in Figure 1.
10. Read Cycle Time is measured from the last valid address to the first transitioning address.
11. Not used
12. Not used

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-17		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	14		15		20		30		ns
t_{CW}	Chip Enable Time to End of Write	12		15		20		30		ns
t_{AW}	Address Valid to End of Write	12		15		20		25		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		20		25		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	8		10		13		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		8		10		10	ns
t_{OW}	Output Active from End of Write	2		2		3		3		ns

*V_{CC} = 5V ± 5% for -15

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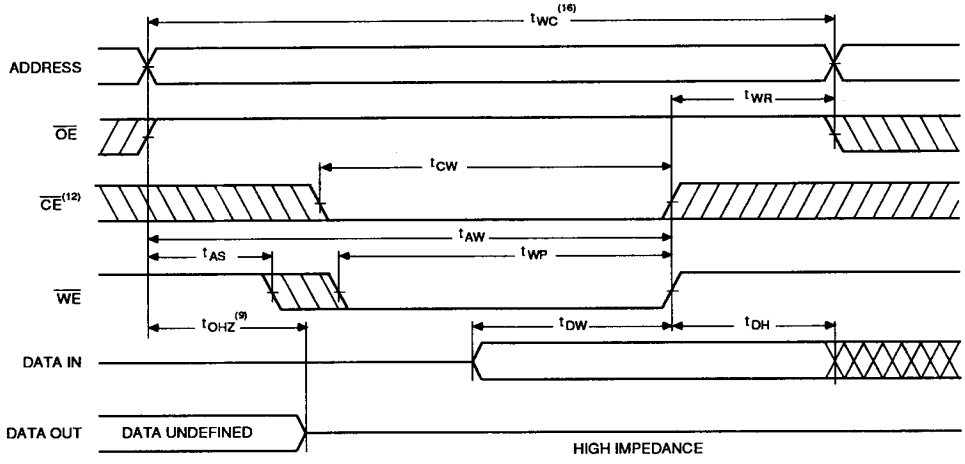
WRITE CYCLE NO. 1 (With $\overline{OE}$ high)



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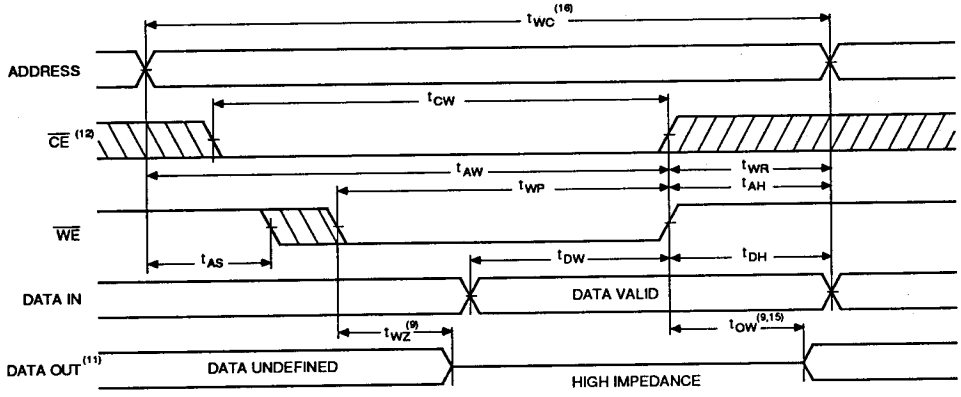
WRITE CYCLE NO. 2 ($\overline{WE}$ CONTROLLED) [13,14]



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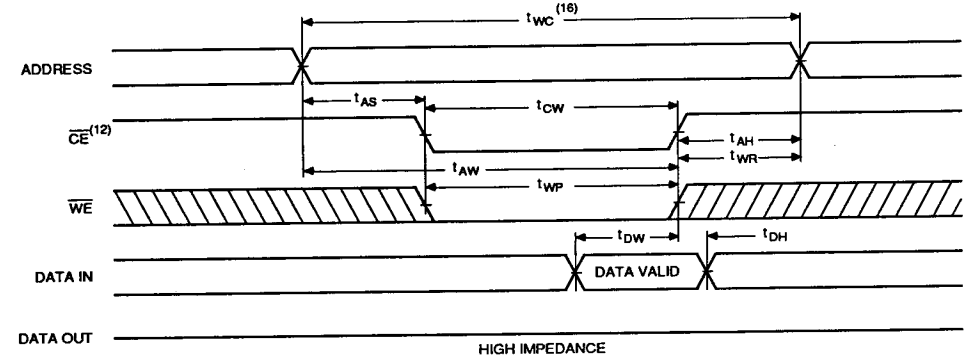
WRITE CYCLE NO. 3 ($\overline{CE}$ (12) CONTROLLED) [13,14]



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Notes:
13. $\overline{CE}$ and $\overline{WE}$ must be low for WRITE cycle.
14. $\overline{OE}$ is low for this WRITE cycle.
15. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a low impedance state.
16. Write Cycle Time is measured from the last valid address to the first transitioning address.

TRUTH TABLES

PMC1632

$\overline{CE}_N$	$\overline{WE}$	$\overline{OE}$	Mode	Output
H	X	X	Standby	High Z
L	H	H	Output Inhibit	High Z
L	H	L	READ	D_{OUT}
L	L	X	WRITE	D_{IN}

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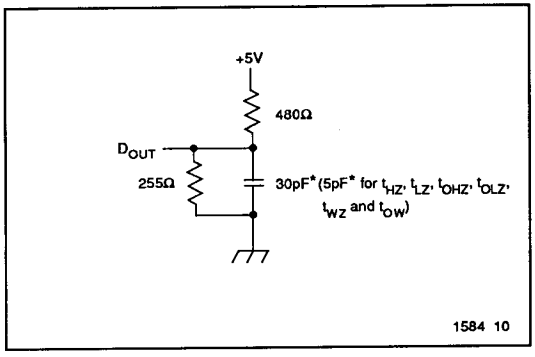

Figure 1. Output Load

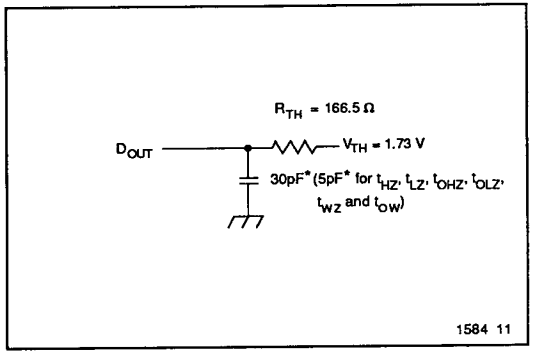

Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Due to the ultra-high speed of the PMC1632 and PMC1632L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{cc} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

Speed (ns)	Operating Range	Ordering Code	Package Type
17	Commercial 0°C – 70°C	PMC1632-17PZC PMC1632L-17PZC	PZ01 PZ01
20	Commercial 0°C – 70°C	PMC1632-20PZC PMC1632L-20PZC	PZ01 PZ01
25	Commercial 0°C – 70°C	PMC1632-25PZC PMC1632L-25PZC	PZ01 PZ01
35	Commercial 0°C – 70°C	PMC1632-35PZC PMC1632L-35PZC	PZ01 PZ01

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