# ::::Lattice®
::::: Semiconductor
::::: Corporation

# ispLSI® 2064E
## In-System Programmable SuperFAST™ High Density PLD

## Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 2000 PLD Gates
  - 64 I/O Pins, Four Dedicated Inputs
  - 64 Registers
  - High Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - 100% Functionally and JEDEC Upward Compatible with ispLSI 2064 Devices
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - $f_{max}$ = 200 MHz Maximum Operating Frequency
  - $t_{pd}$ = 4.5 ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - 5V Programmable Logic Core
  - ispJTAG™ In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port
  - User-Selectable 3.3V or 5V I/O Supports Mixed Voltage Systems
  - PCI Compatible Outputs
  - Open-Drain Output Option
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - Unused Product Term Shutdown Saves Power
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - Enhanced Pin Locking Capability
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Programmable Output Slew Rate Control to Minimize Switching Noise
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™
  - PC and UNIX Platforms

## Functional Block Diagram



0139/2064E
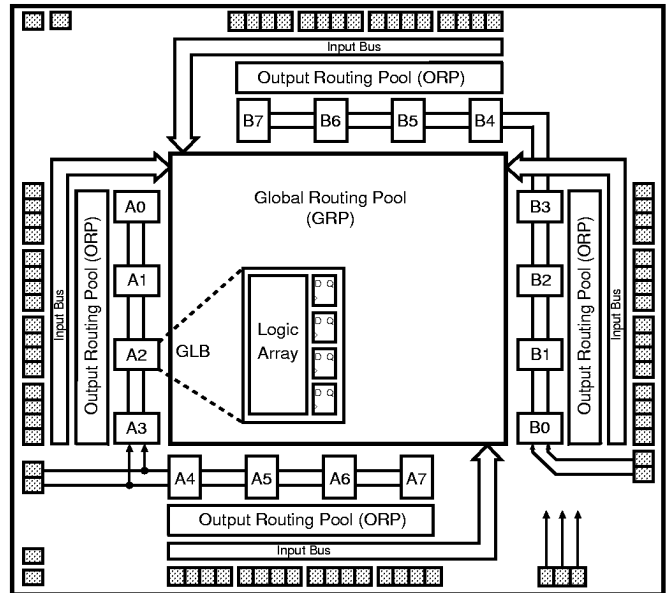
## Description

The ispLSI 2064E is a High Density Programmable Logic Device. The device contains 64 Registers, 64 Universal I/O pins, four Dedicated Input Pins, three Dedicated Clock Input Pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2064E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2064E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2064E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see Figure 1). There are a total of 16 GLBs in the ispLSI 2064E device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

## Functional Block Diagram

**Figure 1. ispLSI 2064E Functional Block Diagram**
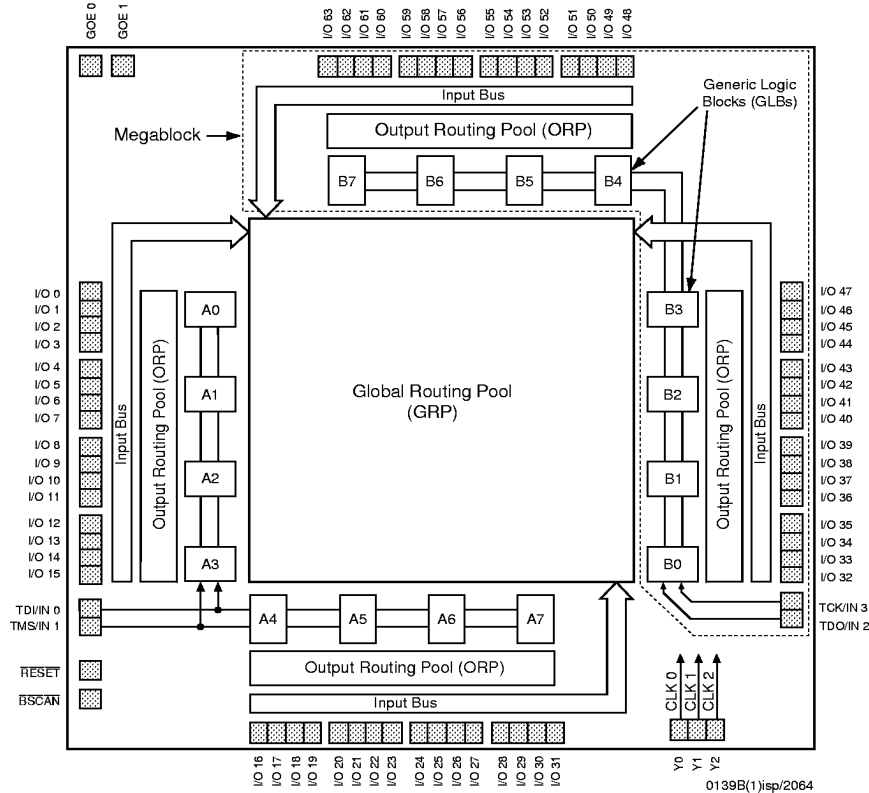
The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. By connecting the VCCIO pins to a common 5V or 3.3V power supply, I/O output levels can be matched to 5V or 3.3V compatible voltages. When connected to a 5V supply, the I/O pins provide PCI-compatible output drive.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by two ORPs. Each ispLSI 2064E device contains two Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2064E device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

### Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2064E are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispEXPERT software tools.

## Absolute Maximum Ratings [1]

Supply Voltage $V_{CC}$ ................................................. -0.5 to +7.0V

Input Voltage Applied .............................. -2.5 to $V_{CC}$ +1.0V

Off-State Output Voltage Applied ........... -2.5 to $V_{CC}$ +1.0V

Storage Temperature ..................................... -65 to 150°C

Case Temp. with Power Applied .................... -55 to 125°C

Max. Junction Temp. ($T_J$) with Power Applied ............ 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Condition

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage: Logic Core, Input Buffers $\quad T_A = 0°C$ to +70°C | | 4.75 | 5.25 | V |
| $V_{CCIO}$ | Supply Voltage: Output Drivers | 5V | 4.75 | 5.25 | V |
| | | 3.3V | 3.0 | 3.6 | V |
| $V_{IL}$ | Input Low Voltage | | 0 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$+1 | V |

Table 2-0005/2096E

## Capacitance (TA=25°C, f=1.0 MHz)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_1$ | Dedicated Input Capacitance | 8 | pf | $V_{CC}$ = 5.0V, $V_{IN}$ = 2.0V |
| $C_2$ | I/O Capacitance | 8 | pf | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |
| $C_3$ | Clock Capacitance | 10 | pf | $V_{CC}$ = 5.0V, $V_Y$ = 2.0V |

Table 2-0006/2064e

## Erase/Reprogram Specification

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| Erase/Reprogram Cycles | 10,000 | – | Cycles |

Table 2-0008/2064e

## Switching Test Conditions

| Input Pulse Levels | GND to 3.0V |
|---|---|
| Input Rise and Fall Time 10% to 90% | 1.5 ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure 2 |

Table 2-0003/2064E

3-state levels are measured 0.5V from steady-state active level.
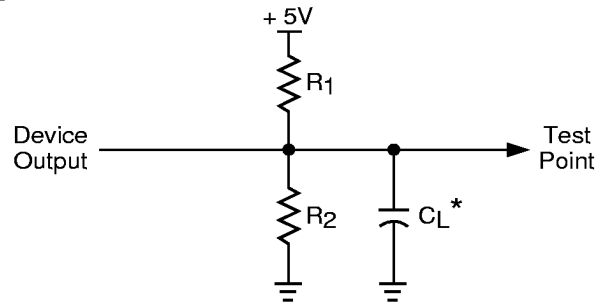
**Figure 2. Test Load**



*$C_L$ includes Test Fixture and Probe Capacitance.

### Output Load Conditions (see Figure 2)

| TEST CONDITION | | R1 | R2 | CL |
|---|---|---|---|---|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}$ -0.5V | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}$ +0.5V | 470Ω | 390Ω | 5pF |

Table 2-0004/2064

## DC Electrical Characteristics

### Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8 mA | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4 mA | 2.4 | – | – | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{IL}$ (Max.) | – | – | -10 | μA |
| $I_{IH}$ | Input or I/O High Leakage Current | ($V_{CCIO}$ - 0.2)V ≤ $V_{IN}$ ≤ $V_{CCIO}$ | – | – | 10 | μA |
| | | $V_{CCIO}$ ≤ $V_{IN}$ ≤ 5.25V | – | – | 10 | μA |
| $I_{IL-PU}$ | I/O Active Pull-Up Current | 0V ≤ $V_{IN}$ ≤ 2.0V | -10 | – | -250 | μA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CCIO}$ = 5.0V or 3.3V, $V_{OUT}$ = 0.5V | – | – | -240 | mA |
| $I_{CC}$[2,4,5] | Operating Power Supply Current | $V_{IL}$ = 0.0V, $V_{IH}$ = 3.0V  $f_{TOGGLE}$ = 1 MHz | – | 100 | – | mA |

Table 2-0007/2064E

1. One output at a time for a maximum duration of one second. $V_{OUT}$ = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at $V_{CC}$ = 5V and $T_A$ = 25°C.
4. Unused inputs held at 0.0V.
5. Maximum $I_{CC}$ varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum $I_{CC}$.

## External Timing Parameters

### Over Recommended Operating Conditions

| PARAMETER | TEST COND.[4] | #[2] | DESCRIPTION[1] | -200 | | -135 | | -100 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd1}$ | A | 1 | Data Prop Delay, 4PT Bypass, ORP Bypass | – | 4.5 | – | 7.5 | – | 10.0 | ns |
| $t_{pd2}$ | A | 2 | Data Prop Delay | – | 7.0 | – | 10.0 | – | 13.0 | ns |
| $f_{max}$ | A | 3 | Clk Freq with Internal Feedback[3] | 200 | – | 135 | – | 100 | – | MHz |
| $f_{max}$ (Ext.) | – | 4 | Clk Freq with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$ | 133 | – | 100 | – | 77 | – | MHz |
| $f_{max}$ (Tog.) | – | 5 | Clk Frequency, Max. Toggle | 200 | – | 143 | – | 100 | – | MHz |
| $t_{su1}$ | – | 6 | GLB Reg Setup Time before Clk, 4 PT Bypass | 3.5 | – | 5.0 | – | 6.5 | – | ns |
| $t_{co1}$ | A | 7 | GLB Reg Clk to Output Delay, ORP Bypass | – | 3.0 | – | 4.0 | – | 5.0 | ns |
| $t_{h1}$ | – | 8 | GLB Reg Hold Time after Clk, 4 PT Bypass | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{su2}$ | – | 9 | GLB Reg Setup Time before Clk | 4.5 | – | 6.0 | – | 8.0 | – | ns |
| $t_{co2}$ | – | 10 | GLB Reg Clk to Output Delay | – | 3.5 | – | 4.5 | – | 6.0 | ns |
| $t_{h2}$ | – | 11 | GLB Reg Hold Time after Clk | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| $t_{r1}$ | A | 12 | External Reset Pin to Output Delay | – | 6.0 | – | 10.0 | – | 13.5 | ns |
| $t_{rw1}$ | – | 13 | External Reset Pulse Duration | 3.5 | – | 5.0 | – | 6.5 | – | ns |
| $t_{ptoeen}$ | B | 14 | Input to Output Enable | – | 8.0 | – | 12.0 | – | 15.0 | ns |
| $t_{ptoedis}$ | C | 15 | Input to Output Disable | – | 8.0 | – | 12.0 | – | 15.0 | ns |
| $t_{goeen}$ | B | 16 | Global OE Output Enable | – | 4.0 | – | 7.0 | – | 9.0 | ns |
| $t_{goedis}$ | C | 17 | Global OE Output Disable | – | 4.0 | – | 7.0 | – | 9.0 | ns |
| $t_{wh}$ | – | 18 | External Synch Clk Pulse Duration, High | 2.5 | – | 3.5 | – | 5.0 | – | ns |
| $t_{wl}$ | – | 19 | External Synch Clk Pulse Duration, Low | 2.5 | – | 3.5 | – | 5.0 | – | ns |

Table 2-0030A/2064E

1. Unless noted otherwise, all parameters use a GRP load of four GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

## Internal Timing Parameters[1]

### Over Recommended Operating Conditions

| PARAMETER | #[2] | DESCRIPTION | -200 | | -135 | | -100 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| **Inputs** | | | | | | | | | |
| $t_{io}$ | 20 | Input Buffer Delay | – | 0.5 | – | 0.5 | – | 0.5 | ns |
| $t_{din}$ | 21 | Dedicated Input Delay | – | 1.1 | – | 1.7 | – | 2.2 | ns |
| **GRP** | | | | | | | | | |
| $t_{grp}$ | 22 | GRP Delay | – | 0.6 | – | 1.2 | – | 1.7 | ns |
| **GLB** | | | | | | | | | |
| $t_{4ptbpc}$ | 23 | 4 Product Term Bypass Path Delay (Combinatorial) | – | 1.4 | – | 3.7 | – | 5.8 | ns |
| $t_{4ptbpr}$ | 24 | 4 Product Term Bypass Path Delay (Registered) | – | 1.9 | – | 4.2 | – | 5.8 | ns |
| $t_{1ptxor}$ | 25 | 1 Product Term/XOR Path Delay | – | 2.9 | – | 5.2 | – | 6.8 | ns |
| $t_{20ptxor}$ | 26 | 20 Product Term/XOR Path Delay | – | 2.9 | – | 5.2 | – | 7.3 | ns |
| $t_{xoradj}$ | 27 | XOR Adjacent Path Delay[3] | – | 2.9 | – | 5.2 | – | 8.0 | ns |
| $t_{gbp}$ | 28 | GLB Register Bypass Delay | – | 0.5 | – | 0.5 | – | 0.5 | ns |
| $t_{gsu}$ | 29 | GLB Register Setup Time before Clock | 1.2 | – | 0.7 | – | 1.2 | – | ns |
| $t_{gh}$ | 30 | GLB Register Hold Time after Clock | 2.3 | – | 4.3 | – | 4.0 | – | ns |
| $t_{gco}$ | 31 | GLB Register Clock to Output Delay | – | 0.3 | – | 0.3 | – | 0.3 | ns |
| $t_{gro}$ | 32 | GLB Register Reset to Output Delay | – | 0.6 | – | 1.1 | – | 1.3 | ns |
| $t_{ptre}$ | 33 | GLB Product Term Reset to Register Delay | – | 4.3 | – | 6.0 | – | 6.1 | ns |
| $t_{ptoe}$ | 34 | GLB Product Term Output Enable to I/O Cell Delay | – | 4.9 | – | 6.9 | – | 8.6 | ns |
| $t_{ptck}$ | 35 | GLB Product Term Clock Delay | 1.0 | 4.0 | 2.5 | 5.5 | 4.1 | 7.1 | ns |
| **ORP** | | | | | | | | | |
| $t_{orp}$ | 36 | ORP Delay | – | 0.9 | – | 1.0 | – | 1.4 | ns |
| $t_{orpbp}$ | 37 | ORP Bypass Delay | – | 0.4 | – | 0.5 | – | 0.4 | ns |
| **Outputs** | | | | | | | | | |
| $t_{ob}$ | 38 | Output Buffer Delay | – | 1.6 | – | 1.6 | – | 1.6 | ns |
| $t_{sl}$ | 39 | Output Slew Limited Delay Adder | – | 1.5 | – | 1.5 | – | 1.0 | ns |
| $t_{oen}$ | 40 | I/O Cell OE to Output Enabled | – | 2.0 | – | 3.4 | – | 4.2 | ns |
| $t_{odis}$ | 41 | I/O Cell OE to Output Disabled | – | 2.0 | – | 3.4 | – | 4.2 | ns |
| $t_{goe}$ | 42 | Global Output Enable | – | 2.0 | – | 3.6 | – | 4.8 | ns |
| **Clocks** | | | | | | | | | |
| $t_{gy0}$ | 43 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 0.7 | 0.7 | 1.6 | 1.6 | 2.7 | 2.7 | ns |
| $t_{gy1/2}$ | 44 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 0.9 | 0.9 | 1.8 | 1.8 | 2.7 | 2.7 | ns |
| **Global Reset** | | | | | | | | | |
| $t_{gr}$ | 45 | Global Reset to GLB | – | 3.4 | – | 6.3 | – | 9.2 | ns |

Table 2-0036A/2064E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

## ispLSI 2064E Timing Model



0491/2064
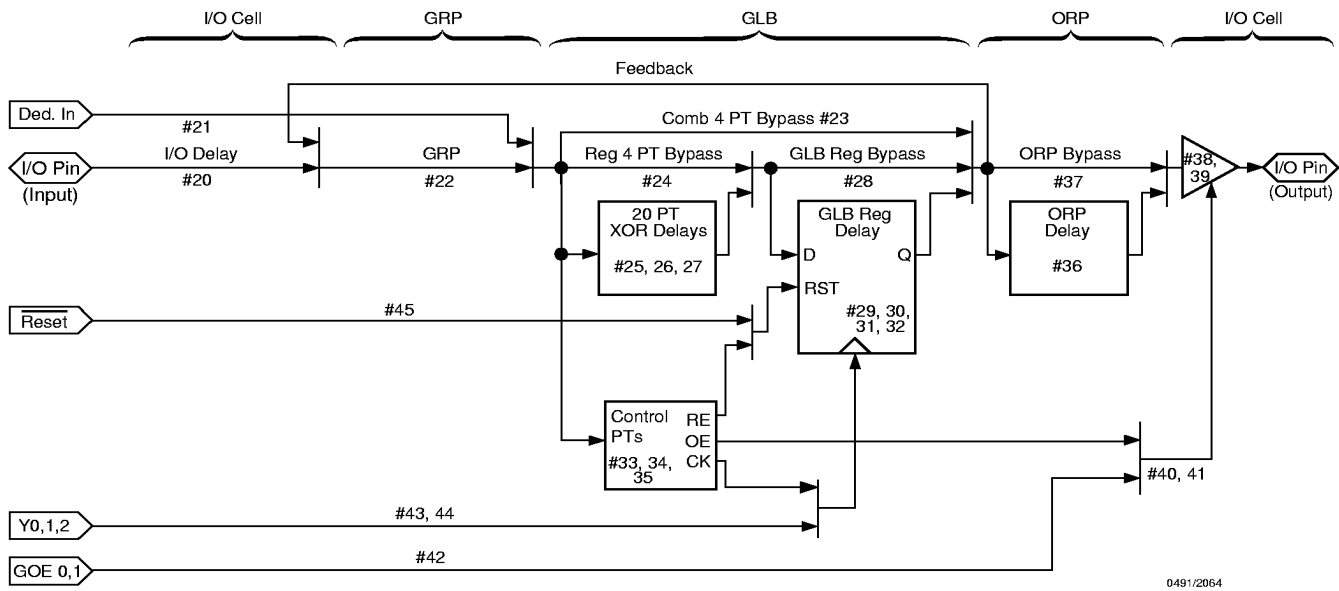
### Derivations of tsu, th and tco from the Product Term Clock

tsu  = Logic + Reg su - Clock (min)
  = (tio + tgrp + t20ptxor) + (tgsu) - (tio + tgrp + tptck(min))
  = (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
3.1ns = (0.5 + 0.6 + 2.9) + (1.2) - (0.5 + 0.6 + 1.0)

th  = Clock (max) + Reg h - Logic
  = (tio + tgrp + tptck(max)) + (tgh) - (tio + tgrp + t20ptxor)
  = (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
3.4ns = (0.5 + 0.6 + 4.0) + (2.3) - (0.5 + 0.6 + 2.9)

tco  = Clock (max) + Reg co + Output
  = (tio + tgrp + tptck(max)) + (tgco) + (torp + tob)
  = (#20 + #22 + #35) + (#31) + (#36 + #38)
7.9ns = (0.5 + 0.6 + 4.0) + (0.3) + (0.9 + 1.6)

Table 2- 0042A-2064e

Note: Calculations are based upon timing specifications for the ispLSI 2064E-200L.

## Power Consumption

Power consumption in the ispLSI 2064E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used.

Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**
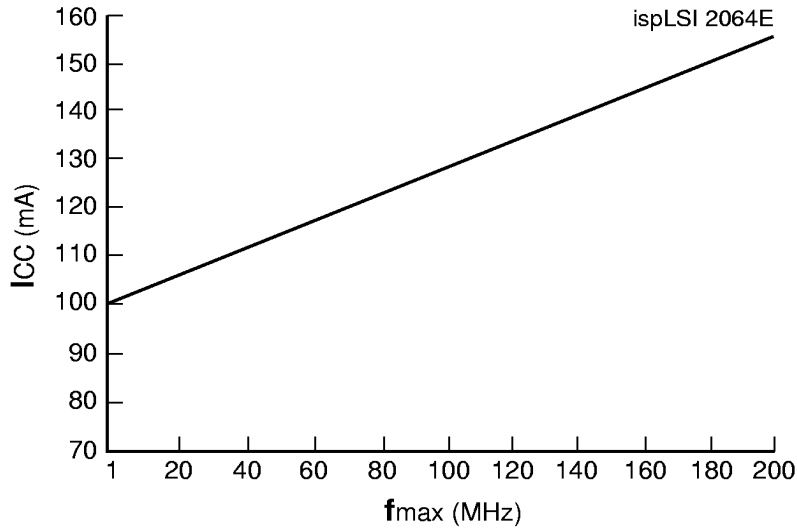


Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25° C

$I_{CC}$ can be estimated for the ispLSI 2064E using the following equation:

$I_{CC}$(mA) = 7 + (# of PTs * 0.75) + (# of nets * Max freq * 0.004)

Where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The $I_{CC}$ estimate is based on typical conditions ($V_{CC}$ = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of $I_{CC}$ is sensitive to operating conditions and the program in the device, the actual $I_{CC}$ should be verified.
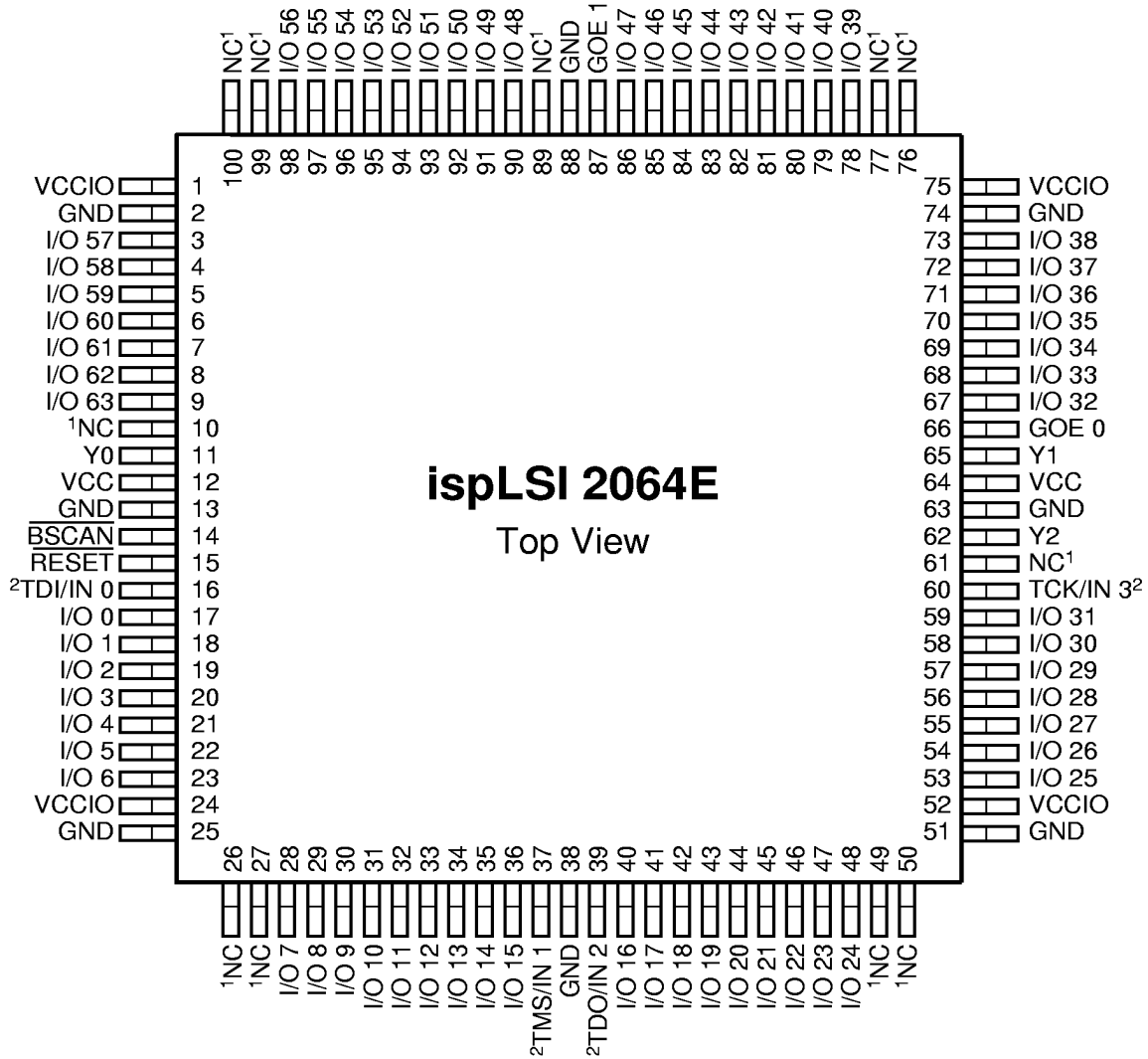
0127A/2064E

## Pin Description

| NAME | TQFP PIN NUMBERS | | | | DESCRIPTION |
|---|---|---|---|---|---|
| I/O 0 - I/O 3 | 17, | 18, | 19, | 20, | Input/Output Pins - These are the general purpose I/O pins used by the logic array. |
| I/O 4 - I/O 7 | 21, | 22, | 23, | 28, | |
| I/O 8 - I/O 11 | 29, | 30, | 31, | 32, | |
| I/O 12 - I/O 15 | 33, | 34, | 35, | 36, | |
| I/O 16 - I/O 19 | 40, | 41, | 42, | 43, | |
| I/O 20 - I/O 23 | 44, | 45, | 46, | 47, | |
| I/O 24 - I/O 27 | 48, | 53, | 54, | 55, | |
| I/O 28 - I/O 31 | 56, | 57, | 58, | 59, | |
| I/O 32 - I/O 35 | 67, | 68, | 69, | 70, | |
| I/O 36 - I/O 39 | 71, | 72, | 73, | 78, | |
| I/O 40 - I/O 43 | 79, | 80, | 81, | 82, | |
| I/O 44 - I/O 47 | 83, | 84, | 85, | 86, | |
| I/O 48 - I/O 51 | 90, | 91, | 92, | 93, | |
| I/O 52 - I/O 55 | 94, | 95, | 96, | 97, | |
| I/O 56 - I/O 59 | 98, | 3, | 4, | 5, | |
| I/O 60 - I/O 63 | 6, | 7, | 8, | 9 | |
| GOE 0, GOE 1 | 66, | 87 | | | Global Output Enable input pins. |
| Y0, Y1, Y2 | 11, | 65, | 62 | | Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device. |
| $\overline{\text{RESET}}$ | 15 | | | | Active Low (0) Reset pin which resets all of the registers in the device. |
| $\overline{\text{BSCAN}}$ | 14 | | | | Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK options become active. |
| TDI/IN 0[2] | 16 | | | | Input - This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an input pin to load programming data into the device. TDI/IN0 also is used as one of the two control pins for the JTAG state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin. |
| TMS/IN 1[2] | 37 | | | | Input - This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a pin to control the operation of the JTAG state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin. |
| TDO/IN 2[2] | 39 | | | | Output/Input - This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin. |
| TCK/IN 3[2] | 60 | | | | Input - This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin. |
| GND | 2, | 13, | 25, | 38, | Ground (GND) |
| | 51, | 63, | 74, | 88 | |
| VCC | 12, | 64 | | | $V_{CC}$ |
| VCCIO | 1, | 24, | 52, | 75 | Supply voltage for output drivers, 5V or 3.3V. All VCCIO pins must be connected to the same voltage level. |
| NC[1] | 10, | 26, | 27, | 49, | No Connect. |
| | 50, | 61, | 76, | 77, | |
| | 89, | 99, | 100 | | |

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.
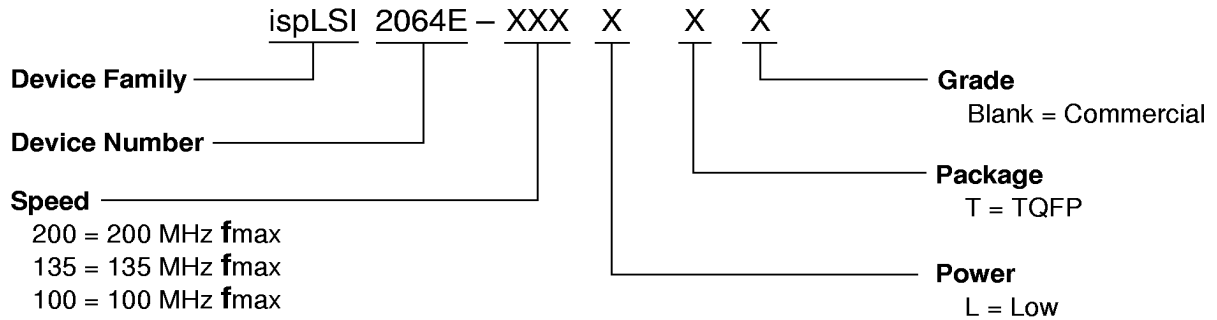
Table 2-0002-2064E.eps

## Pin Configuration

**ispLSI 2064E 100-Pin TQFP Pinout Diagram**



Top pins (left to right, 100–76):
NC[1], NC[1], I/O 56, I/O 55, I/O 54, I/O 53, I/O 52, I/O 51, I/O 50, I/O 49, I/O 48, NC[1], GND, GOE 1, I/O 47, I/O 46, I/O 45, I/O 44, I/O 43, I/O 42, I/O 41, I/O 40, I/O 39, NC[1], NC[1]

Left side (pins 1–25):
1 VCCIO
2 GND
3 I/O 57
4 I/O 58
5 I/O 59
6 I/O 60
7 I/O 61
8 I/O 62
9 I/O 63
10 [1]NC
11 Y0
12 VCC
13 GND
14 BSCAN
15 RESET
16 [2]TDI/IN 0
17 I/O 0
18 I/O 1
19 I/O 2
20 I/O 3
21 I/O 4
22 I/O 5
23 I/O 6
24 VCCIO
25 GND

Right side (pins 75–51):
75 VCCIO
74 GND
73 I/O 38
72 I/O 37
71 I/O 36
70 I/O 35
69 I/O 34
68 I/O 33
67 I/O 32
66 GOE 0
65 Y1
64 VCC
63 GND
62 Y2
61 NC[1]
60 TCK/IN 3[2]
59 I/O 31
58 I/O 30
57 I/O 29
56 I/O 28
55 I/O 27
54 I/O 26
53 I/O 25
52 VCCIO
51 GND

Center: **ispLSI 2064E** Top View

Bottom pins (left to right, 26–50):
[1]NC, [1]NC, I/O 7, I/O 8, I/O 9, I/O 10, I/O 11, I/O 12, I/O 13, I/O 14, I/O 15, [2]TMS/IN 1, GND, [2]TDO/IN 2, I/O 16, I/O 17, I/O 18, I/O 19, I/O 20, I/O 21, I/O 22, I/O 23, I/O 24, [1]NC, [1]NC

0766A-2064E

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

## Part Number Description

ispLSI 2064E – XXX   X   X   X

Device Family

Device Number

**Speed**
200 = 200 MHz $f_{max}$
135 = 135 MHz $f_{max}$
100 = 100 MHz $f_{max}$

**Grade**
Blank = Commercial

**Package**
T = TQFP

**Power**
L = Low

0212/2064E

## ispLSI 2064E Ordering Information

### COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|---|---|---|---|---|
| ispLSI | 200 | 4.5 | ispLSI 2064E-200LT | 100-Pin TQFP |
| | 135 | 7.5 | ispLSI 2064E-135LT | 100-Pin TQFP |
| | 100 | 10 | ispLSI 2064E-100LT | 100-Pin TQFP |

Table 2-0041A/2064E