Integrated
Circuit
Systems, Inc.

ICS9178-02

245 MHz Clock Generator and Integrated Buffer for PowerPC™

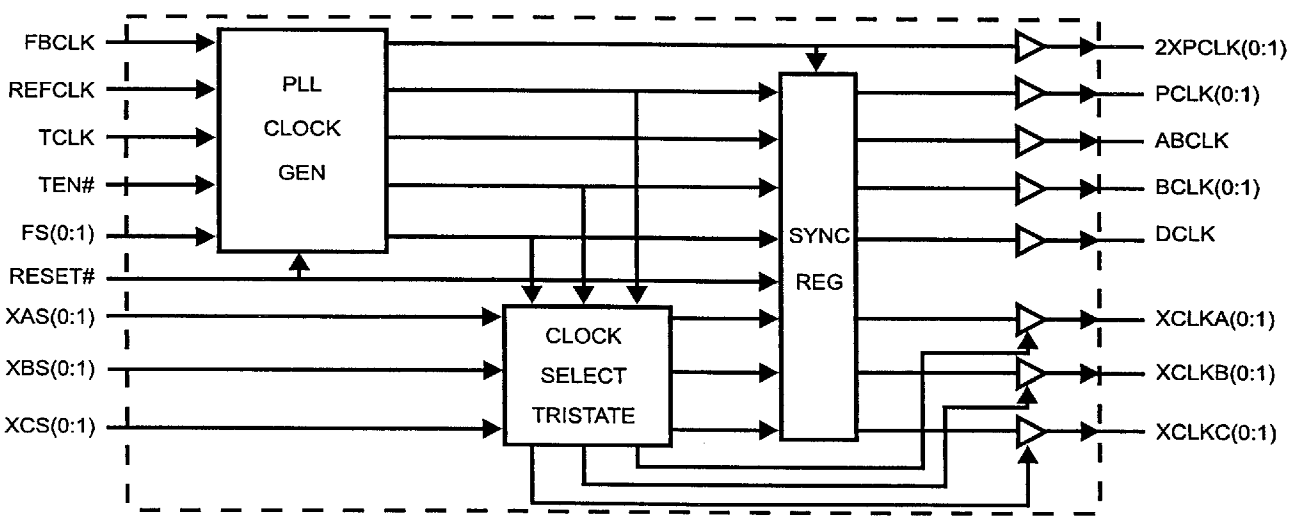
General Description

The **ICS9178-02** generates all clocks required for high speed PowerPC RISC microprocessor systems. Generating clocks in phase with an external reference frequency allows the **ICS9178-02** to be used as a multiplying zero delay buffer. Three different multiplying factors are externally selectable. These factors can be customized for specific applications. An external frequency can be directly applied to aid system testing. With 2X processor clock speeds up to 240 MHz, PECL outputs are provided. User selectable frequency ratios are available for PCLK/BCLK and PCLK/XCLK. Each pair of clocks outputs have separate supply pins to minimize output jitter and allow them to operate at 5V, 3.3V or custom voltage levels.

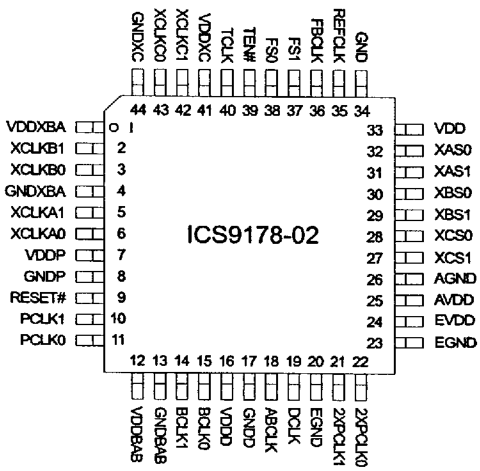
Features

- Generates 2 PECL 2x processor, 2 TTL/CMOS 1x processor and 10 selectable bus clocks
- 2XPCLK ranges from 75 MHz to 245 MHz (5V or 5V/3.3V mixed supply) or 60 to 170 MHz (3.3V only)
- Asymmetric duty cycle bus clock for PowerPC
- Bus to processor clock skews less than ±250ps
- 2XPCLK to PCLK skew controlled at 500 ±300ps
- Selectable reference multiplying factors
- Selectable PCLK/BCLK and PCLK/XCLK ratios
- Separate supplies allow 5V and 3.3V output mix
- 3.0V - 5.5V supply range
- 44-pin PQFP package

Block Diagram



Pin Configuration



44-Pin PQFP

*VCO range is limited from 75- 245 MHz at 5V ±5% and 60 - 170 MHz at 3.3V ±5%. Divide ratios assume BCLK is externally fed back to FBCLK.

Rising edge of ABCLK is coincident with rising edges of 2XPCLK, PCLK and other BCLKs.

X_S1	X_S0	XCLK_(0,1)
0	0	PCLK
0	1	BCLK
1	0	DCLK
1	1	Tristate

_=A,B,C

Functionality

FS1	FS0	RST#	TEN	*VCO	2XPCLK	PCLK	ABCLK (H/L%)	BCLK	DCLK
0	0	1	0	6x REF	VCO	VCO/2	VCO/6 (66/33)	VCO/6	VCO/12
0	1	1	0	8x REF	VCO	VCO/2	VCO/8 (75/25)	VCO/8	VCO/16
1	0	1	0	12x REF	VCO	VCO/2	VCO/12 (66/33)	VCO/12	VCO/24
1	1	1	0	X	1	1	1	1	1
X	X	0	X	X	0	0	0	0	0
0	0	1	1	TCLK	TCLK	TCLK/2	TCLK/6 (66/33)	TCLK/6	TCLK/12
0	1	1	1	TCLK	TCLK	TCLK/2	TCLK/8 (75/25)	TCLK/8	TCLK/16
1	0	1	1	TCLK	TCLK	TCLK/2	TCLK/12 (66/33)	TCLK/12	TCLK/24
1	1	1	1	TCLK	TCLK	TCLK/2	TCLK/2	TCLK/2	TCLK/2

Note: The 2XPCLK series or Thevinen trace terminations must be optimized for the specific operating frequency and board layout. The rising edge of ABCLK is coincident with the rising edges of 2XPCLK, PCLK and other BCLKs.

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
32	XAS0	Input	LSB Programmable Group A frequency selector.
31	XAS1	Input	MSB Programmable Group A frequency selector.
6	XCLKA0	Output	TTL/CMOS group A programmable clock output.
5	XCLKA1	Output	TTL/CMOS group A programmable clock output.
30	XBS0	Input	LSB Programmable Group B frequency selector.
29	XBS1	Input	MSB Programmable Group B frequency selector.
3	XCLKB0	Output	TTL/CMOS Group B programmable clock output.
2	XCLKB1	Output	TTL/CMOS Group B programmable clock output.
1	VDDXBA	—	Power for programmable Gr oup A and B buffers (Pins 2, 3, 5, 6).
4	GNDXBA	—	Ground for programmable Group A and B buffers (Pins 2, 3, 5, 6).
44	GNDXC	—	Ground for the programmable Group C buffers (Pins 42 and 43).
43	XCLKC0	Output	TTL/CMOS Group C programmable clock output.
42	XCLKC1	Output	TTL/CMOS Group C programmable clock output.
41	VDDXC	—	Power for the XC signal output buffers (Pins 42 and 43).
28	XCS0	Input	LSB Programmable Group C frequency selector.
27	XCS1	Input	MSB Programmable Group C frequency selector.
11	PCLK0	Output	TTL/CMOS 1X Processor clock output.
10	PCLK1	Output	TTL/CMOS 1X Processor clock output.
8	GNDP	—	Ground for PCLK output buffers (Pins 11 and 10).
7	VDDP	—	Power for PCLK output buffers (Pins 11 and 10).
22	2XPCLK0	Output	PECL 2X Processor clock output.
21	2XPCLK1	Output	PECL 2X Processor clock output.
24	EVDD	—	Power for PECL buffers (Pins 21 and 22).
23	EGND	—	Ground for PECL buffers (Pins 21 and 22).
20	EGND	—	Ground for PECL buffers (Pins 21 and 22).
38*	FS0	Input	LSB frequency select PLL (divider mode control).
37*	FS1	Input	MSB frequency select PLL (divider mode control).
36	FBCLK	Input	External PLL feedback path from one of the BCLK outputs.
35	REFCLK	Input	External reference clock input.
25	AVDD	—	Power for the analog PLL circuitry.
26	AGND	—	Ground for the analog PLL circuitry.
19	DCLK	Output	TTL/CMOS D clock output.
16	VDDD	—	Power for D output buffers (Pin 19).
17	GNDD	—	Ground for D output buffer (Pin 19).
15	BCLK0	Output	TTL/CMOS B (Bus) clock output.
14	BCLK1	Output	TTL/CMOS B (Bus) clock output.
13	GNDBAB	—	Ground for output buffers AB and B clocks (Pins 14, 15 & 18).
12	VDDBAB	—	Power for output buffers AB and B clocks (Pins 14, 15 & 18).
18	ABCLK	Output	TTL/CMOS AB Bus clock (has Asymmetric duty cycle).
40	TCLK	Input	External test clock input.
39	TEN#	Input	Test enable (tie low).
9	RESET#	Input	Sync register reset (active low).
33	VDD	—	Digital power supply for 5.0 or 3.3V.
34	GND	—	Digital ground supply.

*=Pin is pulled-up to VDD internally by the device.

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias. . . . . 0°C to +70°C
Storage temperature . . . . -65°C to +150°C
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Power dissipation . . . . 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

Device Specifications

Maximum Ratings				
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Supply voltage relative to GND	VDD	-0.5	7.0	V
Input voltage with respect to GND	V_{IN}	-0.5	VDD +0.5	V
Operating temperature	T_{OPER}	0	+70	°C
Storage temperature	T_{STOR}	-65	+150	°C
Max soldering temperature (10 sec)	T_{SOL}		+260	°C
Junction temperature	T_J		+135	°C
Package power dissipation	P_{DISS}	800	900	mWatts

DC Characteristics

VDD =+5V ±5%, 0°C ≥ TAMBIENT ≥ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High level input voltage	V_{IH}		2.0			V
Low level input voltage	V_{IL}				0.8	V
High level CMOS output voltage	V_{OH}	I_{OH}=-25mA	2.4			V
Low level CMOS output voltage	V_{OL}	I_{OL}=25mA			0.4	V
High level PECL output voltage (2XPCLK)	V_{OHP}	110 ohm load to ground	1.9	2.2		V
Low level PECL output voltage (2XPCLK)	V_{OLP}	110 ohm load to ground		0.3	0.5	V
Input high current	I_{IH}	V_{IH}=VDD	-10		10	µA
Input low current (MSX pins, pull-up)	I_{IL1}	V_{IL}=0V			-150	µA
Input low current (other inputs)	I_{IL2}	V_{IL}=0V	-10		10	µA
Output leakage current (XCLKs)	I_{OZ}	(tristate)	-10		10	µA
Power supply current	I_{DD}	@240 MHz on 2XPCLK		145	185	mA
Power supply current (typical) (Note 1)	I_{DD-TYP}	@75 MHz on 2XPCLK		80	100	mA
Input capacitance (Note 1)	C_{IN}				8	pF

Note 1: Parameter is guaranteed by design and characterization. Not tested 100% in production.

AC Characteristics

V_{DD} =+5V ±5%, 0°C ≥ TAMBIENT ≥ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Frequency (Note 1)	f		8	40.0	50.0	MHz
Input Clock Rise time (Note 1)	t_{CLKr}		-	-	3	ns
Input Clock Fall time (Note 1)	t_{CLKf}		-	-	3	ns
Output Frequency (2XPCLK)	f_{2XPCLK}	6X mode	75		245	MHz
Output Frequency (2XPCLK)	f_{2XPCLK}	8X mode	75	-	250	Mhz
Output Frequency (2XPCLK)	f_{2XPCLK}	12X mode	75	-	245	Mhz
Output Rise time, 0.8 to 2.0V (Note 1)	$t_{r2XPCLK}$	15pF load 0.8 to 2.0V	-	-	1.0	ns
		20% to 80%	-	-	1.5	ns
Fall time 2.0 to 0.8 80% to 20% (Note 1)	$t_{f2XPCLK}$	15pF load 2.0 to 0.8V	-	-	1.0	ns
		80% to 20%	-	-	1.5	ns
Output Rise time 80% to 20% (Note 1)	$t_{(TTL)r}$	15pF load	-	-	3.0	ns
Output Fall time 80% to 20% (Note 1)	$t_{(TTL)f}$	15pF load	-	-	2.0	ns
Duty cycle 2XPCLK (Note 1)	d_1	200 to 240 MHz @ 1.4V 110 ohm, 15pF load	42.5	50	57.5	%
Pulse Width, High, 2XPCLK (Note 1, 2)	T_{pwH}	@ 1.8V, 110Ω Load ²	1.2	-	-	ns
Pulse Width, Low, 2XPCLK (Note 1, 2)	T_{pwL}	@ 0.6V, 110Ω Load ²	1.0	-	-	ns
Duty cycle ABCLK (Note 1)	d_3	15pF load @ 1.4V (8X mode)	70	75	80	%
Duty cycle ABCLK (Note 1)	d_4	15pF load @ 1.4V (6X and 12X mode)	61	66	71	%
Duty cycle TTL (other clocks) (Note 1)	d_{t5}	15pF load @ 1.4V	45	50	55	%
Jitter 1 Sigma 2XPCLK (10,000 samples) (Note 1)	T_{j1s1}	for 200 to 240 MHz on 2XPCLK	-	40	-	ps
Jitter 1 Sigma 1XPCLK B & D (10,000 samples) (Note 1)	T_{j1s2}	for 200 to 240 MHz on 2XPCLK	-	50	-	ps
Jitter 1 Sigma AB clock (10,000 samples) (Note 1)	T_{j1s3}	for 200 to 240 MHz on 2XPCLK	-	60	-	ps
Jitter Absolute 2XPCLK (Note 1)	T_{jabs1}	for 200 to 240 MHz on 2XPCLK	-150	80	+150	ps
Jitter Absolute 1XPCLK, B, D clocks (Note 1)	T_{jabs2}	for 200 to 240 MHz on 2XPCLK	-200	110	+200	ps
Jitter Absolute AB clock (Note 1)	T_{jabs3}	for 200 to 240 MHz on 2XPCLK	-250	120	+250	ps

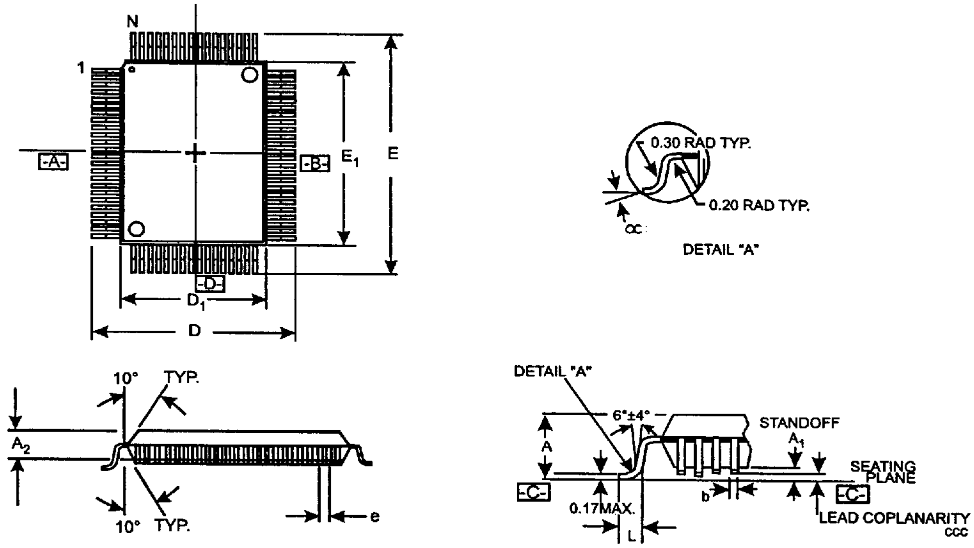
Note 1: Parameter is guaranteed by design and characterization. Not tested 100% in production.
Note 2: For 70Ω Load, 2XPCLK level may be pulled-up with a 390 Ω resistor to meet minimum pulse width requirements at both 1.8V and 0.6V at 240 MHz.

AC Characteristics (continued)

V_{DD} =+5V ±5%, 0°C ≥ TAMBIENT ≥ +70°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Jitter Absolute 2XPCLK (Note 1)	T_{jabs4}	for 200 to 240 MHz on 2XPCLK at VDD 4.9 to 5.2V	-125	80	+125	ps
Jitter Absolute 1XPCLK, B, D clocks (Note 1)	T_{jabs5}	for 200 to 240 MHz on 2XPCLK at VDD 4.9 to 5.2V	-160	110	+160	ps
Jitter Absolute 2XPCLK (Note 1)	T_{jabs6}	for 200 MHz on 2XPCLK	-200	-	+200	ps
Jitter Absolute 1XPCLK (Note 1)	T_{jabs7}	for 200 MHz on 2XPCLK	-250	-	+250	ps
Jitter Absolute AB clock (Note 1)	T_{jabs8}	for 200 MHz on 2XPCLK	-300	-	+300	ps
Skew, output to output (P, B, D and AB) (Note 1)	T_{skew1}	@ 1.4V	-250	-	+250	ps
Skew, Feedback CLK to REFCLK Input (Feedback is earlier than REF) (Note 1)	T_{skew2}	@ 1.4V	-350	-125	+100	ps
Skew, 2XPCLK to PCLK (2XPCLK is later than PCLK) (Note 1)	T_{skew3}	@ 1.4V	+200	500	+800	ps
Skew, REFCLK to PCLK (REF is later than P) (Note 1)	Tskew4	@ 1.4V	0	+250	+500	ps

Note 1: Parameter is guaranteed by design and characterization. Not tested 100% in production.
Note 2: For 70 Ω Load, 2XPCLK level may be pulled-up with a 390 Ω resistor to meet minimum pulse width requirements at both 1.8Vand 0.6Vat 240 Mhz.



PLCC Package

LEAD COUNT		44L
BODY THICKNESS		2.0
FOOTPRINT (BODY+)		3.20
DIMENSIONS	TOLERANCE	
A	MAX.	2.45
A1	MAX.	0.25
A2	±0.10	2.00
D	±0.25	13.20
D1	±0.10	10.0
E	±0.25	13.20
E1	±0.10	10.0
L	±0.15/-0.10	0.70
e	BASIC	0.80
b	+0.05	0.35
ccc	MAX.	0.10
α		0° - 7°

Ordering Information
ICS9178-02CY44

Example:

ICS XXXX-PPP M X#W

- **Lead Count & Package Width**
  Lead Count=1, 2 or 3 digits
  W=.3" SOIC or .6" DIP; None=Standard Width
- **Package Type**
  Y=QFP
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device; GSP=Genlock