
HM658512AI Series

4 M PSRAM (512-kword $\times$ 8-bit)
2 k Refresh

HITACHI

ADE-203-286C(Z)
Rev. 3.0
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Description

The Hitachi HM658512AI is a 4-Mbit pseudo static RAM organized 524288-word $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μ m Hi-CMOS process technology. It offers low power data retention by self refresh mode. HM658512AI is suitable for handy systems which work with battery back-up systems. It is packaged in 32-pin plastic SOP.

Features

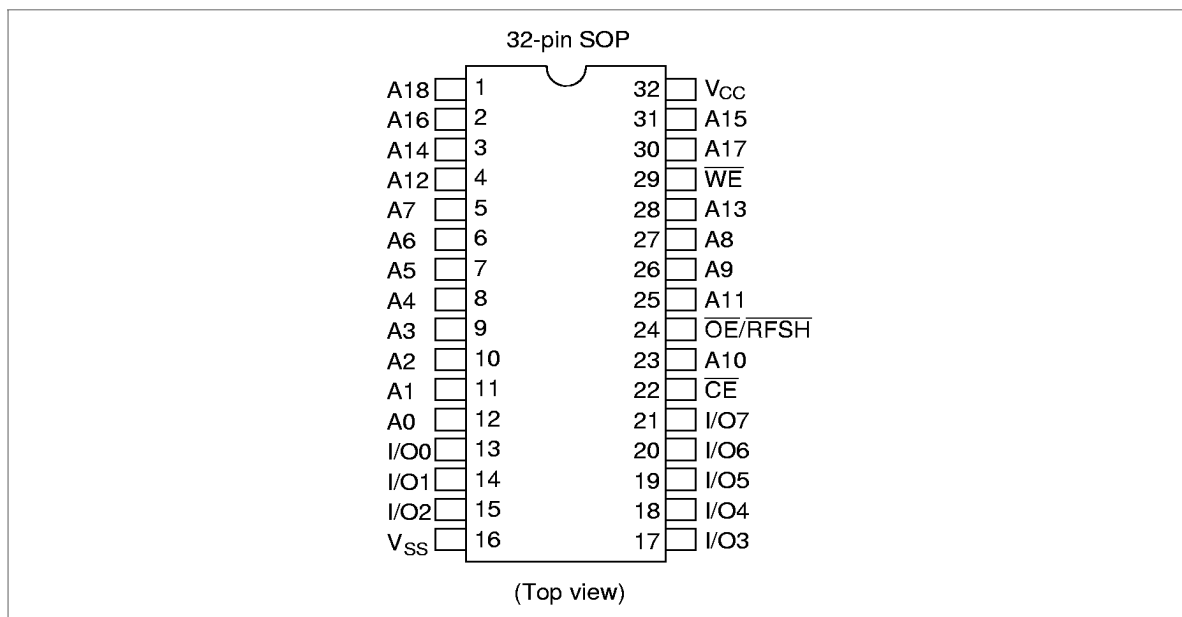
- Single 5 V supply: 5 V $\pm$ 10%
- High speed
 - $\overline{\text{CE}}$ access time: 80 ns/100 ns/120 ns (max)
 - Random read/write cycle time: 130 ns/160 ns/190 ns (min)
- Power dissipation
 - Active: 250 mW (typ)
 - Standby: 350 μ W (typ)
- Directly TTL compatible all inputs and outputs
- Simple address configuration
 - Non multiplexed address
- Refresh cycle
 - 2048 refresh cycles: 32 ms
- Easy refresh functions
 - Address refresh
 - Automatic refresh
 - Self refresh
- Temperature range: -40 to $+85^{\circ}\text{C}$

HM658512AI Series

Ordering Information

Type No.	Access time	Package
HM658512ALFPI-8	80 ns	525-mil 32-pin plastic SOP (FP-32D)
HM658512ALFPI-10	100 ns	
HM658512ALFPI-12	120 ns	
HM658512ALFPI-8V	80 ns	
HM658512ALFPI-10V	100 ns	
HM658512ALFPI-12V	120 ns	

Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CE	Chip enable
OE/RFSH	Output enable/Refresh
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Notes

Refresh

There are three refresh modes : address refresh, automatic refresh and self refresh.

- (1) Address refresh: Data is refreshed by accessing all 2048 row addresses every 32 ms. A read is one method of accessing those addresses. Each row address (2048 addresses of A0 to A10) must be read at least once every 32 ms. In address refresh mode, $\overline{OE}/\overline{RFSH}$ can remain high. In this case, the I/O pins remain at high impedance, but the refresh is done within RAM.
- (2) Automatic refresh: Instead of address refresh, automatic refresh can be used. RAM goes to automatic refresh mode if $\overline{OE}/\overline{RFSH}$ falls while $\overline{CE}$ is high and it remains low for at least t_{FAP} . One automatic refresh cycle is executed by one low pulse of $\overline{OE}/\overline{RFSH}$. It is not necessary to input the refresh address from outside since it is generated internally by an on-chip address counter. 2048 automatic refresh cycles must be done every 32 ms.
- (3) Self refresh: Self refresh mode is suitable for data retention by battery. In standby mode, a self refresh starts automatically when $\overline{OE}/\overline{RFSH}$ stays low for more than 8 μ s. Refresh addresses are automatically specified by the on-chip address counter, and the refresh period is determined by the on-chip timer.

Automatic refresh and self refresh are distinguished from each other by the width of the $\overline{OE}/\overline{RFSH}$ low pulse in standby mode. If the $\overline{OE}/\overline{RFSH}$ low pulse is wider than 8 μ s, RAM becomes into self refresh mode; if the $\overline{OE}/\overline{RFSH}$ low pulse is less than 8 μ s, it is recognized as an automatic refresh instruction.

At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS} , $\overline{CE}$ and $\overline{OE}/\overline{RFSH}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{OE}/\overline{RFSH}$ at the beginning of automatic refresh must not occur during t_{RFS} period.

Others

Since pseudo static RAM consists of dynamic circuits like DRAM, its clock pins are more noise-sensitive than conventional SRAM's.

- (1) If a short $\overline{CE}$ pulse of a width less than $t_{CE \text{ min}}$ is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{CE}$ low pulses of less than $t_{CE \text{ min}}$ are inhibited. Note that a 10 ns $\overline{CE}$ low pulse may sometimes occur owing to the gate delay on the board if the $\overline{CE}$ signal is generated by the decoding of higher address signals on the board. Avoid these short pulses.
- (2) $\overline{OE}/\overline{RFSH}$ works as refresh control in standby mode. A short $\overline{OE}/\overline{RFSH}$ low pulse may cause an incomplete refresh that will destroy data. Make sure that $\overline{OE}/\overline{RFSH}$ low pulse of less than $t_{FAP \text{ min}}$ are also inhibited.
- (3) t_{OHC} and t_{OCD} are the timing specs which distinguish the $\overline{OE}$ function of $\overline{OE}/\overline{RFSH}$ from the $\overline{RFSH}$ function. The t_{OHC} and t_{OCD} specs must be strictly maintained.
- (4) Start the HM658512AI operating by executing at least eight initial cycles (dummy cycles) at least 100 μ s after the power voltage reaches 4.5 V to 5.5 V after power-on.

Operation Table

$\overline{\text{CE}}$	$\overline{\text{OE/RFSH}}$	$\overline{\text{WE}}$	I/O	Operation
L	L	H	Dout	Read
L	×	L	High-Z	Write
L	H	H	High-Z	—
H	L	×	High-Z	Refresh
H	H	×	High-Z	Standby

Note: H; V_{IH} ; L; V_{IL} ; ×; V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Terminal voltage with respect to V_{SS}	V_T	−1.0 to +7.0	V	1
Power dissipation	P_T	1.0	W	
Storage temperature range	Tstg	−55 to +125	°C	
Storage temperature range under bias	Tbias	−40 to +85	°C	

Note: 1. With respect to V_{SS}

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.8	—	6.0	V	
Input low voltage	V_{IL}	−1.0	—	0.8	V	1
Ambient temperature range	Ta	−40	—	+85	°C	

Note: 1. V_{IL} min = −3.0 V for pulse width 30 ns

HM658512AI Series

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{VO} = 0 \text{ mA}$, $t_{cyc} = \text{min}$	
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE} = V_{IH}$, $V_{in} \geq 0 \text{ V}$ $\overline{OE}/\overline{RFSH} = V_{IH}$	
	I_{SB2}	—	20	200	μA	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$, $\overline{OE}/\overline{RFSH} \geq V_{CC} - 0.2 \text{ V}$	
Operating power supply current in self refresh mode	I_{CC2}	—	1	2	mA	$\overline{CE} = V_{IH}$, $V_{in} \geq 0 \text{ V}$, $\overline{OE}/\overline{RFSH} = V_{IL}$	
	I_{CC3}	—	70	200	μA	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$, $\overline{OE}/\overline{RFSH} \leq 0.2 \text{ V}$	
Input leakage current	I_{LI}	-10	—	10	μA	$V_{CC} = 5.5 \text{ V}$, $V_{in} = V_{SS}$ to V_{CC}	
Output leakage current	I_{LO}	-10	—	10	μA	$\overline{OE}/\overline{RFSH} = V_{IH}$ $V_{IO} = V_{SS}$ to V_{CC}	
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1 \text{ mA}$	
	V_{OH}	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$	

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	8	pF	$V_{in} = 0 \text{ V}$
Input/output capacitance	C_{VO}	—	10	pF	$V_{IO} = 0 \text{ V}$

Note : This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V, 2.8 V
- Input rise and fall time: 5 ns
- Timing measurement level: 0.8 V, 2.2 V
- Reference levels: $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.8 \text{ V}$
- Output load: 1 TTL Gate and C_L (100 pF) (Including scope and jig)

HM658512AI Series

		HM658512AI							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	130	—	160	—	190	—	ns	
Chip enable access time	t _{CEA}	—	80	—	100	—	120	ns	
Read-modify- write cycle time	t _{RWC}	180	—	220	—	260	—	ns	
Output enable access time	t _{OEA}	—	30	—	40	—	50	ns	
Chip disable to output in high-Z	t _{CHZ}	0	25	0	25	0	30	ns	1, 2
Chip enable to output in low-Z	t _{CLZ}	20	—	20	—	20	—	ns	2
Output disable to output in high-Z	t _{OHZ}	—	25	—	25	—	25	ns	1, 2
Output enable to output in low-Z	t _{OLZ}	0	—	0	—	0	—	ns	2
Chip enable pulse width	t _{CE}	80 n	10 μ	100 n	10 μ	120 n	10 μ	s	
Chip enable precharge time	t _P	40	—	50	—	60	—	ns	
Address setup time	t _{AS}	0	—	0	—	0	—	ns	
Address hold time	t _{AH}	20	—	25	—	30	—	ns	
Read command setup time	t _{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t _{RCH}	0	—	0	—	0	—	ns	
Write command pulse width	t _{WP}	25	—	30	—	35	—	ns	
Chip enable to end of write	t _{CW}	80	—	100	—	120	—	ns	
Chip enable to output enable delay time	t _{OCD}	0	—	0	—	0	—	ns	
Output enable hold time	t _{OHC}	0	—	0	—	0	—	ns	
Data in to end of write	t _{DW}	20	—	25	—	30	—	ns	
Data in hold time for write	t _{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	5	—	ns	2
Write to output in high-Z	t _{WHZ}	—	20	—	25	—	30	ns	1, 2
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	6

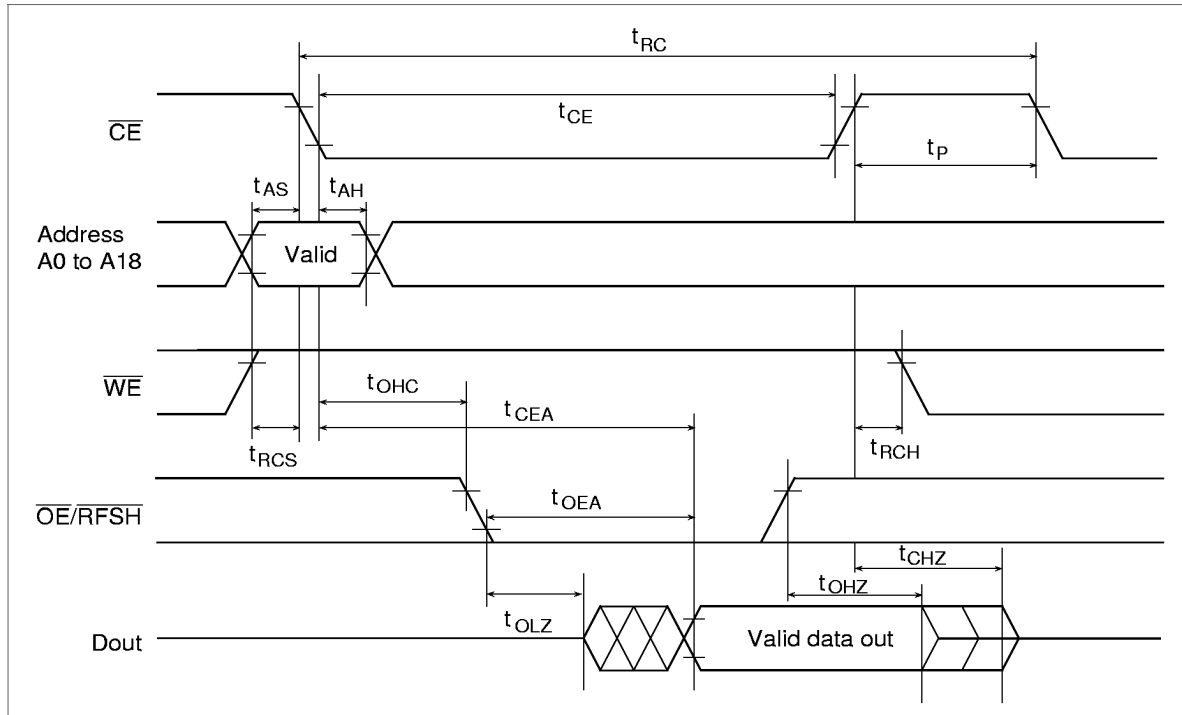
HM658512AI Series

		HM658512AI							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Refresh command delay time	t_{RFD}	40	—	50	—	60	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 n	8 μ	80 n	8 μ	80 n	8 μ	s	
Automatic refresh cycle time	t_{FC}	130	—	160	—	190	—	ns	
Refresh command pulse width for self refresh	t_{FAS}	8	—	8	—	8	—	μ s	
Refresh reset time from self refresh	t_{RFS}	600	—	600	—	600	—	ns	9
Refresh period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
 2. t_{CHZ} , t_{CLZ} , t_{OHZ} , t_{OLZ} , t_{WHZ} and t_{OW} are sampled under the condition of $t_T = 5$ ns and not 100% tested.
 3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
 4. If the $\overline{CE}$ low transition occurs simultaneously with or from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
 5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 6. Transition time t_T is measured between V_{IH} (min) and V_{IL} (max). V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
 7. After power-up, pause for more than 100 μ s and execute at least 8 initialization cycles.
 8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 μ s after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
 9. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS} , $\overline{CE}$ and $\overline{OE}/\overline{RFSH}$ must be kept high. If automatic refresh follows self refresh, low transition of $\overline{OE}/\overline{RFSH}$ at the beginning of automatic refresh must not occur during t_{RFS} period.

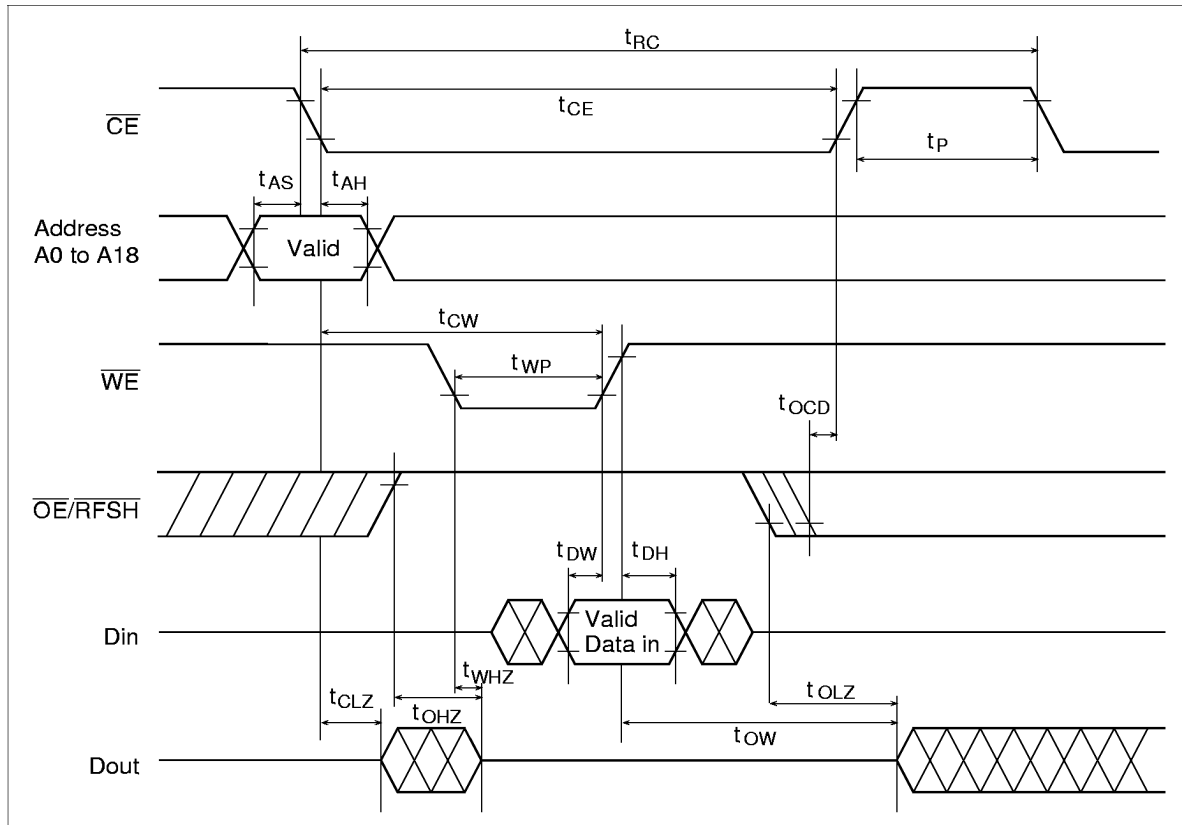
Timing Waveform

Read Cycle

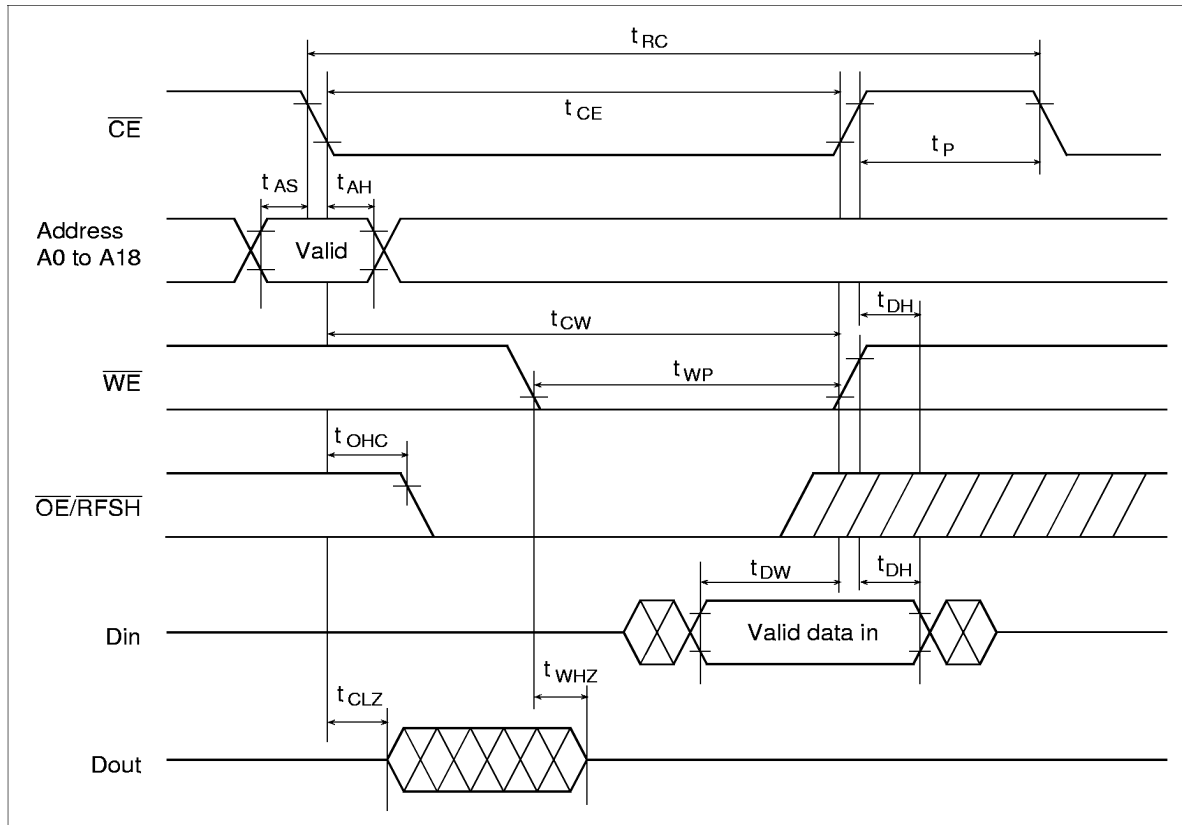


HM658512AI Series

Write Cycle (1) ($\overline{\text{OE}} = V_{\text{IH}}$)

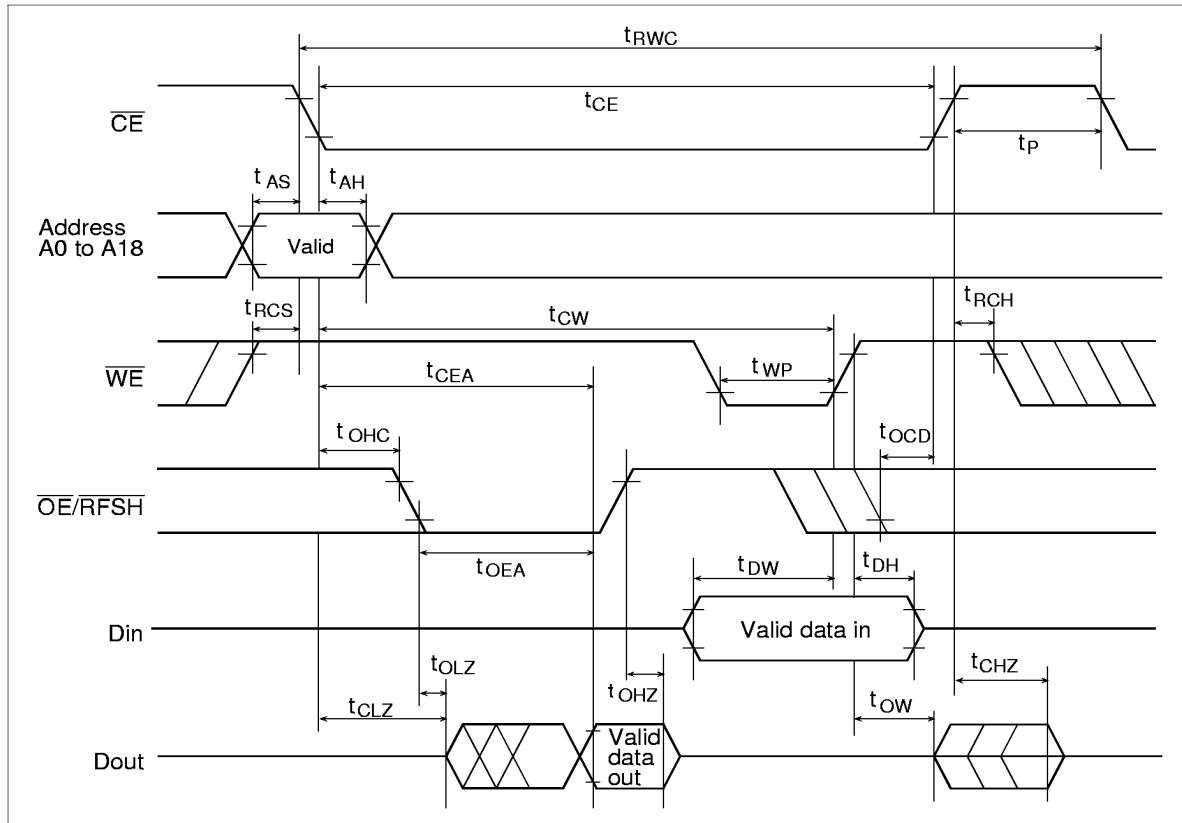


Write Cycle (2) ($\overline{OE} = V_{IL}$)

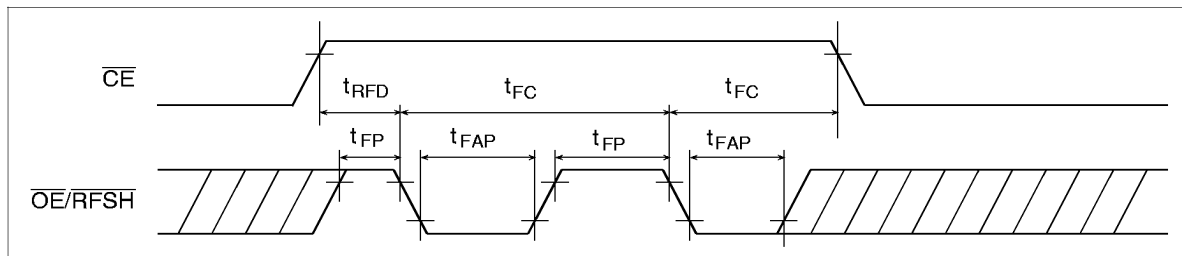


HM658512AI Series

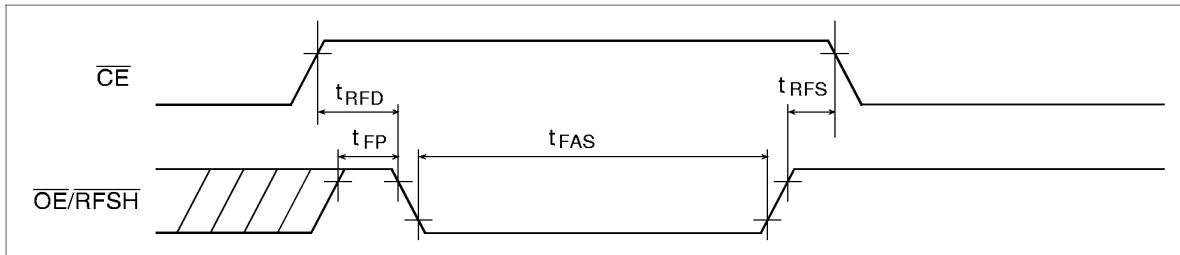
Read-Modify-Write Cycle



Automatic Refresh Cycle



Self Refresh Cycle



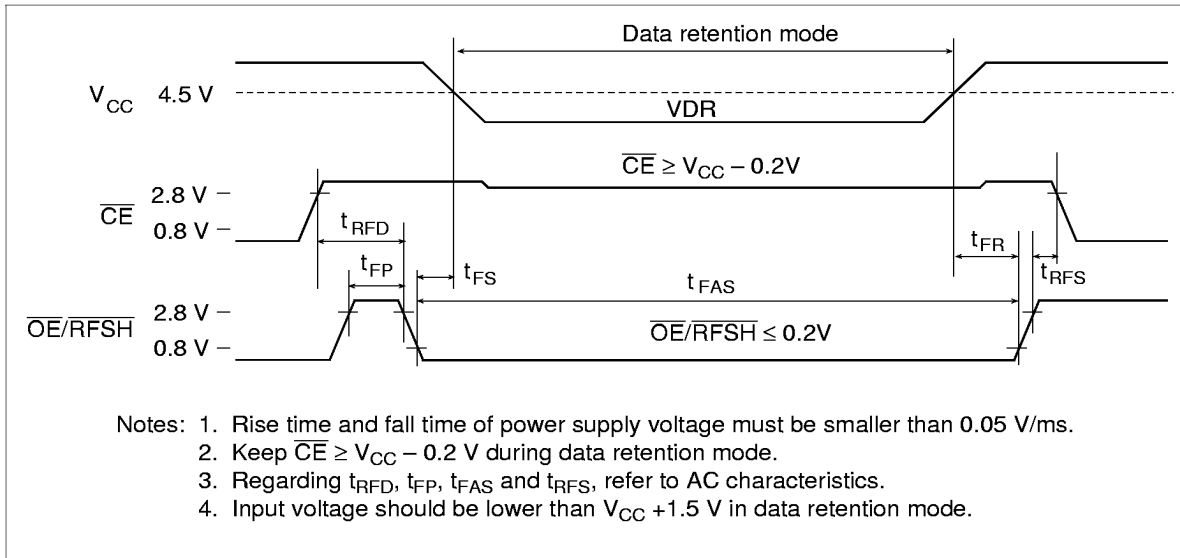
Low V_{CC} Data Retention Characteristics ($T_a = -40$ to $+85^\circ\text{C}$)

This characteristics is guaranteed only for V-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	3.6	—	5.5	V	
Self refresh current	I_{CCDR}	—	—	200	μA	$V_{CC} = 3.6 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ $\overline{OE/RFSH} \leq 0.2$ $V_{in} \geq 0 \text{ V}$
		—	—	200	μA	$V_{CC} = 5.5 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ $\overline{OE/RFSH} \leq 0.2$ $V_{in} \geq 0 \text{ V}$
Refresh setup time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

HM658512AI Series

Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM658512ALFPI Series (FP-32D)

