CT2566

MIL-STD-1553 TO MICROPROCESSOR INTERFACE UNIT

GPS CT2566 MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface. It is available packaged in:

1) 78 pin DIL hybrid

2) 82 pin flatpack

3) PGA

The CT2566 provides an interface by using RAM allowing the CPU to transmit or receive 1553 traffic simply by accessing the memory.

All 1553 message transfers are entirely memory or I/O mapped. The CT2566 supports 1553 interface devices such as GPS's CT2512 dual RT or the CT2565 dual BC, RT, and MT.

The CT2566 operates over the full military –55°C to +125°C temperature range.

FEATURES

- Second source to the BUS-66300
- PGA Version available, (second source to the BUS-66312)
- Compatible with MIL-STD-1750 CPUs
- Compatible with MOTOROLA, INTEL, and ZILOG CPUs
- Compatible with GPS CT2565 BC/RT/MT and CT2512 RT
- Minimises CPU overhead
- Signal controls for shared memory implementation
- Transfers complete messages to shared memory
- Provides Memory Mapped 1553 Interface

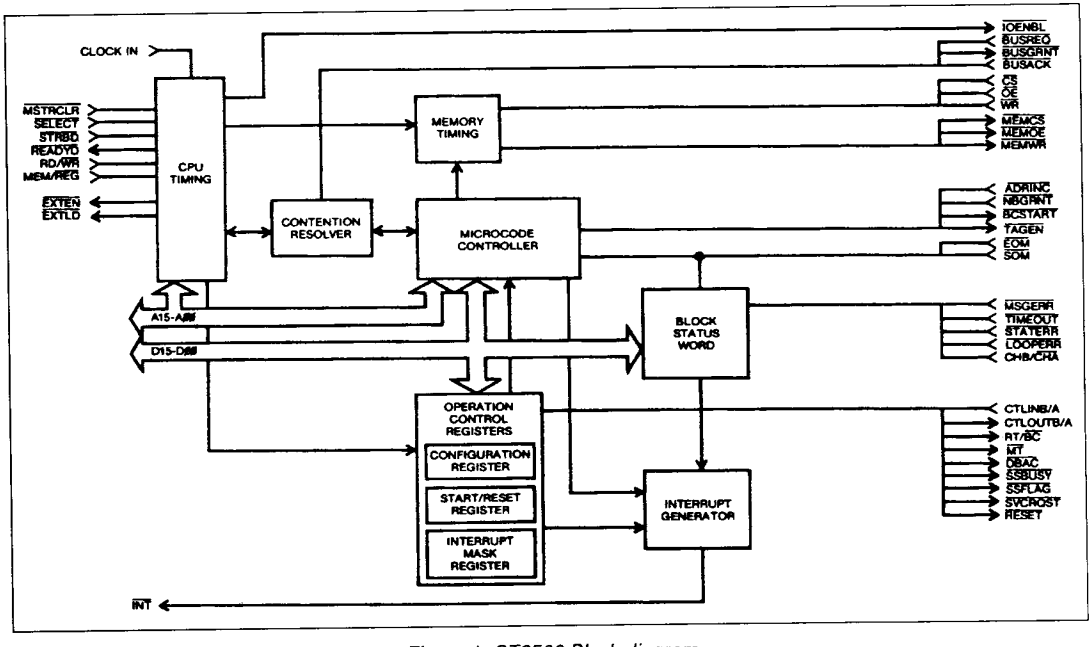

Figure 1: CT2566 Block diagram

SPECIFICATIONS

Specifications at nominal power supply voltages.

PARAMETER	UNITS	VALUE
Logic		
I_{IH} (With V_{IH} = 2.7V)	µA	−630
I_{IL} (With V_{IL} = 0.0V)	µA	−700
I_{OH}	mA	4.0 min
I_{OL}	mA	4.0
V_{IH}	V	2.0
V_{IL}	V	0.8
V_{OH}	V	3.7
V_{OL}	V	0.4
Clock	MHz	12
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	10 typ
Temperature Range		
Operating (Case)	°C	−55 to +125
Storage	°C	−65 to +150
Physical Characteristics		
Size		
(78 pin DIP)	in	2.1 × 1.87 × 0.25
	(mm)	(53 × 47.5 × 6.4)
(82 pin flatpack)	in	2.1 × 1.87 × 25
	(mm)	(55.6 × 40.6 × 3.71)
Weight		
(78 pin DIP)	oz (g)	1 (28)
(82 pin flatpack)	oz (g)	1 (28)

Table 1: Specifications

GENERAL

The CT2566 was designed to perform required handshaking to the 1553 interface device, storing or retrieving message(s) from a user supplied RAM and notifying the CPU that a 1553 transaction has occurred. The CPU uses this RAM to read the received data as well as to store messages to be transmitted onto the Bus.

The CT2566 can be used to implement BC, RT, or MT operation and can be either memory mapped or I/O mapped to CPU address space. Registers internal to the CT2566 control its operation.

The CT2566 can access up to four external, user supplied registers and can address up to 64K words of RAM. The RAM selected must be a non-latched static RAM (capable of meeting the timing constraints for the CT2566). A double buffering architecture is provided to prevent incomplete or partially updated information from being transmitted onto the 1553 Data Bus.

The CT2566 requires an external, user supplied clock.

COMPATIBLE MICROPROCESSOR TYPES

The CT2566 may be used with most common microprocessors, including, the Motorola 68000 family, the Intel 8080 family, Zilog Z8000 products, and available MIL-STD-1750 processors.

Interfacing the CT2566 to the 1553 Data Bus requires external circuitry such as GPS's CT2565(BC/RT/MT) and CT1589D transceivers. Figure 2 shows the interconnection for these components.

PIN NO.	NAME	I/O	DESCRIPTION
1	$\overline{\text{SELECT}}$	I	Select. When active, selects CT2566 for operation.
2	RD/$\overline{\text{WR}}$	I	Read/Write. Controls CPU bus data direction.
3	$\overline{\text{READYD}}$	O	Ready Data. When active indicates data has been received from, or is available to the CPU.
4	$\overline{\text{EXTEN}}$	O	External Enable. Output from CT2566 to enable output from external devices. Same timing as $\overline{\text{MEMOE}}$.
5	$\overline{\text{TAGEN}}$	O	Tag Enable. Enables an external time tag counter for transferring the time tag word into memory.
6	$\overline{\text{EOM}}$	I	End of Message. Input from 1553 device indicating end of message.
7	$\overline{\text{SOM}}$	I	Start of Message. Input from 1553 device indicating start of message in RTU mode.
8	$\overline{\text{STATERR}}$	I	Status Error. Input from 1553 device when status word has either a bit set or unexpected RT address (in BC mode only).
9	$\overline{\text{ADRINC}}$	I	Address Increment. Sent from 1553 device to increment address counter following word transfer.
10	MEM/$\overline{\text{REG}}$	I	Memory/Register. Input from CPU to select memory or register data transfer.
11	CLOCK IN	I	Clock input; 50% duty cycle, 12MHz, max.
12	$\overline{\text{LOOPERR}}$	I	Loop Error. Input from 1553 device if short loop BIT fails.
13	$\overline{\text{BUSREQ}}$	I	Bus Request. When active, indicates 1553 device requires use of the address/ data bus.
14	$\overline{\text{BUSGRNT}}$	O	Bus Grant. Handshake output to 1553 device in response to BUS REQUEST indicating address/data bus available to 1553 device.
15	Not Used	-	-
16	$\overline{\text{MEMCS}}$	O	Memory Chip Select. Low from CT2566 to enable external RAM. Used with 4K × 4 RAM type device to read RAM or used in conjunction with $\overline{\text{MEMWR}}$ to write data into RAM.
17	$\overline{\text{OE}}$	I	Output Enable. Input from 1553 device used to enable memory on the parallel bus.
18	N/C	-	Not Used.
19	$\overline{\text{NBGRNT}}$	I	Low pulse from 1553 device preceding start of received new protocol sequence. Used with superseding command to reset DMA in progress.
20	+ 5 Volt	I	Logic power supply.
21	D15	I/O	Data Bus Bit 15 (MSB).
22	D13	I/O	Data Bus Bit 13.
23	D11	I/O	Data Bus Bit 11.
24	D09	I/O	Data Bus Bit 9.
25	D07	I/O	Data Bus Bit 7.
26	D05	I/O	Data Bus Bit 5.
27	D03	I/O	Data Bus Bit 3.
28	D01	I/O	Data Bus Bit 1.
29	$\overline{\text{SSFLAG}}$	O	Subsystem Flag. Output to 1553 device to set RT subsystem flag status bit.
30	$\overline{\text{SSBUSY}}$	O	Subsystem Busy. Output to 1553 device to set RT subsystem busy flag.
31	RTU/$\overline{\text{BC}}$	O	Output to 1553 device used in conjunction with MT to set operating mode.
32	A14	O	Address Bit 14.
33	A12	O	Address Bit 12.
34	A10	O	Address Bit 10.
35	A08	O	Address Bit 8.
36	A06	O	Address Bit 6.
37	A04	O	Address Bit 4.
38	A02	I/O	Address Bit 2.

Table 2: CT2566 Pin Functions (78 Pin Dip)

PIN NO.	NAME	I/O	DESCRIPTION
39	A00	I/O	Address Bit 0 (LSB).
40	GND	-	Signal Return.
41	$\overline{\text{STRBD}}$	I	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to indicate a data transfer cycle to/from CPU.
42	$\overline{\text{IOEN}}$	O	Input/Output Enable. Output from CT2566 to enable external buffers/latches connecting the hybrid to the address/data bus.
43	$\overline{\text{EXTLD}}$	O	External Load. Used to load data into external device via the CT2566 data bus. Same timing as MEMWR.
44	CHB/$\overline{\text{CHA}}$		Input from 1553 in RT mode used to indicate received 1553 message came in either Channel A or B.
45	$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
46	$\overline{\text{BCSTART}}$	O	Bus Controller Start. Outputs to 1553 in initiate BC cycle.
47	$\overline{\text{RESET}}$	O	Reset. Output to external device from CT2566 consisting of the OR condition of CPU reset and CPU Master Clear.
48	MSGERR	I	Message Error. Input from 1553 device when an error occurs in message sequence.
49	CTLIN B/$\overline{\text{A}}$	I	Input to change active memory map area (0 = area A).
50	CTLOUT B/$\overline{\text{A}}$	O	Output from CT2566 selecting which area is to be active (0 = area A).
51	$\overline{\text{TIMEOUT}}$	I	Input from 1553 device indicating no response time-out.
52	$\overline{\text{MSTRCLR}}$	I	Master Clear. Power-on reset from CPU. Resets DMA in progress and internal registers to logic "O".
53	$\overline{\text{BUSACK}}$	I	Bus Acknowledge. Input from 1553 device acknowledge receipt of $\overline{\text{BUSGRNT}}$.
54	$\overline{\text{WR}}$	I	Write. Input from 1553 device for writing data into memory.
55	$\overline{\text{CS}}$	I	Chip Select. Input from 153 device that is routed to $\overline{\text{MEMCS}}$.
56	$\overline{\text{MEMOE}}$	O	Memory Output Enable. Output from CT2566 to enable memory output data.
57	MEMWR	O	Memory Write. Output pulse from CT2566 to write data bus data into memory.
58	Not Used	-	-
59	$\overline{\text{MT}}$	O	Bus Monitor. Used in conjunction with RTU/$\overline{\text{BC}}$ to set operating mode.
60	D14	I/O	Data Bus Bit 14.
61	D12	I/O	Data Bus Bit 12.
62	D10	I/O	Data Bus Bit 10.
63	D08	I/O	Data Bus Bit 8.
64	D06	I/O	Data Bus Bit 6.
65	D04	I/O	Data Bus Bit 4.
66	D02	I/O	Data Bus Bit 2.
67	D00	I/O	Data Bus Bit 0 (LSB).
68	$\overline{\text{SVCREQ}}$	O	Service Request. Used to set service request bit in RT Block Status Word.
69	$\overline{\text{DBAC}}$	O	Dynamic Bus Acceptance. Used to set status bit in RT Block Status Word.
70	A15	O	Address Bit 15 (MSB).
71	A13	O	Address Bit 13.
72	A11	O	Address Bit 11.
73	A09	O	Address Bit 9.
74	A07	O	Address Bit 7.
75	A05	O	Address Bit 5.
76	A03	O	Address Bit 3.
77	A01	I/O	Address Bit 1.
78	GND	-	Chassis Ground.

Table 2: CT2566 Pin Functions (78 Pin Dip) (Continued)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	N/C	42	N/C
2	$\overline{\text{SELECT}}$	43	GROUND
3	$\overline{\text{STRBD}}$	44	CHASSIS GROUND
4	RD/$\overline{\text{WR}}$	45	A00 (LSB)
5	$\overline{\text{IOENBL}}$	46	A01
6	$\overline{\text{READYD}}$	47	A02
7	$\overline{\text{EXTLD}}$	48	A03
8	$\overline{\text{EXTEN}}$	49	A04
9	CHB/$\overline{\text{CHA}}$	50	A05
10	$\overline{\text{TAGEN}}$	51	A06
11	$\overline{\text{INT}}$	52	A07
12	$\overline{\text{EOM}}$	53	A08
13	$\overline{\text{BCSTART}}$	54	A09
14	$\overline{\text{SOM}}$	55	A10
15	$\overline{\text{RESET}}$	56	A11
16	$\overline{\text{STATERR}}$	57	A12
17	$\overline{\text{MSGERR}}$	58	A13
18	$\overline{\text{ADRINC}}$	59	A14
19	CTLIN B/$\overline{\text{A}}$	60	A15
20	MEM/$\overline{\text{REG}}$	61	RTU/$\overline{\text{BC}}$
21	CTLOUT B/$\overline{\text{A}}$	62	$\overline{\text{DBAC}}$
22	CLOCK IN	63	$\overline{\text{SSBUSY}}$
23	$\overline{\text{TIMEOUT}}$	64	$\overline{\text{SVCREQ}}$
24	$\overline{\text{LOOPERR}}$	65	$\overline{\text{SSFLAG}}$
25	$\overline{\text{MSTRCLR}}$	66	D00
26	$\overline{\text{BUSYREQ}}$	67	D01
27	$\overline{\text{BUSACK}}$	68	D02
28	$\overline{\text{BUSGRNT}}$	69	D03
29	$\overline{\text{WR}}$	70	D04
30	N/C	71	D05
31	$\overline{\text{CS}}$	72	D06
32	$\overline{\text{MEMCS}}$	73	D07
33	$\overline{\text{MEMOE}}$	74	D08
34	$\overline{\text{OE}}$	75	D09
35	$\overline{\text{MEMWR}}$	76	D10
36	Not Used	77	D11
37	N/C	78	D12
38	$\overline{\text{NBGRNT}}$	79	D13
39	$\overline{\text{MT}}$	80	D14
40	+5V	81	D15
41	N/C	82	N/C

Table 3: CT2566FP Pin Functions (82 Pin Flatpack)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	NC	F01	$\overline{SSBUSY}$
A02	A09	F02	$\overline{DBAC}$
A03	A08	F03	RTU/$\overline{BC}$
A04	A06	F11	CLOCKOUT
A05	A05	F12	VCC
A06	A03	F13	CLOCKIN
A07	A02	G01	$\overline{SSFLAG}$
A08	GND	G02	VCC
A09	$\overline{NBGRNT}$	G03	$\overline{SVCRQST}$
A10	$\overline{OE}$	G11	GND
A11	$\overline{MEMCS}$	G12	CTLOUTB/$\overline{A}$
A12	NC	G13	VCC
A13	$\overline{CS}$	H01	D00
B01	NC	H02	D01
B02	GND	H03	GND
B03	NC	H11	$\overline{ADRINC}$
B04	A07	H12	CTLINB/$\overline{A}$
B05	GND	H13	MEM/$\overline{REG}$
B06	VCC	J01	D02
B07	A00	J02	D03
B08	$\overline{ADRDIR}$	J12	$\overline{STATERR}$
B09	$\overline{MEMWR}$	J13	$\overline{MSGERR}$
B10	$\overline{MEMOE}$	K01	D04
B11	NC	K02	D05
B12	GND	K12	$\overline{SOM}$
B13	$\overline{BUSGRNT}$	K13	$\overline{RESET}$
C01	A11	L01	VCC
C02	A10	L02	D07
C06	A04	L06	D13
C07	A01	L07	$\overline{DDIR}$
C08	$\overline{MT}$	L08	$\overline{IOENBL}$
C12	$\overline{WR}$	L12	$\overline{EOM}$
C13	$\overline{BUSACK}$	L13	$\overline{BCSTART}$
D01	A13	M01	D06
D02	A12	M02	GND
D12	$\overline{BUSREQ}$	M03	D08
D13	$\overline{MSTRCLR}$	M04	D10
E01	A15	M05	D12
E02	A14	M06	D14
E12	$\overline{LOOPERR}$	M07	VCC
E13	$\overline{TIMEOUT}$	M08	RD/$\overline{WR}$

Table 4: CT2566PGA Pin Functions (Pin Grid Array)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
M09	GND	N05	GND
M10	$\overline{\text{EXTEN}}$	N06	D15
M11	$\overline{\text{INT}}$	N07	$\overline{\text{SELECT}}$
M12	GND	N08	$\overline{\text{STRBED}}$
M13	VCC	N09	$\overline{\text{READYD}}$
N01	NC	N10	$\overline{\text{EXTLD}}$
N02	NC	N11	CHB/$\overline{\text{CHA}}$
N03	D09	N12	$\overline{\text{TAGEN}}$
N04	D11	N13	NC

Table 4: CT2566PGA Pin Functions (Pin Grid Array) (Continued)

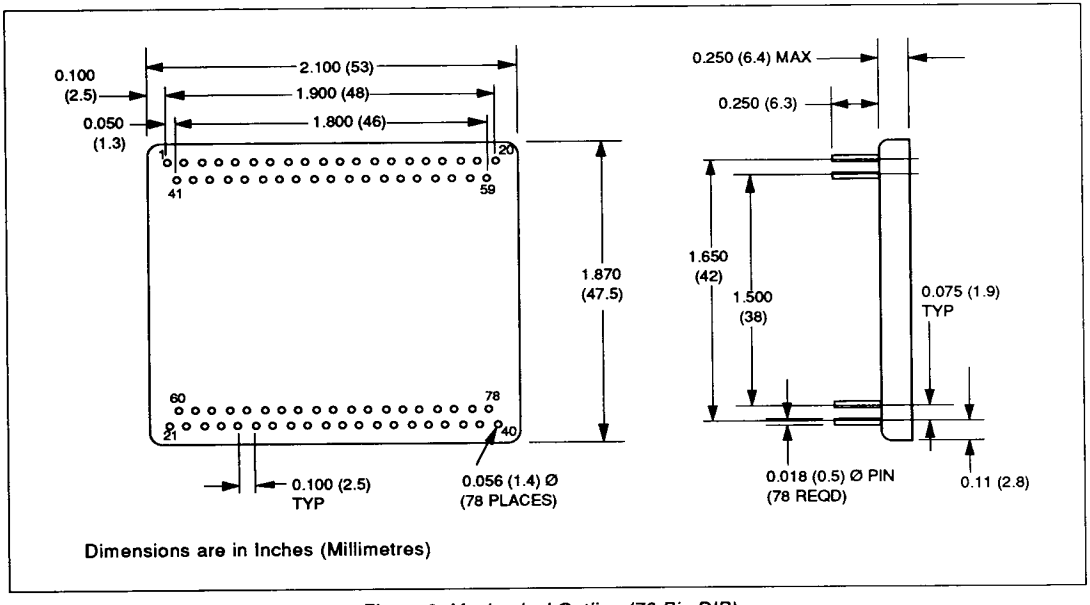

Figure 2: Mechanical Outline (78 Pin DIP)

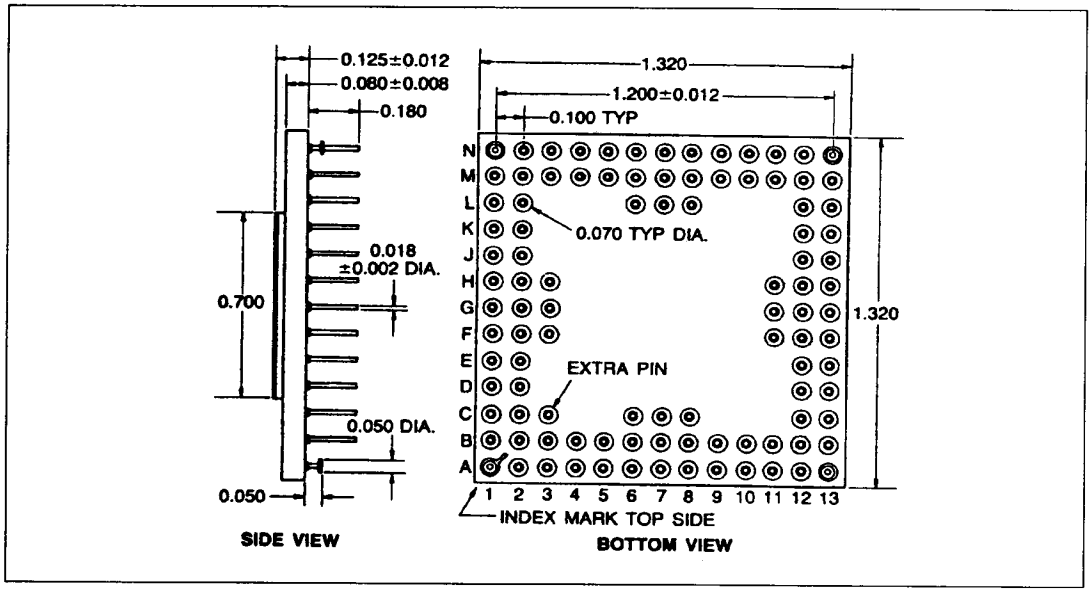

Figure 3: Mechanical Outline (CT2566PGA)