Dual Frequency Generator

Features

- **Two independent clock outputs available**
- **On chip Phase Locked Loops with VCO and integrated loop filters for low jitter clock outputs**
- **Mask option for 16 + 4 frequencies, or 8 + 8**
- **Frequencies up to 130 MHz on each output clock generated internally**
- **Low power CMOS technology**
- **20 pin PDIP or SOIC package**
- **Minimum number of external components**
- **Tristate outputs**
- **Pin compatible with ICS2494 and ICS90C64**
- **Crystal oscillator circuitry with output clock**
- **16 pin narrow SOIC (150 mil) or PDIP package option available**

Applications

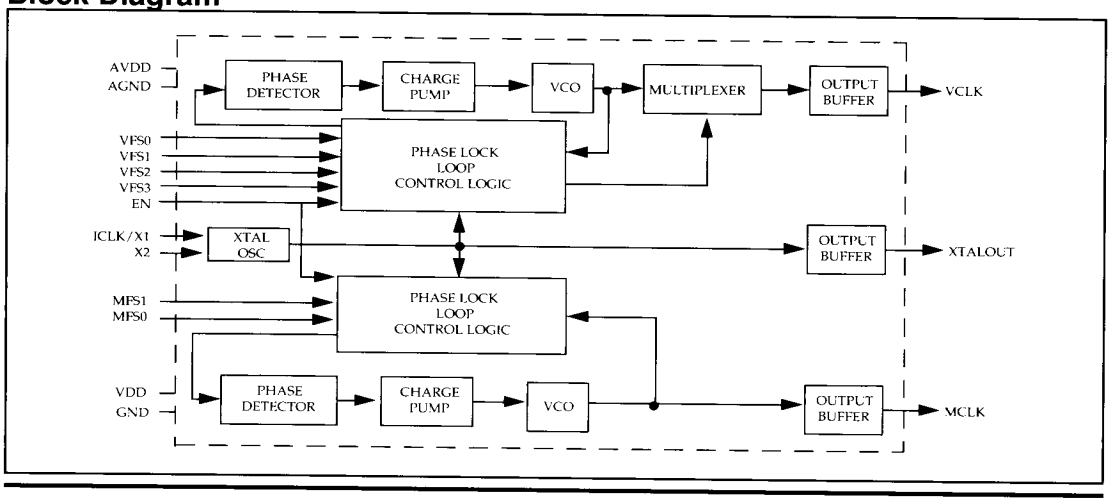
Graphics: Many video graphics systems now utilize multiple clock oscillators to provide all of the frequencies required for different monitors and modes of resolution. In addition, many graphics processors require one separate fixed frequency for the memory or system clock. By providing two independent output clocks, the AV9194 saves power, board space, and cost in eliminating these oscillators.

General Description

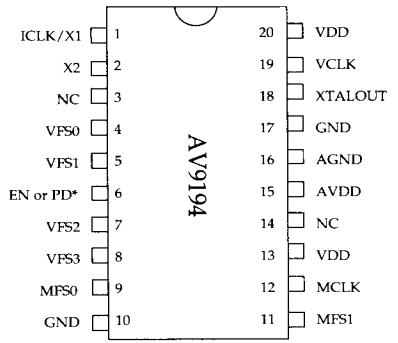
The AV9194 is a dual output frequency generator that is ideal for graphics applications. The device can replace many crystal oscillators by containing all of the required output frequencies on-chip. The AV9194 can use either a crystal or TTL level clock for its input reference frequency. On notebooks and other motherboards, the 14.318MHz input can be generated by the AV9128/9 or the AV9152/3/5. Utilizing ICS' proprietary analog CMOS Phase Locked Loop (PLL) technology, this reference frequency is used to generate two independently controlled output clocks, VCLK and MCLK. Up to 20 output frequencies, ranging from 5 to 130 MHz, can be mask programmed into the device at the time of manufacture. The six Frequency Select pins are used to choose one of 16 (or 8) masked output frequencies on the video clock, VCLK, and one of 4 (or 8) frequencies on the second clock, designated MCLK. This second clock can be used as a memory clock to time DRAMs and VRAMs, as another video (or pixel) clock, or as a system clock required by graphics processors like the 8514A and 34010/20. Standard versions of the AV9194 are available.

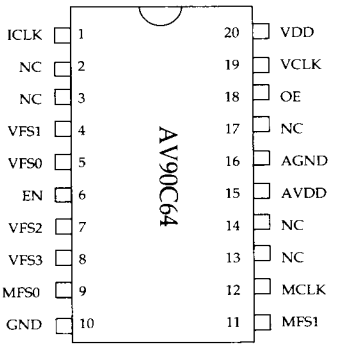
The AV9194 is one of the latest in ICS's frequency generator family. ICS has devices that are designed for many computer and computer peripheral applications, all manufactured in analog CMOS technology.

Block Diagram



Pin Configurations





Pin Description for AV9194 / AV90C64

Pin Name	Pin # AV9194	Pin # AV90C64	Pin type	Description
ICLK/X1	1	1	Input	INPUT CLOCK. TTL clock signal or crystal input
X2	2	-	Output	CRYSTAL OUT. Connect when using crystal or ceramic resonator
NC	3	3	-	NOT CONNECTED. No internal connection
VFS0	4	5	Input	VIDEO FREQUENCY SELECT 0 (LSB)
VFS1	5	4	Input	VIDEO FREQUENCY SELECT 1
EN	6	-	Input	ENABLE. Transparent high. A low latches the frequency select data
EN	-	6	Input	ENABLE. Latches VFS0-VFS3 and MFS0, MFS1 upon rising edge
PD*	6	-	Input	POWER DOWN. Turns off V+MCLK when low (AV9194-46 only)
VFS2	7	7	Input	VIDEO FREQUENCY SELECT 2
VFS3	8	8	Input	VIDEO FREQUENCY SELECT 3 (MSB)
MFS0	9	9	Input	MEMORY FREQUENCY SELECT 0 (LSB)
GND	10	10	-	DIGITAL GROUND
MFS1	11	11	Input	MEMORY FREQUENCY SELECT 1 (MSB)
MCLK	12	12	Output	MEMORY CLOCK output
VDD	13	-	-	Digital power supply. Connect to +5V DC supply
NC	14	14	-	NOT CONNECTED. No internal connection
AVDD	15	15	-	Analog power supply. Connect to +5V DC supply
AGND	16	16	-	ANALOG GROUND
GND	17	-	-	DIGITAL GROUND
XTALOUT	18	-	Intput	CRYSTAL CLOCK OUTPUT
OE	-	18	Input	OUTPUT ENABLE. Tristates VCLK when low
VCLK	19	19	Output	VIDEO CLOCK output to drive pixel clock
VDD	20	20	-	Digital power supply. Connect to +5V DC supply

ABSOLUTE MAXIMUM RATINGS

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias.....0°C to +70°C
Storage temperature..... -40°C to +125°C
Voltage on I/O pins referenced to GND.....GND - 0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts
ESD rating as per MIL-STD-883D, Method 3015, any pin.....1800V

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-		0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0		-	V	V_{DD} = 5V
$I_{IL(1)}$	Input Low Current	-5		-50	µA	V_{IN} = 0V
I_{IH}	Input High Current	-		5	µA	V_{IN} = VDD
V_{OL}	Output Low Voltage	-		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	VDD-.4V	-	-	V	I_{OH} = -1mA,VDD = 5.0V
V_{OH}	Output High Voltage	VDD-.8V	-	-	V	I_{OH} = -4mA,VDD =.5.0V
V_{OH}	Output High Voltage	2.4		-	V	I_{OH} = -8mA
I_{DD}	Supply Current		20		mA	No load. 28 and 40MHz
I_{DDSB}	Supply Current, Power Down (AV9194-46 Only)		30	50	µA	No load. 28 and 40MHz
$R_{UP(1)}$	Internal Pullup Resistors		500		KΩ	
F_d	Output Frequency Change over Supply and Temperature			0.005	%	With respect to typical frequency
C_I	Input Capacitance			8	pF	F_C = 1 MHz

NOTES: (1) Input pins VFS0-VFS3, MFS0, MFS1, EN, OE and PD* have internal pull-up resistors.
(2) Pins X1 and X2 have on-chip capacitors of 20pF to GND and are tied together by a 1MΩ on-chip resistor.

AC Characteristics						
t_{CLKR}	Input Clock Rise Time			20	ns	
t_{CLKF}	Input Clock Fall Time			20	ns	
t_w	Enable pulse width	20		-	ns	
t_{su}	Setup time data to enable	20		-	ns	
t_{hd}	Hold time data to enable	10		-	ns	
t_r	Rise time, 0.8 to 2.0 Volts	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80%	-	2	4	ns	25 pf load
t_f	Fall time, 2.0 to 0.8 Volts	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20%	-	2	4	ns	25 pf load
d_t	Duty cycle, MCLK andVCLK		48/52	40/60	%	25 pf load
f_{in}	Input frequency, ICLK	5	14.318	20	MHz	
t_{jls}	Jitter, 1 sigma		±75		ps	
t_{jab}	Jitter, absolute		±325	±500	ps	
fmax	Maximum Output Frequency			130	MHz	

AV9194 and AV90C64 Standard Versions

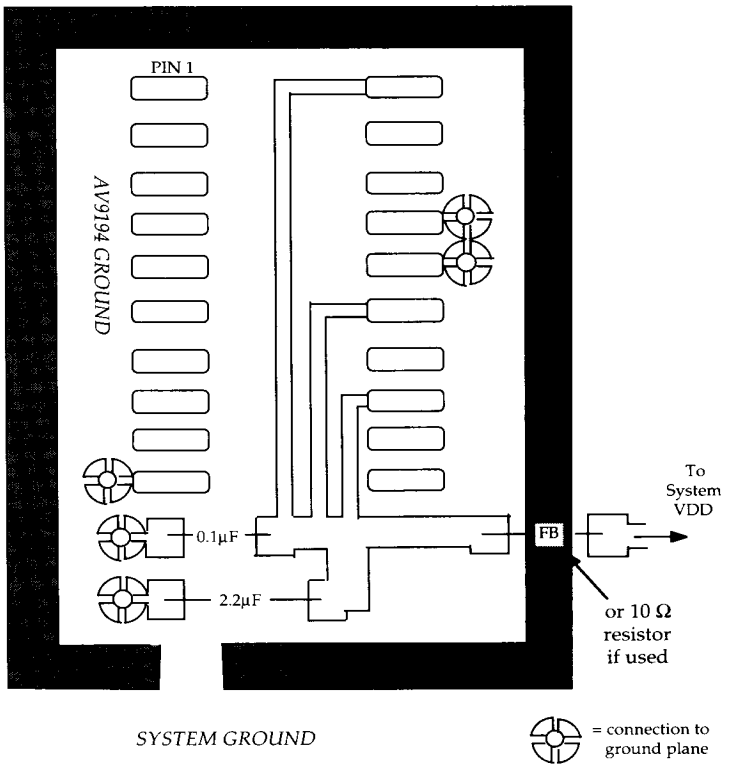
Mask Number	AV9194-04	AV9194-07	AV9194-11	AV9194-12	AV9194-36	AV9194-37
VGA Controllers	Tseng Labs ET4000	S3 86C801,805,928	S3 86C801,805,928	S3 86C911,924	Cirrus Logic	Tseng Labs ET4000
VCLK ADDRESS	VCLK OUTPUT (MHz)					
0	25.175	25.175	25.175	25.175	XTAL	50.350
1	28.322	28.322	28.322	28.322	65.028	56.644
2	32.514	40.0	40.0	40.0	EXTFREQ	65.00
3	36.00	0.00	0.00	0.00	36.00	72.00
4	40.00	50.00	50.00	50.00	25.175	80.00
5	44.90	77.00	77.00	77.00	28.322	89.80
6	50.35	36.00	36.00	36.00	24.00	63.00
7	65.00	44.90	44.90	44.90	40.00	75.00
8	50.35	130.00	130.00	130.00	44.90	25.175
9	56.664	120.00	120.00	120.00	50.35	28.322
A	65.028	80.00	80.00	80.00	16.257	31.50
B	72.00	31.50	31.50	31.50	32.514	36.00
C	80.00	110.00	110.00	110.00	56.644	40.00
D	89.80	65.00	65.00	65.00	20.00	44.90
E	75.00	75.00	75.00	75.00	41.539	50.00
F	108.00	94.50	94.50	72.00	80.00	65.00
MCLK ADDRESS	MCLK OUTPUT (MHz)					
0	41.00	45.00	32.90	40.00	55.00	55.00
1	46.00	38.00	35.60	41.612	60.00	75.00
2	50.00	52.00	43.90	44.744	70.00	70.00
3	56.00	50.00	49.10	50.00	65.00	80.00

AV9194 and AV90C64 Standard Versions (continued)

Mask Number	AV9194-42	AV9194-44	AV9194-46	AV9194-56	AV9194-60	AV90C64
VGA Controllers	WD WD90C30	CPU Applications	NCR 77C22E	S3 86C911, 86C924	Weitek 5X86	WD (All)
VCLK ADDRESS	VCLK OUTPUT (MHz)					
0	30.00	20.00	25.175	25.175	50.35	30.00
1	77.250	24.00	28.322	28.322	56.644	77.25
2	EXTFREQ	32.00	36.00	40.0	33.25	0.00
3	80.00	40.00	65.00	0.00	52.00	80.00
4	31.50	50.00	44.90	50.00	80.00	31.50
5	36.00	66.667	50.00	77.00	63.00	36.00
6	75.00	80.00	80.00	36.00	0.00	75.00
7	50.00	100.00	75.00	44.90	75.00	50.00
8	40.00	54.00	56.644	130.00	25.175	40.00
9	50.00	70.00	63.00	120.00	28.322	50.00
A	32.00	90.00	72.00	80.00	31.50	32.00
B	44.90	110.00	130.00	31.50	36.00	44.90
C	25.175	25.00	90.00	110.00	40.00	25.175
D	28.322	33.333	100.00	65.00	44.90	28.322
E	65.00	40.00	110.00	75.00	50.00	65.00
F	36.00	50.00	120.00	72.00	65.00	36.00
MCLK ADDRESS	MCLK OUTPUT (MHz)					
0	36.00	16.00	50.00	55.00	40.00	41.61
1	44.347	24.00	60.00	75.00	33.333	37.50
2	37.50	50.00	65.00	70.00	45.00	49.22
3	44.773	66.667	75.00	80.00	50.00	44.30

Avasem is continually developing new standard versions of the AV9194.
Consult your local sales representative for the latest Avasem products.

AV9194 BOARD LAYOUT

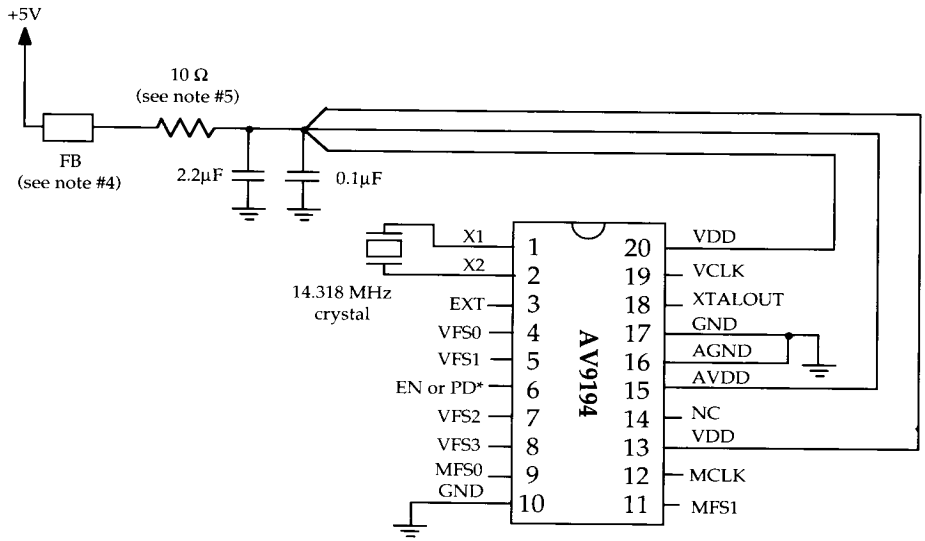


This is the recommended layout for the AV9194. Shown are the power connections and the ground plane.

The most important feature is the isolated ground plane, connected at one point near the 2.2µF and 0.1 µF decoupling caps. The ferrite bead is optional, but will help with EMI radiation from the power supply trace. In applications with an excessively noisy power supply, a 10 Ω resistor in the power supply line (between the decoupling caps and the ferrite bead, if used) is recommended to reduce induced clock jitter. The traces to distribute power should be as wide as possible.

If a crystal or crystal oscillator is used, it should be surrounded by the isolated ground plane. Clock output traces should be kept narrow, and distance over isolated ground plane should be kept to a minimum to reduce coupling.

AV9194
Recommended External Circuit



Notes:

1. Avasem recommends the use of an isolated ground plane for the AV9194. All grounds shown on this drawing should be connected to this ground plane. This ground plane should be connected to the system ground plane at a single point. Please refer to AV9194 Board Layout diagram.

2. A single power supply connection for all VDD lines at the decoupling capacitors is recommended to reduce interaction of analog and digital circuits. The decoupling capacitors should be located as close to the VDD pins as possible.

4. The ferrite bead does not enhance the performance of the AV9194, but will reduce EMI radiation from the VDD line.

5. The 10 Ω resistor is optional for noisy power supply applications. It is used to reduce clock jitter which may be induced by excessive power supply noise.

Ordering Information

Part Number	Temperature Range	Package Type
AV9194-xxCN20	0°C to +70°C	20 lead Plastic DIP
AV9194-xxCW20	0°C to +70°C	20 lead Plastic SOIC
AV90C64N	0°C to +70°C	20 lead Plastic DIP
AV90C64M	0°C to +70°C	20 lead Plastic SOIC

Note: The dash number following AV9194, (denoted by xx above) must be included when ordering product since it specifies the mask options being ordered. Please request an AV9194 customer order form when ordering custom masks.