NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
99-11-15	

2. PROCURING ACTIVITY NO.
3. DODAAC

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Supply Center, Columbus 3990 East Broad Street Columbus, OH 43216-5000	67268	5962-R003-00
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. 5962-94558

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, 32-BIT ALU/16-BIT BUS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON	a. CURRENT C	b. NEW D	No users listed.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "D".
Revisions description column; add "Changes in accordance with NOR 5962-R003-00".
Revisions date column; add "99-11-15".
Revision level block; change from “C” to "D".
Rev status of sheets; for sheets 1 and 3 change from “C” to "D".

Sheet 3: 1.3 Absolute maximum ratings. Junction temperature.
Device type 03, and Device type 04, Case outlines X and Y, delete “+175°C” and change to the following:
“Junction temperature (T_J): . . . . . +150°C”.
For device type 03, , device type 04, and device type 05, Case outlines 9 and Z: delete “+175°C” and change to the following:
“Junction temperature (T_J): . . . . . +125°C”.
Revision level block; change from “C” to “D”.

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DSCC-VAC	MONICA L. POELKING

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
CHIEF, ACTIVE DEVICES TEAM	MONICA L. POELKING	99-11-15

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)
DSCC-VAC	Larry T. Gauder	99-11-15

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate to include class "N". Added device types 03 and 04. Changes made in table I and II. Added case Z. Editorial changes throughout.	96-03-15	Monica L. Poelking
B	Changes in accordance with NOR 5962-R144-96.	96-06-07	Monica L. Poelking
C	Add Appendix A for QML microcircuit die. Add Device 05. Editorial changes throughout.	97-03-06	Monica L. Poelking

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51			
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
CHRISTOPHER A RAUCH

CHECKED BY
THOMAS M HESS

APPROVED BY
MONICA L POELKING

DRAWING APPROVAL DATE
94-06-06

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, 32-BIT ALU/16-BIT BUS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

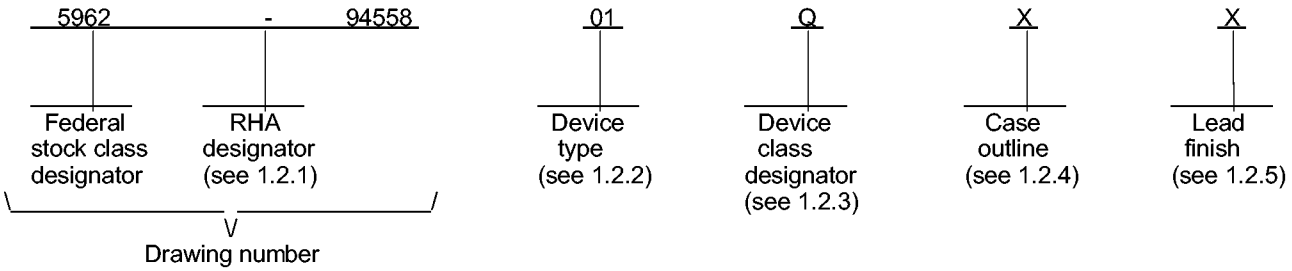
SIZE	CAGE CODE	
A	67268	5962-94558

SHEET 1 OF 51

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C50A	Digital signal processor, 40 MHz
02	320C50A	Digital signal processor, 50 MHz
03	320C50	Digital signal processor, 50 MHz
04	320C50	Digital signal processor, 66 MHz
05 1/	320C50	Digital signal processor, 40 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 2/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	141	Ceramic pin grid array
Y	See figure 1	132	Ceramic quad flat package with non-conductive tiebar
Z	See figure 1	132	Plastic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type 05 is available as QML die only.
2/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.3 Absolute maximum ratings. 3/

Supply voltage range (V_{DD}) 4/	-0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to +7.0 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to +7.0 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}) Case X	4.8°C/W
Thermal resistance, junction-to-case (Θ_{JC}) Case Y	2.6°C/W
Thermal resistance, junction-to-case (Θ_{JC}) Case Z	10°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}) Case X	39.0°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}) Case Y	55.7°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}) Case Z	49.0°C/W
Maximum power dissipation (P_D) T_A = 25°C, V_{DD} = Max:	
Device 01	1 W
Device 02	1.375 W
Device 03, 04. 05	0.9 W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}):	
Devices 01 and 02	+4.5 V dc to +5.5 V dc
Devices 03, 04 and 05	+4.75 V dc to +5.25 V dc
Supply voltage (V_{SS})	+0.0 V dc
High level input voltage range (V_{IH})	
CLKIN, CLKIN2	+3.0 V dc to V_{DD} + 0.3 V dc
CLKX, CLKR, TCLKX, TCLKR	+2.5 V dc to V_{DD} + 0.3 V dc
All others	+2.2 V dc to V_{DD} + 0.3 V dc
Low level input voltage range (V_{IL})	-0.3 V dc to 0.6 V dc
Maximum high level output current (I_{OH})	-300 µA
Maximum low level output current (I_{OL})	+2 mA
Input clock frequency range	
(Device 01, 05) 5/	0 MHz to 40 MHz
(Device 02) 5/	0 MHz to 50 MHz
(Device 03) 5/	0 MHz to 50 MHz
(Device 04) 5/	0 MHz to 66 MHz
Internal clock option capacitors C1, C2	10 pF
Case operating temperature range (T_C)	-55°C ≤ T_C ≤ +125°C
Minimum free-air operating temperature (T_A)	-55°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ All voltage values are with respect to V_{SS}.
5/ This device utilizes a fully static design and therefore can operate with $t_{c(Cl)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 6.7 MHz to meet device test time requirements.
6/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies shouldbe addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 5.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Device types 01, 02, 03, 04 and 05 shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage 2/	V_{OH}	I_{OH} = -300 µA		1,2,3	All	2.4		V
Low level output voltage 2/	V_{OL}	I_{OL} = 2 mA		1,2,3	All		0.6	V
3-state current	I_Z	V_{DD} = Max	$\overline{BR}$ (with internal pullup)	1,2,3	01-02	-400	30	µA
					03-05	-500	30	
			All other 3-state		All	-30	30	
Input current	I_I	$V_I = V_{SS}$ to V_{DD}	$\overline{TRST}$ pin (with internal pulldown)	1,2,3	All	-30	800	µA
			TMS, TCK, TDI pins (with internal pullups)		01-02	-400	30	
					03-05	-500	30	
			X2/CLKIN pin		All	-50	50	
			All other input-only pins			-30	30	mA
Standby supply current	I_{DD1}	IDLE instruction, V_{DD} = Max, f_x = 50 MHz		3	All		30	mA
		IDLE2 instruction, clocks shut off, V_{DD} = Max					7	
Operating supply current	I_{DD2}	V_{DD} = Max, f_x = 40 MHz		3	01		200	mA
		V_{DD} = Max, f_x = 50 MHz			02		250	
		V_{DD} = Max, f_x = 50 MHz			03,05		225	
		V_{DD} = Max, f_x = 66 MHz			04		225	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance (excluding X2CLKIN)	C_{IN}	See 4.4.1 c.	4	01-02		11	pF
				03-05		40	
Output capacitance	C_{OUT}	See 4.4.1 c.	4	01-02		9	pF
				03-05		40	
Functional tests		See 4.4.1 b.	7,8	All			
Cycle time, CLKOUT1	$t_{c(CO)}$	See figure 3 $H = 0.5\ t_{c(CO)}$ External divide-by-two clock option	9,10,11	01,05	50	2/	ns
				02	40	2/	
				03	40	2/	
				04	30	2/	
Delay time, CLKIN high to CLKOUT1 high/low	$t_{d(CIH-CO)}$		9,10,11	01-02	6	20	ns
				03-05	3	20	
Pulse duration, CLKOUT1 low	$t_{w(COL)}$		9,10,11	All	H-3	H+2	ns
Pulse duration, CLKOUT1 high	$t_{w(COH)}$		9,10,11	All	H-3	H+2	ns
Cycle time, CLKIN 3/	$t_{c(CI)}$		9,10,11	01,05	25	2/	ns
				02	20	2/	
				03	20	2/	
				04	15	2/	
Fall time, CLKIN 4/	$t_{f(CI)}$		9,10,11	All		5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise time, CLKIN 4/	$t_{r(CI)}$	See figure 3 H = 0.5 $t_{c(CO)}$ External divide-by-two clock option	9,10,11	All		5	ns
Pulse duration, CLKIN low	$t_{w(CIL)}$		9,10,11	01,05	11	2/	ns
				02	8	2/	
				03	8	2/	
				04	7	2/	
Pulse duration, CLKIN high	$t_{w(CIH)}$		9,10,11	01,05	11	2/	ns
				02	8	2/	
				03	8	2/	
				04	7	2/	
Cycle time, CLKOUT1	$t_{c(CO)}$		9,10,11	01,05	50	4/ 75	ns
				02	40	4/ 75	
				03	40	4/ 75	
				04	30	4/ 75	
Delay time, CLKIN2 high to CLKOUT1 high	$t_{d(CIH-CO)}$		9,10,11	All	2	16	ns
Pulse duration, CLKOUT1 low 4/	$t_{w(COL)}$		9,10,11	All	H-3	H+2	ns
Pulse duration, CLKOUT1 high 4/	$t_{w(COH)}$		9,10,11	All	H-3	H+2	ns
Transitory phase-PLL synchronized after CLKIN2 supplied 4/	t_p		9,10,11	All	256	1000 $t_{C(CI)}$	ns
Cycle time, CLKIN2	$t_{c(C2)}$		9,10,11	01,05	50	4/ 75	ns
				02	40	4/ 75	
				03	40	4/ 75	
				04	30	4/ 75	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Fall time, CLKIN2 4/	$t_{f(C2)}$	See figure 3 H = 0.5 $t_{c(CO)}$ External divide-by-one clock option	9,10,11	All		5	ns
Rise time, CLKIN2 4/	$t_{r(C2)}$		9,10,11	All		5	ns
Pulse duration, CLKIN2 low	$t_{w(CIL)}$		9,10,11	01,05	15	60	ns
				02	11	64	
				03	11	64	
				04	9	66	
Pulse duration, CLKIN2 high	$t_{w(CIH)}$		9,10,11	01,05	15	60	ns
				02	11	64	
				03	11	64	
				04	9	66	
Setup time, address valid before RD low 5/	$t_{u(A)R}$	See figure 3 H = 0.5 $t_{c(CO)}$ Memory and parallel I/O interface read timing	9,10,11	All	H-10		ns
Hold time, address valid after RD high 5/	$t_{h(A)R}$		9,10,11	All	0		ns
Pulse duration, $\overline{RD}$ low 4/ 6/	$t_{w(SL)R}$		9,10,11	01-02	H-8		ns
				03-05	H-2		ns
Pulse duration, $\overline{RD}$ high 4/ 6/	$t_{w(SH)R}$		9,10,11	01-02	H-8		ns
				03-05	H-2		ns
Delay time, $\overline{RD}$ high to $\overline{WE}$ low	$t_{d(D)RW}$		9,10,11	All	2H-5		ns
Access time, read data valid from address valid	$t_{s(A)}$		9,10,11	All		2H-15	ns
Setup time, read data valid before RD high	$t_{su(D)R}$		9,10,11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, address valid before WE low 5/	$t_{su(A)W}$	See figure 3 H = 0.5 $t_{c(CO)}$ Memory and parallel I/O interface write timing	9,10,11	All	H-5		ns
Hold time, address valid after WE high 5/	$t_{h(A)W}$		9,10,11	All	H-10		ns
Hold time, read data valid after RD high	$t_{h(D)R}$		9,10,11	All	0		ns
Access time, read data valid after RD low	$t_{s(R)}$		9,10,11	All		H-10	ns
Pulse duration, $\overline{WE}$ low 7/	$t_{w(SL)W}$		9,10,11	01-02	2H-8		ns
				03-05	2H-4	2H+2 4/	
Pulse duration, $\overline{WE}$ high 7/	$t_{w(SH)W}$		9,10,11	01-02	2H-8		ns
				03-05	2H-4		
Delay time, $\overline{WE}$ high to $\overline{RD}$ low	$t_{d(D)WR}$		9,10,11	All	3H-10		ns
Setup time, write data valid before WE high 7/	$t_{su(D)W}$		9,10,11	All	2H-20	4/ 2H 8/	ns
Hold time, write data valid after WE high 7/	$t_{h(D)W}$		9,10,11	All	H-5	4/ H+10	ns
Enable time, $\overline{WE}$ to data bus driven	$t_{en(D)W}$		9,10,11	All	-5 4/		ns
Setup time, READY before CLKOUT1 rises	$t_{su(R-CO)}$	See figure 3 Ready timing for externally generated wait states	9,10,11	All	10		ns
Hold time, READY after CLKOUT1 rises	$t_{h(CO-R)}$		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, READY before RD falls	$t_{su(R)R}$	See figure 3 Ready timing for externally generated wait states	9,10,11	01-02	15		ns
				03-05	10		
Hold time, READY after RD falls	$t_{h(R)R}$		9,10,11	All	0		ns
Valid time, READY after WE falls	$t_{v(R)W}$		9,10,11	All	H-15		ns
Hold time, READY after WE falls	$t_{h(R)W}$		9,10,11	All	H+5		ns
Setup time, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$, before CLKOUT1 low 9/	$t_{su(IN)}$	See figure 3 H = 0.5 $t_{c(CO)}$ Reset, interrupt, and BIO timings	9,10,11	All	15		ns
Hold time, $\overline{INT1}$-$\overline{INT4}$, $\overline{NMI}$, after CLKOUT1 low 9/	$t_{h(IN)}$		9,10,11	All	0		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, NMI low, synchronous 10/	$t_{w(INL)s}$		9,10,11	All	4H+15		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, NMI high, synchronous 4/ 10/	$t_{w(INH)s}$		9,10,11	All	2H+15		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, NMI low, asynchronous 4/ 10/	$t_{w(INL)a}$		9,10,11	All	6H+15		ns
Pulse duration, $\overline{INT1}$-$\overline{INT4}$, NMI high, asynchronous 4/ 10/	$t_{w(INH)a}$		9,10,11	All	4H+15		ns
Setup time, $\overline{RS}$ before X2/CLKIN low	$t_{su(R)}$		9,10,11	All	10		ns
Pulse duration, $\overline{RS}$ low	$t_{w(RSL)}$		9,10,11	All	12H		ns
Delay time, $\overline{RS}$ high to reset vector fetch	$t_{d(EX)}$		9,10,11	All	34H		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, $\overline{BIO}$ low, synchronous	$t_{w(BI)s}$	See figure 3 Ready timing for externally generated wait states	9,10,11	All	15		ns
Pulse duration, $\overline{BIO}$ low, asynchronous 4/	$t_{w(BI)a}$		9,10,11	All	H+15		ns
Setup time, $\overline{BIO}$ before CLKOUT1 low	$t_{su(BI)}$		9,10,11	All	15		ns
Hold time, $\overline{BIO}$ after CLKOUT1 low	$t_{h(BI)}$		9,10,11	All	0		ns
Setup time, address valid before IAQ low 11/ 12/	$t_{su(A)IAQ}$	See figure 3 $H = 0.5\ t_{c(CO)}$ Instruction acquisition (IAQ), interrupt acknowledge (IACK), external flag (XF), and TOUT timings	9,10,11	All	H-12		ns
Hold time, address valid after IAQ low 12/	$t_{h(A)IAQ}$		9,10,11	All	H-10		ns
Pulse duration, $\overline{IAQ}$ low 12/	$t_{w(IAQL)}$		9,10,11	All	H-10		ns
Delay time, CLKOUT1 falling to TOUT	$t_{d(TOUT)}$		9,10,11	All	-6	6	ns
Setup time, address valid before IACK low 12/ 13/	$t_{su(A)IACK}$		9,10,11	All	H-12		ns
Hold time, address valid after IACK high 12/ 13/	$t_{h(A)IACK}$		9,10,11	All	H-10		ns
Pulse duration, $\overline{IACK}$ low 12/	$t_{w(IACKL)}$		9,10,11	All	H-10		ns
Pulse duration, TOUT	$t_{w(TOUT)}$		9,10,11	All	2H-12		ns
Delay time, XF valid after CLKOUT1	$t_{d(XF)}$		9,10,11	All	0	12	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{HOLD}$ low to HOLDA low 15/	$t_{d(H-HA)}$	See figure 3 H = 0.5 $t_{c(CO)}$ External DMA timing 14/	9,10,11	All	4H		ns
Delay time, $\overline{HOLD}$ high before HOLDA high	$t_{d(H-HA)}$		9,10,11	All	2H		ns
Disable time, address 3-state before HOLDA low 4/ 16/	$t_{dis(M-HA)}$		9,10,11	All	H-15		ns
Enable time, $\overline{HOLDA}$ high to address driven 4/	$t_{en(HA-M)}$		9,10,11	All	H-5		ns
Delay time, $\overline{XBR}$ low to IAQ low 4/	$t_{d(B-I)}$	See figure 3 H = 0.5 $t_{c(CO)}$ External DMA timing 14/	9,10,11	All	4H	6H	ns
Delay time, $\overline{XBR}$ high to IAQ high 4/	$t_{d(BH-I)}$		9,10,11	All	2H	4H	ns
Delay time, read data valid after XSTRB low	$t_{d(D)XR}$		9,10,11	All		40	ns
Hold time, read data after XSTRB high	$t_{h(D)XR}$		9,10,11	All	0		ns
Enable time, $\overline{IAQ}$ low to read data driven 4/ 17/	$t_{en(I-D)}$		9,10,11	All	0	2H	ns
Disable time, XR/$\overline{W}$ low to data 3-state 4/	$t_{dis(W)}$		9,10,11	All	0	15	ns
Disable time, $\overline{IAQ}$ high to data 3-state 4/	$t_{dis(I-D)}$		9,10,11	All		H	ns
Enable time, data from XR/W going high 4/	$t_{en(D)RW}$		9,10,11	All		4	ns
Delay time, $\overline{HOLDA}$ low to XBR low 18/	$t_{d(HA-B)}$		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, Write Xaddress hold after XSTRB low	$t_{h(XA)W}$	See figure 3 H = 0.5 $t_{c(CO)}$ External DMA timing 14/	9,10,11	All	15		ns
Delay time, IAQ low to XSTRB low 18/	$t_{d(I-XS)}$		9,10,11	All	0		ns
Setup time, Xaddress valid before XSTRB low	$t_{su(XA)}$		9,10,11	All	15		ns
Setup time, Xdata valid before XSTRB low	$t_{su(XD)W}$		9,10,11	All	15		ns
Hold time, Xdata hold after XSTRB low	$t_{h(WD)W}$		9,10,11	All	15		ns
Pulse duration, XSTRB low	$t_{w(XSL)}$		9,10,11	All	45		ns
Pulse duration, XSTRB high	$t_{w(XSH)}$		9,10,11	All	45		ns
Setup time, R/W valid before XSTRB low	$t_{su(XS)RW}$		9,10,11	All	20		ns
Hold time, read Xaddress after XSTRB high	$t_{h(XA)R}$		9,10,11	All	0		ns
Cycle time, serial port clock 19/	$t_{c(SCK)}$	See figure 3 H = 0.5 $t_{c(CO)}$ Serial port receive timing	9,10,11	All	5.2H		ns
Fall time, serial port clock 4/	$t_{f(SCK)}$		9,10,11	All		8	ns
Rise time, serial port clock 4/	$t_{r(SCK)}$		9,10,11	All		8	ns
Pulse duration, serial port clock low/high	$t_{w(SCK)}$		9,10,11	All	2.1H		ns
Setup time, FSR before CLKR falling edge	$t_{su(FS)}$		9,10,11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, FSR after CLKR falling edge	$t_{h(FS)}$	See figure 3 $H = 0.5\ t_{c(CO)}$ Serial port receive timing	9,10,11	All	10		ns
Setup time, DR before CLKR falling edge	$t_{su(DR)}$		9,10,11	All	10		ns
Hold time, DR after CLKR falling edge	$t_{h(DR)}$		9,10,11	All	10		ns
Delay time, DX valid after CLKX rising	$t_{d(DX)}$	See figure 3 $H = 0.5\ t_{c(CO)}$ Serial port transmit timing of external clocks and external frames 20/	9,10,11	All		25	ns
Disable time, DX valid after CLKX rising 4/	$t_{dis(DX)}$		9,10,11	All		40	ns
Hold time, DX valid after CLKX rising	$t_{h(DX)}$		9,10,11	01-02	-6		ns
				03-05	-5		
Cycle time, serial port clock 19/	$t_{c(SCK)}$		9,10,11	All	5.2H		ns
Fall time, serial port clock 4/	$t_{f(SCK)}$		9,10,11	All		8	ns
Rise time, serial port clock 4/	$t_{r(SCK)}$		9,10,11	All		8	ns
Pulse duration, serial port clock low/high	$t_{w(SCK)}$		9,10,11	All	2.1H		ns
Delay time, FSX after CLKX rising edge	$t_{d(FS)}$		9,10,11	All		2H-8	ns
Hold time, FSX after CLKX falling edge	$t_{h(FS)}$		9,10,11	All	10		ns
Hold time, FSX after CLKX rising edge 4/ 21/	$t_{h(FS)H}$		9,10,11	All		2H-8	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $Min \le V_{DD} \le Max$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, CLKX rising to FSX	$t_{d(FS)}$	See figure 3 $H = 0.5\ t_{c(CO)}$ Serial port transmit timing of internal clocks and internal frames 20/	9,10,11	All		25	ns
Delay time, CLKX rising to DX	$t_{d(DX)}$		9,10,11	All		25	ns
Disable time, CLKX rising to DX 4/	$t_{dis(DX)}$		9,10,11	All		40	ns
Pulse duration, serial port clock low/high	$t_{w(SCK)}$		9,10,11	All	4H-20		ns
Hold time, DX valid after CLKX rising	$t_{h(DX)}$		9,10,11	All	-6		ns
Cycle time, serial port clock 19/	$t_{c(SCK)}$	See figure 3 $H = 0.5\ t_{c(CO)}$ Serial port receive timing in TDM mode	9,10,11	All	5.2H		ns
Fall time, serial port clock 4/	$t_{f(SCK)}$		9,10,11	All		8	ns
Rise time, serial port clock 4/	$t_{r(SCK)}$		9,10,11	All		8	ns
Pulse duration, serial port clock low/high	$t_{w(SCK)}$		9,10,11	All	2.1H		ns
Setup time, TDAT/TADD before TCLK rising	$t_{su(LB)}$		9,10,11	All	30		ns
Hold time, TDAT/TADD after TCLK rising	$t_{h(LB)}$		9,10,11	All	-3		ns
Setup time, TDAT/TADD before TCLK rising 22/	$t_{su(SB)}$		9,10,11	All	20		ns
Hold time, TDAT/TADD after TCLK rising 22/	$t_{h(SB)}$		9,10,11	All	-3		ns
Setup time, TRFM before TCLK rising edge 23/	$t_{su(FS)}$		9,10,11	All	10		ns
Hold time, TRFM after TCLK rising edge 23/	$t_{h(FS)}$		9,10,11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ Min $\le V_{DD} \le$ Max 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, TDAT/TADD valid after TCLK rising	$t_{h(AD)}$	See figure 3 H = 0.5 $t_{c(CO)}$ Serial port transmit timing	9,10,11	All	0		ns
Delay time, TFRM valid after TCLK rising	$t_{d(FS)}$		9,10,11	All	H	3H+10	ns
Delay time, TCLK to valid TDAT/TADD	$t_{d(AD)}$		9,10,11	All		20	ns
Cycle time, serial port clock 19/	$t_{c(SCK)}$		9,10,11	All	5.2H		ns
Fall time, serial port clock 4/	$t_{f(SCK)}$		9,10,11	All		8	ns
Rise time, serial port clock 4/	$t_{r(SCK)}$		9,10,11	All		8	ns
Pulse duration, serial port clock low/high	$t_{w(SCK)}$		9,10,11	All	2.1H		ns

1/ Unless otherwise specified all test conditions are worst case condition.
Clocks can be stopped only while the device executes IDLE2 when using the external divide-by-one clock option. Note that t_p (the transitory phase) will occur when restarting clock from IDLE2 in this mode.

2/ All input and output voltage levels are TTL-compatible. Figure 3 shows the tested load circuit and the voltage reference levels.

3/ This device utilizes a fully static design and therefore can operate with $t_{c(Cl)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 6.7 MHz to meet device test time requirements.

4/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I. Values are either derived from characterization data or specified by design thereafter.

5/ $\overline{A15}$-$\overline{A0}$, $\overline{PS}$, $\overline{DS}$, IS, R/$\overline{W}$, and BR timings are all included in timings referenced as address.

6/ $\overline{STRB}$ timing is -3/+5 ns from CLKOUT1 timing on read cycles, following the first cycle after reset, which is always a 7 wait-state cycle.

7/ $\overline{STRB}$ and $\overline{WE}$ edges are 0-4 ns from CLKOUT1 edges on writes. Rising and falling edges of these signals track each other; tolerance of resulting pulse durations is ±2 ns, not ±4 ns.

8/ This value holds true for zero or one wait state only.

9/ These parameters must be met to use the synchronous timing. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to assure internal synchronization.

10/ If in IDLE2, add 4H to these timings.

TABLE I. Electrical performance characteristics - Continued.

11/ $\overline{IAQ}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the MPST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.

12/ Valid only if the external address reflects the current instruction activity (that is, code is executing on chip with no external bus cycles and AVIS is on, or code is executing off-chip).

13/ $\overline{IACK}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the PMST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.

14/ X preceding a name refers to external drive of the signal.

15/ $\overline{HOLD}$ is not acknowledged until current external access request is complete.

16/ This parameter includes all memory control lines.

17/ This parameter refers to the delay between the time the condition ($\overline{IAQ}$ = 0 and XR/$\overline{W}$ = 1) is satisfied and the time that the device data lines become valid.

18/ $\overline{XBR}$, XR/$\overline{W}$, and $\overline{XSTRB}$ lines should be pulled up with a 10-kΩ resistor to assure that they are in an inactive (high) state during the transition period between the device driving them and the external circuit driving them.

19/ The serial port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

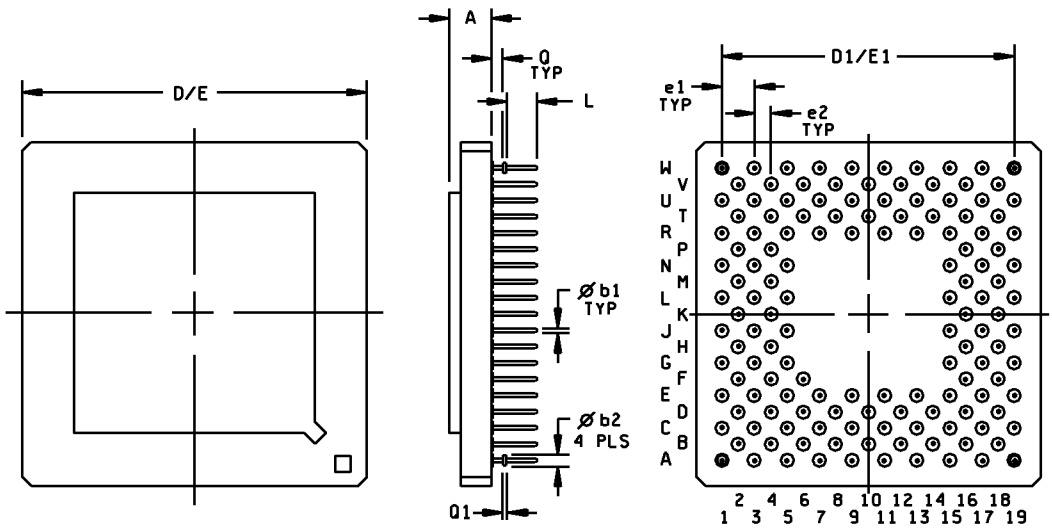
20/ Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

21/ If the FSX pulse does not meet this specification, the first bit of serial data will be driven on the DX pin until the falling edge of FSX. After the falling edge of FSX, data will be shifted out on the DX pin. The transmit-buffer-empty interrupt will be generated when the $t_{h(FS)}$ and $t_{h(FS)H}$ specification is met.

22/ These parameters apply only to the first bits in the serial bit string.

23/ TFRM timing and waveforms shown in Figure 3 are from external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 3.

Case X



Letter	Millimeters		Inches	
	Min	Max	Min	Max
A	2.79	3.68	0.110	0.145
b1	0.41	0.56	0.016	0.022
b2	1.22		0.048	
D/E	26.42	27.43	1.040	1.080
D1/E1	22.86 BSC		0.900 BSC	
e1	2.54 BSC		0.100 BSC	
e2	1.27 BSC		0.050 BSC	
L	3.05	3.56	0.120	0.140
Q	0.86		0.034	
Q1	0.15	0.66	0.006	0.026

Figure 1. Case outline

Case Y

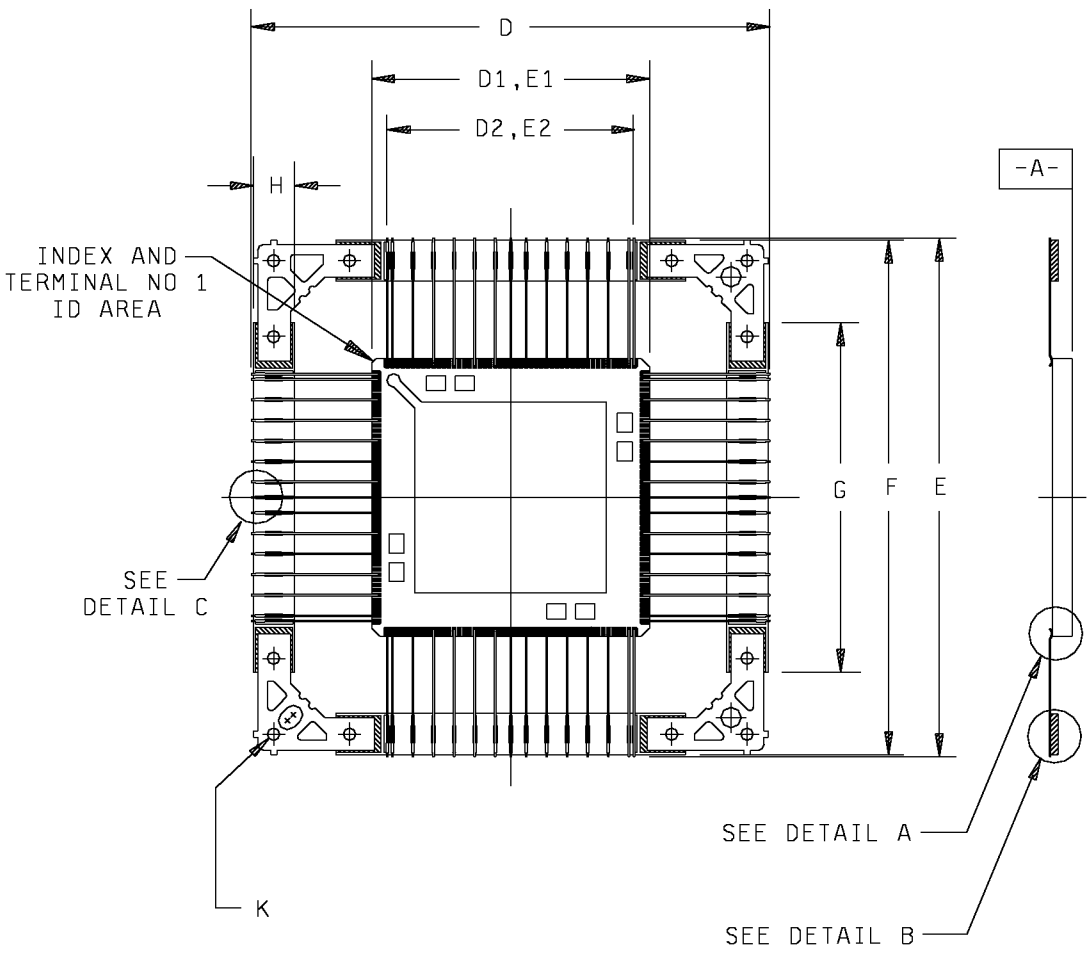
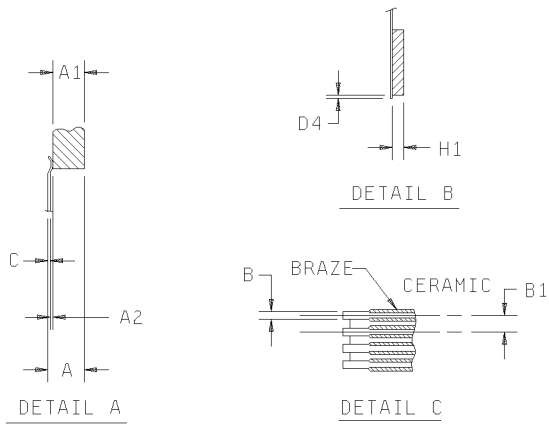


FIGURE 1. Case outline. - Continued

Case Y



Letter	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	0.116	---	2.95	
A1	---	0.091	---	2.31	
A2	0.002	0.014	0.05	0.35	At braze pads
B	0.009	0.016	0.22	0.41	
B1	0.025 BSC		0.064 BSC		
C	0.005	0.010	0.12	0.26	
D	---	2.025	---	51.44	
D1,E1	0.945	0.960	24.00	24.38	
D2,E2	0.800 BSC		20.32 BSC		
D4	0.005 BSC		0.13 BSC		
E	- - -	2.025	- - -	51.44	
F	1.990	2.015	50.55	51.18	Tie bar dimension
G	1.210 BSC		30.73 BSC		Tie bar dimension
H	0.195	0.205	4.95	5.21	Tie bar dimension
H1	0.030	0.040	0.76	1.02	Tie bar dimension
K	0.058	0.062	1.4	1.57	4 places

NOTE:All linear dimensions are in inches. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier.
FIGURE 1. Case outline - Continued.

Case Z

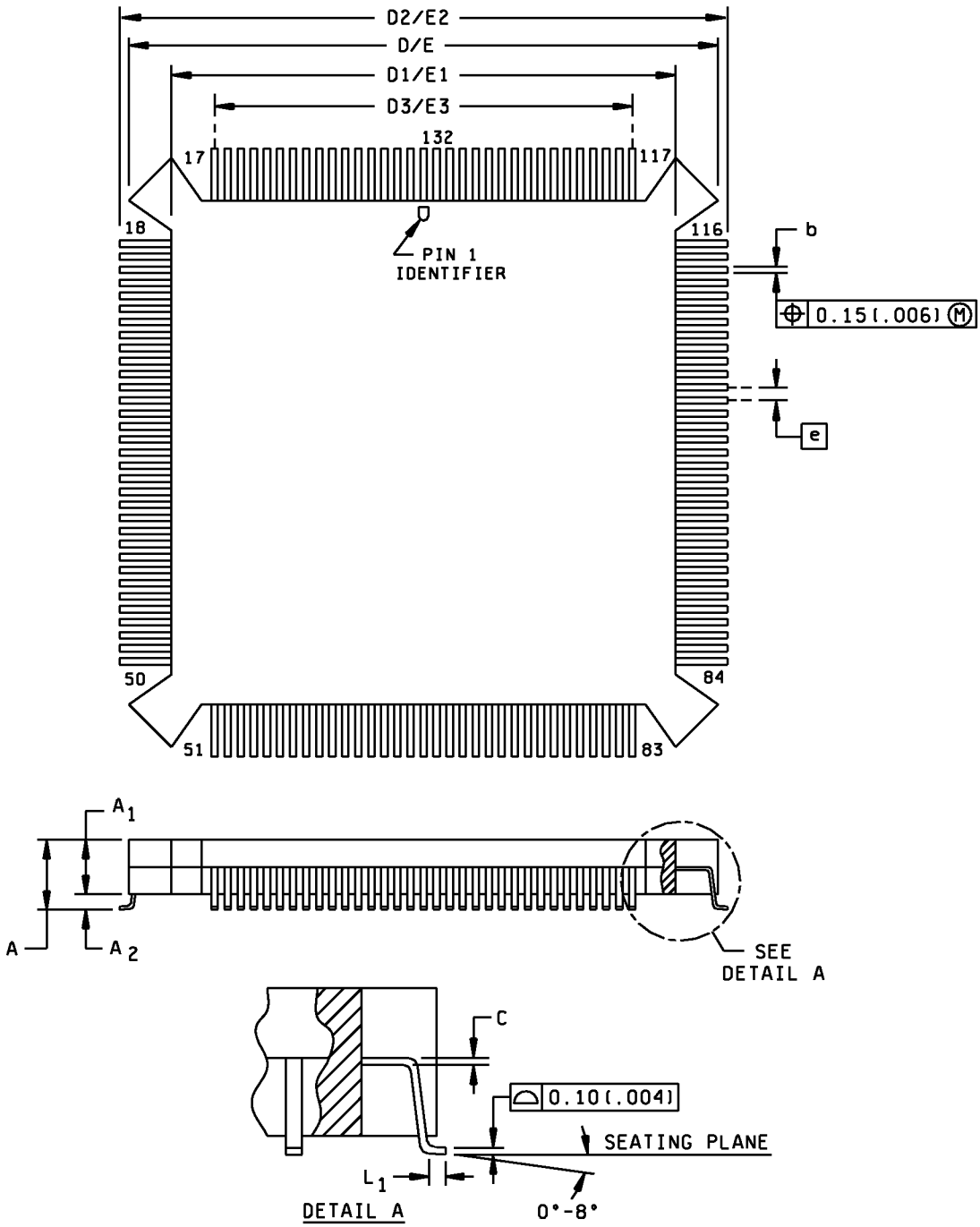


FIGURE 1. Case outline - Continued.

Case Z

Dimensions				
Ltr	Millimeters		Inches	
	Min	Max	Min	Max
A		4.57		.180
A_1	3.30	3.81	.130	.150
A_2		0.51	20.020	
b	0.20	0.30	.008	.012
c	0.16 BSC		.006 BSC	
D	27.18	27.69	1.070	1.090
D1	23.72	24.54	.934	.966
D2	27.64	28.25	1.088	1.112
D3	20.32 BSC		.800 BSC	
e	0.635 BSC		.025 BSC	
L_1	0.91	1.17	.036	.046

FIGURE 1. Case outline - Continued.

PIN NO.						
Case Z	CASE Y	CASE X	SIGNAL NAME		TYPE	DESCRIPTION
18	1		NC			Reserved
19	2		NC			Reserved
20	3	D8	V_{SS}		Supply	Ground
21	4	D10	V_{SS}		Supply	Ground
22	5		NC			Reserved
23	6	E3	D7		I/O/Z	Parallel data port, high-byte (8-pins)
24	7	D2	D6		I/O/Z	
25	8	C1	D5		I/O/Z	
26	9	G3	D4		I/O/Z	
27	10	F2	D3		I/O/Z	
28	11	E1	D2		I/O/Z	
29	12	J3	D1		I/O/Z	
30	13	H2	D0 (LSB)		I/O/Z	
31	14	G1	TMS		I	JTAG test mode
32	15	C3	V_{DD}		Supply	+5 V
33	16	D4	V_{DD}		Supply	+5 V
34	17	J1	TCK		I	JTAG test clock
35	18	D12	V_{SS}		Supply	Ground
36	19	F4	V_{SS}		Supply	Ground
37	20		NC			Reserved
38	21	L1	$\overline{INT1}$		I	Interrupt #1
39	22	N1	$\overline{INT2}$		I	Interrupt #2
40	23	M2	$\overline{INT3}$		I	Interrupt #3
41	24	L3	$\overline{INT4}$		I	Interrupt #4
42	25	R1	$\overline{NMI}$		I	Nonmaskable interrupt
43	26	P2	DR		I	Serial Port 1 data receive
44	27	N3	TDR		I	Serial Port 2 data receive
45	28	T2	FSR		I	Serial Port 1 receiver frame sync
46	29	R3	CLKR		I	Serial Port 1 receiver clock
47	30	E5	V_{DD}		Supply	+5 V
48	31	E7	V_{DD}		Supply	+5 V
49	32		NC			Reserved
50	33		NC			Reserved
51	34		NC			Reserved
52	35		NC			Reserved
53	36	H4	V_{SS}		Supply	Ground
54	37	K2	V_{SS}		Supply	Ground
55	38	U5	A0 (LSB)		I/O/Z	Parallel port address bus (10 pins)
56	39	V4	A1	I/O/Z		
57	40	W3	A2	I/O/Z		
58	41	U7	A3	I/O/Z		
59	42	V6	A4	I/O/Z		
60	43	W5	A5	I/O/Z		
61	44	U9	A6	I/O/Z		
62	45	V8	A7	I/O/Z		
63	46	W7	A8	I/O/Z		
64	47	W9	A9	I/O/Z		
65	48	E9	V_{DD}		Supply	+5 V
66	49	E11	V_{DD}		Supply	+5 V
67	50	V10	TDI		I	JTAG scan input

FIGURE 2. Terminal connections.

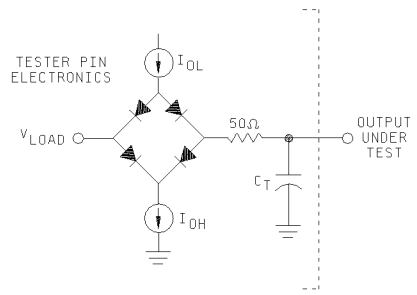
PIN no.					
Case Z	Case Y	Case X	Signal name	Type	Description
68	51	K4	V_{SS}	Supply	Ground
69	52	M4	V_{SS}	Supply	Ground
70	53		NC		Reserved
71	54	W11	CLKMD1	I	Clock mode pin 1
72	55	W13	A10	I/O/Z	Parallel port address bus (6 pins)
73	56	V12	A11	I/O/Z	
74	57	U11	A12	I/O/Z	
75	58	W15	A13	I/O/Z	
76	59	V14	A14	I/O/Z	
77	60	U13	A15	I/O/Z	
78	61		NC		Reserved
79	62		NC		Reserved
80	63	E13	V_{DD}	Supply	+5 V
81	64	G5	V_{DD}	Supply	+5 V
82	65	V16	$\overline{RD}$	O/Z	Read enable
83	66	U15	$\overline{WE}$	O/Z	Write enable
84	67		NC		Reserved
85	68		NC		Reserved
86	69	P4	V_{SS}	Supply	Ground
87	70	T4	V_{SS}	Supply	Ground
88	71		NC		Reserved
89	72	R17	$\overline{DS}$	O/Z	Data space select
90	73	T18	$\overline{IS}$	O/Z	I/O space select
91	74	U19	$\overline{PS}$	O/Z	Program space select
92	75	N17	R/$\overline{W}$	I/O/Z	Read/Write
93	76	P18	$\overline{STRB}$	I/O/Z	External parallel access active
94	77	R19	$\overline{BR}$	I/O/Z	Bus request
95	78	L17	CLKIN2	I	Divide-by-one clock input
96	79	M18	X2/CLKIN2	I	Divide-by-two clock input
97	80	N19	X1	O	Oscillator output
98	81	J5	V_{DD}	Supply	+5 V
99	82	L5	V_{DD}	Supply	+5 V
100	83	L19	TDO	O/Z	JTAG scan output
101	84	T6	V_{SS}	Supply	Ground
102	85	T8	V_{SS}	Supply	Ground
103	86	K18	CLKMD2	I	Clock mode pin 2
104	87	J19	FSX	I/O/Z	Serial port 1 transmitter frame sync
105	88	G19	TFSX/TFRM	I/O/Z	Serial port 2 transmitter frame sync
106	89	H18	DX	O/Z	Serial port 1 transmitter output
107	90	J17	TDX	O/Z	Serial port 2 transmitter output
108	91	E19	HOLDA	O/Z	Hold acknowledge
109	92	F18	XF	O/Z	External flag
110	93	G17	CLKOUT1	O/Z	Machine clock output
111	94		NC		Reserved
112	95	E17	$\overline{IACK}$	O/Z	Interrupt acknowledge
113	96	N5	V_{DD}	Supply	+5 V
114	97	R5	V_{DD}	Supply	+5 V
115	98		NC		Reserved
116	99		NC		Reserved
117	100		NC		Reserved

FIGURE 2. Terminal connections - Continued.

PIN no.					
Case Z	Case Y	Case X	Signal name	Type	Description
118	101	B18	EMU0	I/O/Z	Emulator interrupt 0
119	102	A19	EMU1/$\overline{OFF}$	I/O/Z	Emulator interrupt 1
120	103	T10	V_{SS}	Supply	Ground
121	104	T12	V_{SS}	Supply	Ground
122	105	C15	TOUT	O/Z	Timer output
123	106	B16	TCLKX	I/O/Z	Serial port 2 transmitter clock
124	107	A17	CLKX	I/O/Z	Serial port 1 transmitter clock
125	108	C13	TFSR/TADD	I/O/Z	Serial port 2 receive frame/address
126	109	B14	TCLKR	I	Serial port 2 receiver clock
127	110	A15	$\overline{RS}$	I	Device reset
128	111	C11	READY	I	External access ready to complete
129	112	B12	$\overline{HOLD}$	I	Request access of local memory
130	113	A13	$\overline{BIO}$	I	Bit I/O pin
131	114	R7	V_{DD}	Supply	+5 V
132	115	R7	V_{DD}	Supply	+5 V
1	116	A11	$\overline{IAQ}$	O/Z	Instruction acquisition
2	117	A9	$\overline{TRST}$	I	JTAG test request
3	118	B10	V_{SS}	Supply	Ground
4	119	D6	V_{SS}	Supply	Ground
5	120	A7	MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select
6	121	B8	D15 (MSB)	I/O/Z	Parallel data port, high-byte (8 pins)
7	122	C9	D14	I/O/Z	
8	123	A5	D13	I/O/Z	
9	124	B6	D12	I/O/Z	
10	125	C7	D11	I/O/Z	
11	126	A3	D10	I/O/Z	
12	127	B4	D9	I/O/Z	
13	128	C5	D8	I/O/Z	
14	129	A1	V_{DD}	Supply	+5 V
15	130	B2	V_{DD}	Supply	+5 V
16	131		NC		Reserved
17	132		NC		Reserved

NOTES: NC = No Connect.
Case X additional connections:
V_{DD}: R11, E15, G15,J15, L15, N15, R13, R15, T16, U17, V18, W17, W19
V_{SS}: T14, U1, U3, V2, W1, C17, C19, D14, D16, D18, F16, H16, K16, M16, P16

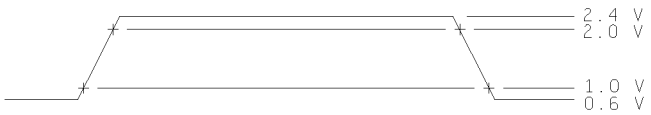
FIGURE 2. Terminal connections - Continued.



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 80 pF typical load circuit capacitance.

Test load circuit

TTL-output levels are driven to a minimum logic-high level of 2.4 volts and to a maximum logic-low level of 0.6 volt.



TTL-level outputs

TTL-output transition times are specified as follows:

For a high-to-low transition, the level at which the output is said to be no longer high is 2.0 volts, and the level at which the output is said to be low is 1.0 volt.

For a low-to-high transition, the level at which the output is said to be no longer low is 1.0 volt, and the level at which the output is said to be high is 2.0 volts.

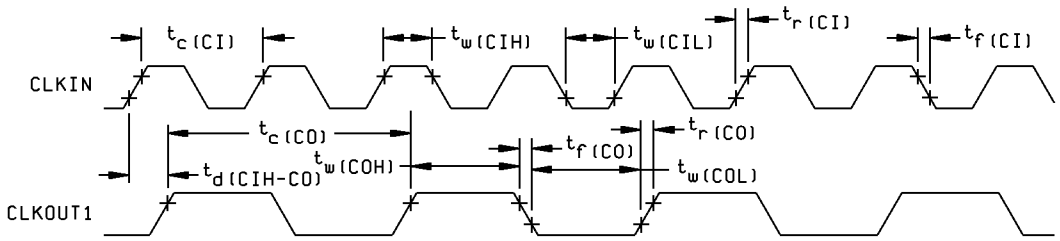
TTL-compatible input transition times are specified as follows:

For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2.0 volts, and the level at which the input is said to be low is 0.8 volt.

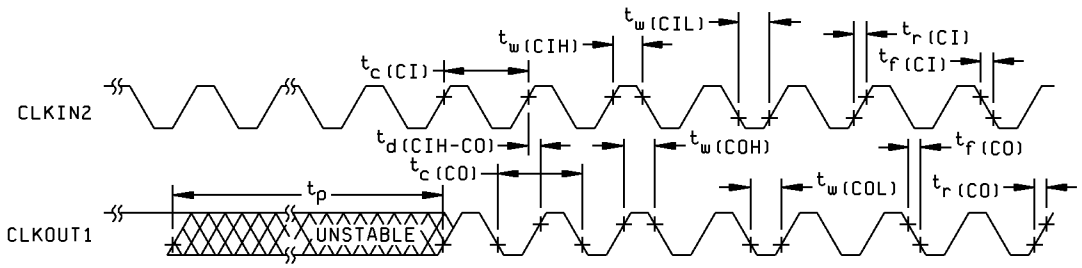
For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 volt, and the level at which the input is said to be high is 2.0 volts.

TTL-level inputs

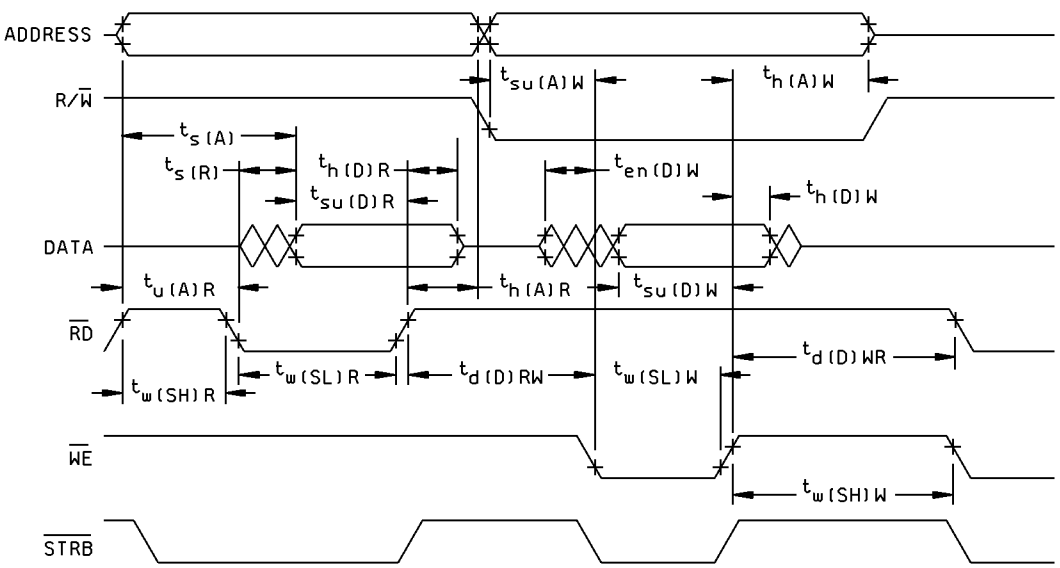
FIGURE 3. Timing waveforms



EXTERNAL DIVIDE-BY-TWO CLOCK TIMING



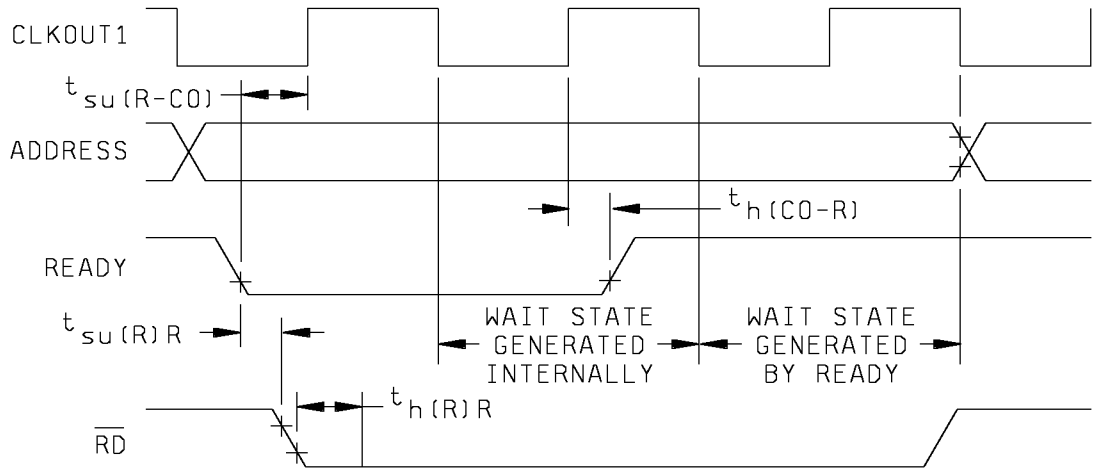
EXTERNAL DIVIDE-BY-ONE CLOCK TIMING



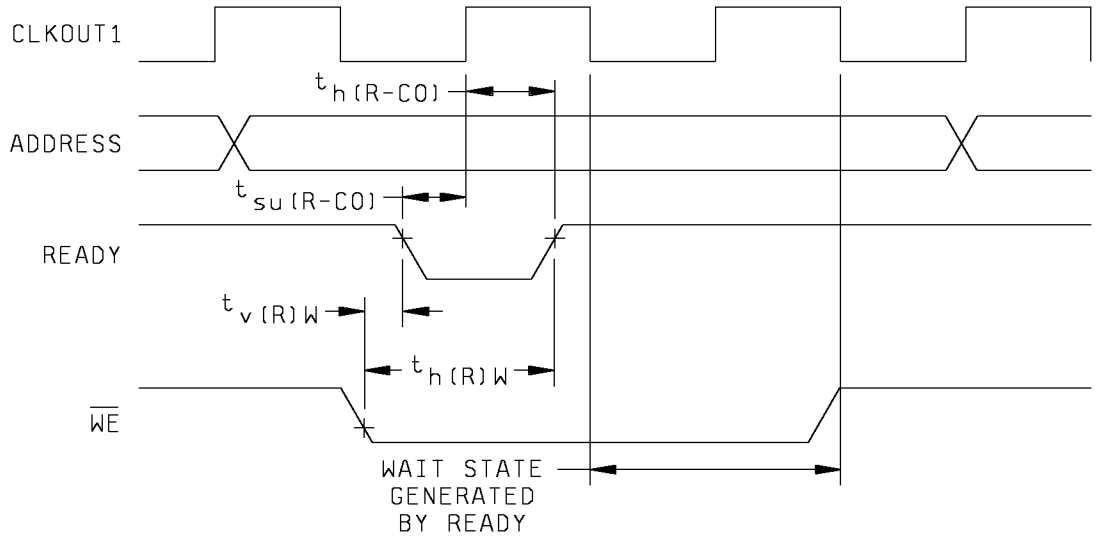
MEMORY AND PARALLEL I/O INTERFACE READ AND WRITE TIMING

NOTE: All timings are for 0 wait states. However, external writes always require two cycles to prevent external bus conflicts. The above diagram illustrates a one-cycle read and a two-cycle write and is not drawn to scale. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycle.

FIGURE 3. Timing waveforms - Continued.

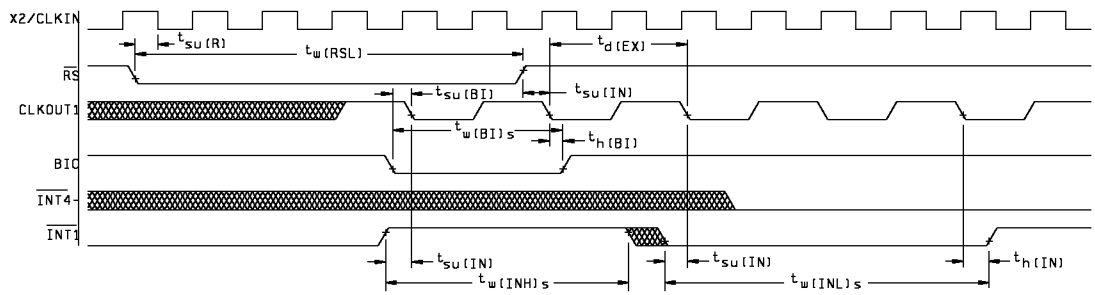


Ready timing for externally generated wait states during an external read cycle

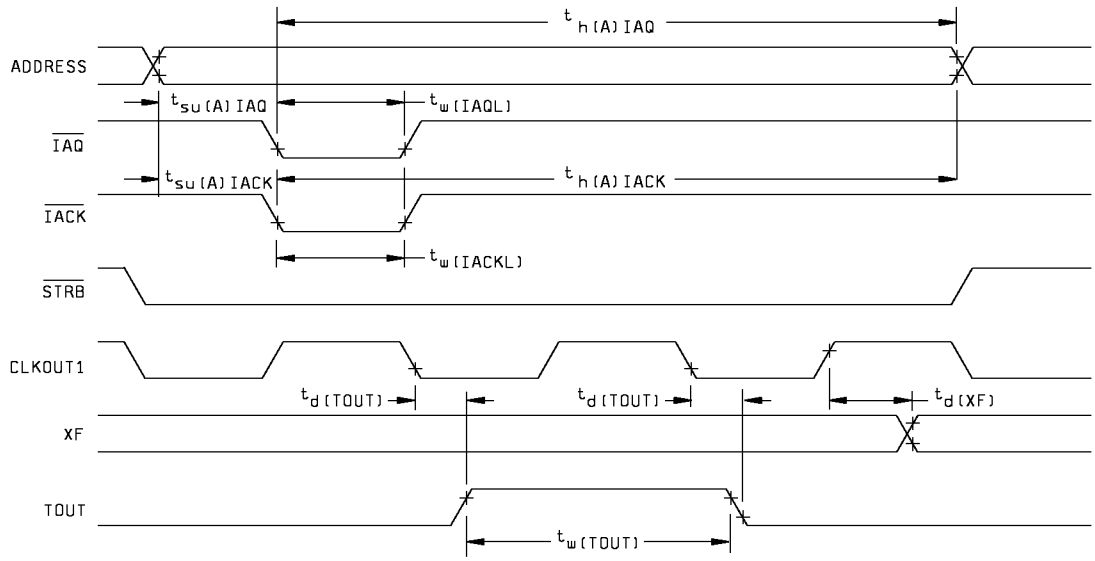


Ready timing for externally generated wait states during an external write cycle

FIGURE 3. Timing waveforms - Continued.



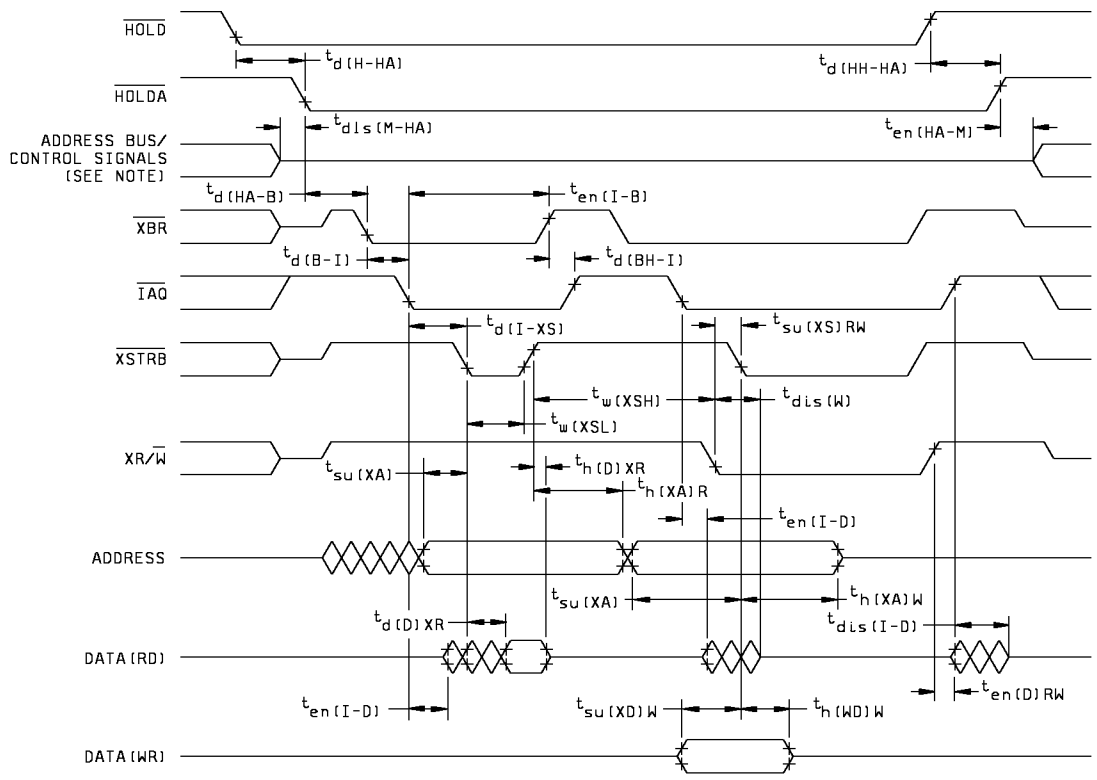
Reset, interrupt, and BIO timings



NOTE: IAQ and IACK are not affected by wait states.

IAQ, IACK, and XF timings example with two external wait states

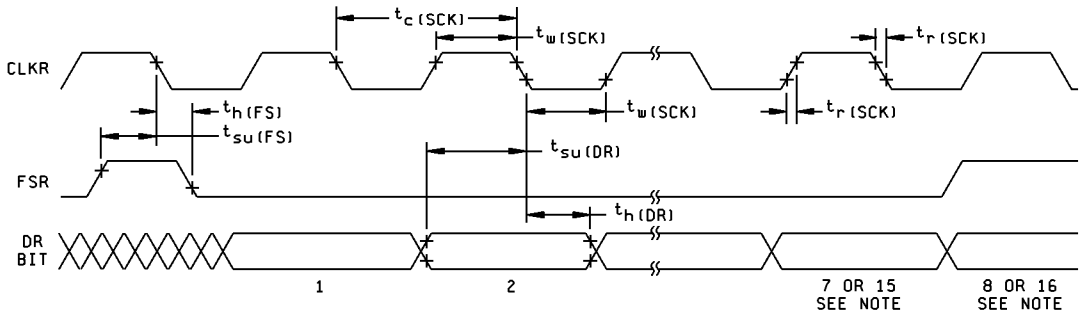
FIGURE 3. Timing waveforms - Continued.



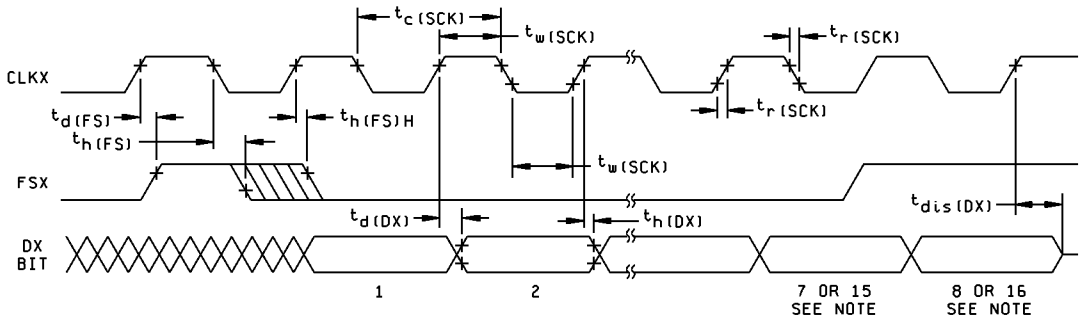
EXTERNAL DMA TIMING

NOTE:
A15 - A0, PS, DS, IS, R/W, and BR timings are all included in timings referenced as address bus/control signals.

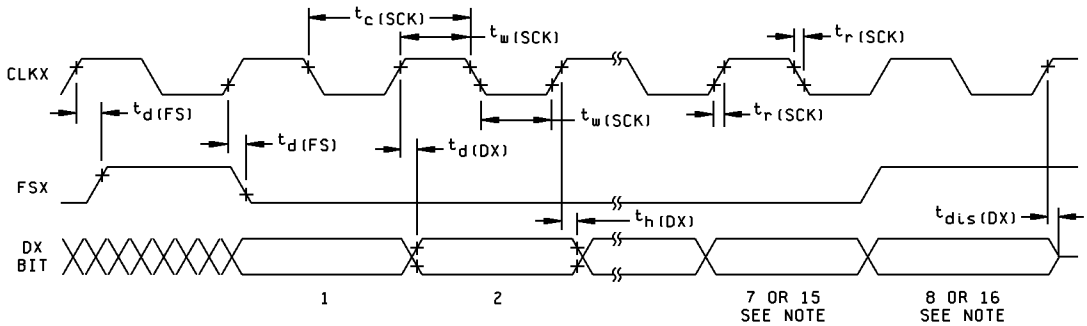
FIGURE 3. Timing waveforms - Continued.



SERIAL PORT RECEIVING TIMING



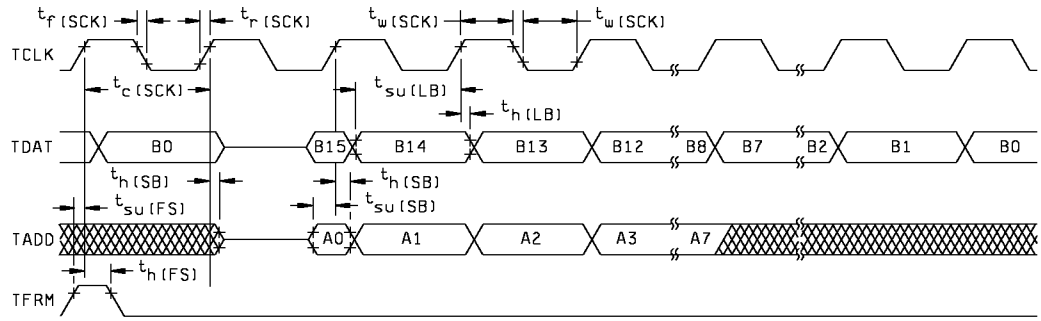
SERIAL PORT TRANSMIT TIMING OF EXTERNAL CLOCKS AND EXTERNAL FRAMES



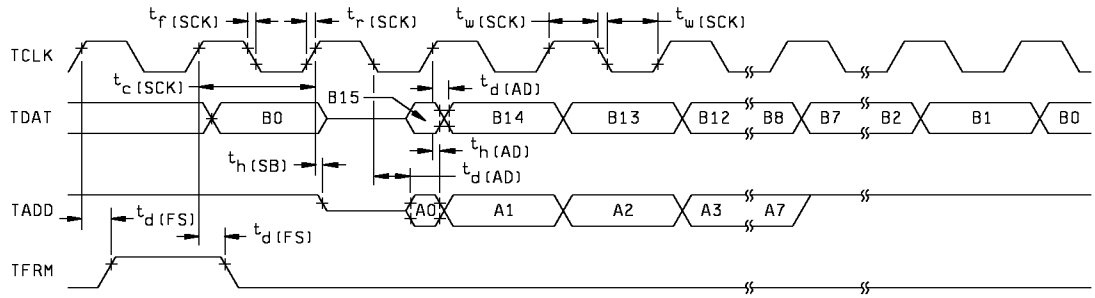
SERIAL PORT TRANSMIT TIMING OF INTERNAL CLOCKS AND INTERNAL FRAMES

NOTE: Depending on whether information is sent in an 8-bit or 16-bit packet.

FIGURE 3. Timing waveforms - Continued.



SERIAL PORT RECIEVE TIMING IN TDM MODE



SERIAL PORT TRANSMIT TIMING IN TDM MODE

FIGURE 3. Timing waveforms - Continued.

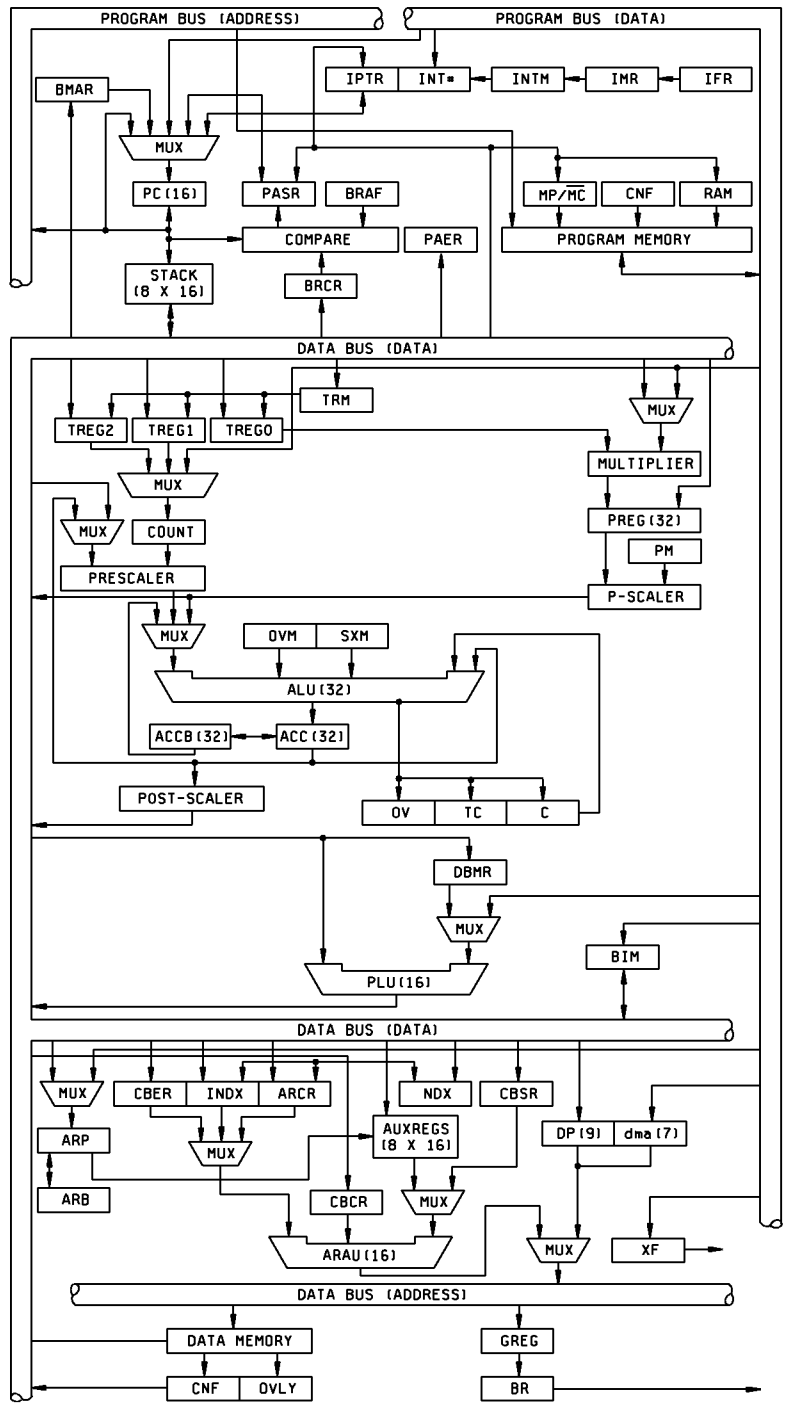


FIGURE 4. Functional block diagram.

Internal hardware summary

Unit	Symbol	Function
Accumulator	ACC(32) ACCH(16) ACCL(16)	A 32-bit accumulator accessible in two halves: ACCH (accumulator high) and ACCL (accumulator low). Used to store the output of the ALU.
Accumulator buffer	ACCB(32)	A register used to temporarily store the 32-bit contents of the accumulator. This register has a direct path back to the ALU and therefore can be arithmetically or logically acted upon with the ACC.
Arithmetic logic unit	ALU	A 32-bit twos-compliment arithmetic logic unit having two 32-bit input ports and one 32-bit output port feeding the accumulator.
Auxiliary register arithmetic unit	ARAU	An unsigned 16-bit arithmetic unit used to calculate indirect addresses using the auxiliary, index, and compare registers as inputs.
Auxiliary register compare	ARCR(16)	A 16-bit register used as a limit to compare indirect address against.
Auxiliary register file	AUXREGS	A register file containing eight 16-bit auxiliary registers (AR0-AR7) used for indirect data address pointers, temporary storage, or integer arithmetic processing through the ARAU.
Auxiliary register buffer	ARB(3)	A 3-bit register that holds the previoius value contained in the ARP. These bits are stored in ST1.
Auxiliary register pointer	ARP(3)	A 3-bit register used as a pointer to the currently selected auxiliary register. These bits are stored in ST0.
Block move address register	BMAR(16)	A 16-bit register that holds an address value for use with block moves or multiply/accumulates.
Block repeat active flag	BRAF(1)	A 1-bit flag indicating that a block repeat is currently active. This bit is normally set when the RPTB instruction is executed and cleared when the BRCR register decrements below zero. This bit resides in the PMST register.
Block repeat address end register	PAER(16)	A 16-bit memory-mapped register containing the end address of the segment of code being repeated.
Block repeat address start register	PASR(16)	A 16-bit memory-mapped register containing the start address of the segment of code being repeated.
Block repeat counter register	BRCR(16)	A 16-bit memory-mapped counter register used to limit the number of times the block is to be repeated.
Bus interface module	BIM	A buffered interface used to pass data between the internal data and program buses.
Bus request	$\overline{BR}$	This signal indicates that a data access is mapped to global memory space as defined by the GREG register.
Carry	C	This bit stores the carry output of the ALU. This bit resides in ST1.
Central arithmetic logic unit	CALU	The grouping of the ALU, multiplier, accumulator, and scaling shifters.
Circular buffer control register	CBCR(8)	An 8-bit register used to enable/disable the circular buffers and define which auxiliary registers are mapped to the circular buffers.

FIGURE 4. Functional block diagram - Continued.

Internal hardware summary - Continued.

Unit	Symbol	Function
Circular buffer	CBER(16)	Two 16-bit registers indicating circular buffer end addresses. CBER1 and end address CBER1(16)CBER2 are associated with circular buffers one and two, respectively. CBER2(16)
Circular buffer	CBSR(16)	Two 16-bit registers indicating circular buffer start addresses. CBSR1 and start address CBSR1(16)CBSR2 are associated with circular buffers one and two, respectively. CBSR2(16)
Compare of program	COMPARE	This circuit compares the current value in the PC to the value in PAER if address BRAF is active. If the compare shows equal, then the PASR is loaded into the PC.
Configure	RamCNF	This bit indicates whether on-chip dual-access RAM blocks are mapped to program or data space. The CNF bit resides in ST1.
Data bus	DATA	A 16-bit bus used to route data.
Data memory	Data	This block refers to data memory used with the core and defined in specific MEMORY device descriptions. It refers to both on- and off-chip memory blocks indata memory space.
Data memory	DATA	A 16-bit bus that carries the address for data memory accesses. Address bus ADDRESS
Data memory address	DMA(7)	A 7-bit register containing the immediate relative address within a 128-word immediate registerdata page.
Data memory page	DP(9)	A 9-bit register containing the address of the current page. Data pages are pointer 128 words each, resulting in 512 pages of addressable data memory space(some locations are reversed).
Data RAM map bit	RAM(1)	This bit indicates if the single-access RAM is mapped into data space.
Direct data memory	DRB(16)	A 16-bit bus that carries the direct address for the data memory, which the address bus concatenation of the DP register and the seven LSBs of the instruction (DMA).
Dynamic bit	DBMR(16)	A 16-bit memory-mapped register used as a mask input to the PLU in the manipulation register absence of a long immediate value.
Dynamic bit pointer	TREG2(4)	A 4-bit register that holds a dynamic bit pointer for the BITT instruction.
Dynamic shift count	TREG1(5)	A 5-bit register that holds a dynamic prescaling shift count for data inputsto the ALU.
External Flag	XF(1)	This bit drives the level of the external flag pin and resides in ST1.
Global memory	GREG(8)	An 8-bit memory-mapped register for specifying the size of the global memory allocation register space.
Hold mode	HM(1)	This bit resides in ST1 and determines whether the CALU will stop or continue when the HOLD signal initiates a power-down mode.
Index register	INDX(16)	This 16-bit memory-mapped register specifies increment sizes greater than 1 for indirect addressing updates. In bit-reversed addressing, the index register defines the array size.
Index register enable	NDX(1)	This bit determines whether a modification or write to AR0 writes also to INDX and ARCR to maintain compatibility with the device. This bit resides in the PMST register.

FIGURE 4. Functional block diagram - Continued.

Internal hardware summary - Continued.

Unit	Symbol	Function
Interrupt flag register	IFR(16)	A 16-bit flag register used to latch the active-low interrupts. The IFR is a memory-mapped register.
Interrupt mask bit	INTM(1)	The interrupt mask bit globally masks or enables all interupts. This bit resides in ST0.
Interrupt number	INT#(4)	The number of the specific interrupt being sent to the CPU to be activated. This value comes from either the interrupt-processing circuitry or, in the case of the INTR instruction, the program bus.
Interrupt pointer	IPTR(5)	Five bits pointing to the 2K page where the interrupt vectors currently reside in the system. These bits reside in the PMST register.
Interrupt mask register	IMR(16)	A 16-bit memory-mapped register used to mask interrupts.
Microcall stack	MCS(15-0)	A single-word stack that temporarily stores the contents of the PFC while the PFC is being used to address data memory with the block move (BLDD/BLPD), multiply-accumulate (MAC/MACD), and table read/write (TBLR/TBLW) instructions.
Microprocessor	/$\overline{MP}$/MC	This bit resides in the PMST register and indicates whether the on-chip ROM microcomputer mode is mapped into program address space.
Multiplexer	MUX	A bus multiplexer used to select the source of operands for a bus or execution unit, depending on the nature of the current instruction.
Multiplier	MULTIPLIER	A 16 X 16-bit parallel multiplier.
Overflow flag	OV(1)	This bit resides in ST0 and indicates an overfow in an arithmetic operation in the ALU.
Overflow mode	OVM(1)	This bit resides in ST0 and determines whether an overflow in the ALU will wrap around or saturate.
Overlay to data space	OVLY(1)	This bit resides in the PMST register and determines whether the on-chip single-access memory will be addressable in data address space.
Parallel logic unit	PLU	A 16-bit logic unit that executes logic operations from either long immediate operands or the contents of the DBMR directly upon data locations without interfering with the contents of the CALU registers.
Prefetch counter	PFC(15-0)	A 16-bit counter used to prefetch program instructions. The PFC contains the address of the instruction currently being prefetched. It is updated when a new prefetch is initiated. The PFC can slo address program memory when the block move (BLPD), multiply-accumulate (MAC/MACD), and table read/write (TBLR/TBLW) instructions are used and can address data memory when the block move (BLDD) instruction is used.
Prescaler count register	COUNT(4)	A four-bit register that contains the value for the prescaling operation. When the register contents are used as prescaling data, this register is loaded from the dynaic shift count or from the instruction. In conjunction with the BIT and BITT instuctions, this register is loaded from the dynamic bit pointer or the instruction word.
Product register	PREG(32)	A 32-bit product register used to hold the multipliers product. The high and low words of the PREG can be accessed individually.
Program bus	PROG DATA	A 16-bit bus used to route instructions(and data for the MAC and MACD instructions).
Program counter	PC(16)	A 16-bit program counter used to address program memory sequentially. The PC always contains the address of the next instruction to be fetched. The PC contents are updated following each instruction decode operation.

FIGURE 4. Functional block diagram - Continued.

Internal hardware summary - Continued.

Unit	Symbol	Function
Program memory	PROGRAM	This block refers to program memory used with the core and defined in MEMORY specific device descriptions. It refers to both on- and off-chip memory blocks accessed in program memory space.
Program memory	PROG	A 16-bit bus that carries the program memory address. address bus ADDRESS
Prescaling shifter	PRESCALER	A 0- to 16-bit left barrel shifter used to prescale data coming into the ALU. Also used to align data for multprecision operations. This shifter is also used as a 0- to 16-bit right barrel shifter of the ACC.
Postscaling shifter	POSTSCALER	A 0- to 7-bit left barrel shifter used to postscale data coming out of the CALU.
Product shifter	P-SCALER	A 0-, 1-, or 4-bit left shifter that can remove extra sign bits (gained in the multiply operation) when fixed-point arithmetic is used; or a 6-bit right shifter that can scale the products down to avoid overflow in the accumulation process.
Product shifter mode	PM(2)	These two bits define the product shifter mode; They reside in ST1.
Repeat conter	RPTC(16)	A 16-bit counter used to control the repeated execution of a single instruction.
Sign extension mode	SXM(1)	This bit resides in ST1 and controls whether the arithmetic operation will be sign-extended or not.
Stack	STACK	An 8 X 16-bit hardware stack used to store the PC during interrupts and calls. The ACCL and data meory values may also be pushed onto and popped from the stack.
Status registers	ST0 ST1 PMST	Three 16-bit status registers that contain status and control bits.
Temporary multiplicand	TREG0(16)	A 16-bit register that temporarily holds an operand for the multiplier.
Temporary registers enable	TRM(1)	This bit defines whether an LT(A,D,P,S) instruction loads all three of the TREGs(0,1,2) to maintain compatibility with the device or loads just TREG0. This bit resides in the PMST register.
Test/control flag	TC(1)	This bit resides in ST1 and stores the results of ALU or PLU test bit operations.

FIGURE 4. Functional block diagram - Continued.

Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	HIGHZ
00000011	PRIVATE1
00100000	PRIVATE2
00100001	PRIVATE3
00100010	PRIVATE4
00100011	PRIVATE5
00100100	PRIVATE6
00100101	PRIVATE7
00100110	PRIVATE8
00100111	PRIVATE9
00101000	PRIVATE10
00101001	PRIVATE11

FIGURE 5. Boundary scan instruction codes..

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures. All input and output terminals shall be tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---	---
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)				

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614)692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Signal name	Signal description
ADDRESS AND DATA BUSES	
A0 - A15	Parallel address bus. Multiplexed to address external data, program memory, or I/O. A0 - A15 are in the high-impedance state in hold mode and when OFF is active (low). These signals are used as inputs for external DMA access of the on-chip single-access RAM. They become inputs while HOLDA is active (low) if BR is externally driven low.
D0 - D15	Parallel data bus. Multiplexed to transfer data between the core CPU and external data, program memory, or I/O devices. D0 - D15 are in the high-impedance state when not outputting data, when RS or HOLD is asserted, or when OFF is active (low). These signals are also used in external DMA access of the on-chip single-access RAM.
MEMORY CONTROL SIGNALS	
$\overline{DS}$, $\overline{PS}$, $\overline{IS}$	Data, program, and I/O space select signals. Always high unless asserted for communicating to a particular external space. DS, PS, and IS are in the high-impedance state in hold mode or when OFF is active (low).
READY	Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. READY also indicates a bus grant to an external device after a BR (bus request) signal.
R/$\overline{W}$	Read/Write. Indicates transfer direction during communication to an external device. Normally in read mode (high) unless asserted for performing a write operation. R/W is in the high-impedance state in hold mode or when OFF is active (low). Used in external DMA access of the 9K RAM cell. While HOLDA and IAQ are active (low), this signal is used to indicate the direction of the data bus for DMA reads (high) and writes (low).
$\overline{STRB}$	Strobe. Always high unless asserted to indicate an external bus cycle. STRB is in the high-impedance state in the hold mode or when OFF is active (low). Used in external DMA access of the on-chip single-access RAM. While HOLDA and IAQ are active (low), this signal is used to select the memory access.
$\overline{RD}$	Read select. Indicates an active external read cycle and can connect directly to the output enable (OE) of external devices. This signal is active on all external program, data, and I/O reads. RD is in the high-impedance state in hold mode or when OFF is active (low).

Signal name	Signal description
$\overline{WE}$	Write enable. The falling edge indicates that the device is driving the external data bus (D15 - D0). Data can be latched by an external device on the rising edge of WE. This signal is active on all external program, data, and I/O writes. WE is in the high-impedance state in hold mode or when OFF is active (low).
MULTIPROCESSING SIGNALS	
$\overline{HOLD}$	Hold. Asserted to request control of the address, data, and control lines. When acknowledged by the device, these lines go to the high-impedance state.
$\overline{HOLDA}$	Hold acknowledge. Indicates to the external circuitry that the processor is in a hold state and that the address, data, and memory control lines are in the high-impedance state so that they are available to the external circuitry for access of local memory. This signal also goes to the high-impedance state when OFF is active (low).
$\overline{BR}$	Bus request. Asserted during access of external global data memory space. READY is asserted when the global data memory is available for the bus transaction. BR can be used to extend the data memory address space by up to 32K words. BR goes to the high-impedance state when OFF is active low. BR is used in external DMA access of the on-chip single-access RAM. While HOLDA is active (low), BR is externally driven (low) to request access to the on-chip single-access RAM.
$\overline{IAQ}$	Instruction acquisition. Asserted (active) when there is an instruction address on the address bus; goes into the high-impedance state when OFF is active (low). IAQ is also used in external DMA access of the on-chip single-access RAM. While HOLDA is active (low), IAQ acknowledges the BR request for access of the on-chip single-access RAM and stops indicating instruction acquisition.
$\overline{BIO}$	Branch control. Samples as the BIO condition. If low, the device executes the conditional instruction. BIO must be active during the fetch of the conditional instruction.
XF	External flag (latched software-programmable signal). Set high or low by a specific instruction or by loading status register 1 (ST1). Used for signaling other processors in multiprocessor configurations or as a general-purpose output. XF goes to the high-impedance state when OFF is active (low) and is set high at reset.
$\overline{IACK}$	Interrupt acknowledge. Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15 - A0. IACK goes to the high-impedance state when OFF is active (low).
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS	
$\overline{INT1}$-$\overline{INT4}$	External interrupts. Prioritized and maskable by the interrupt mask register (IMR) and interrupt mode bit (INTM, bit 9 of status register 0). These signals can be polled and reset via the interrupt flag register.
$\overline{NMI}$	Nonmaskable interrupt. External interrupt that cannot be masked via INTM or IMR. When NMI is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	Reset. Causes the device to terminate execution and forces the program counter to zero. When RS is brought to a high level, execution begins at location zero of program memory.
MP/$\overline{MC}$	Microprocessor/microcomputer select. If active (low) at reset (microcomputer mode), the signal causes the internal program ROM to be mapped into program memory space. In the microprocessor mode, all program memory is mapped externally. This signal is sampled only during reset, and the mode that is set at reset can be overridden via the software control bit MP/MC in the PMST register.
OSCILLATOR/TIMER SIGNALS	
CLKOUT1	Master clock (or CLKIN2 frequency). CLKOUT1 cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. This signal goes to the high-impedance state when OFF is active (low).

Signal name	Signal description

CLKMD1, CLKMD2

CLKMD1	CLKMD2	Clock mode
0	0	External clock with divide-by-two option. Input clock provided to X2/CLKIN1 pin. Internal oscillator and PLL disabled.
0	1	Reserved for test purposes.
1	0	External divide-by-one option. Input clock provided to CLKIN2. Internal oscillator is disabled and internal PLL is enabled.
1	1	Internal or external divide-by-two option. Input clock provided to X2/CLKIN1. Internal oscillator is enabled and internal PLL is disabled.

X2/CLKIN	Input to the internal oscillator from the crystal. If the internal oscillator is not being used, a clock may be input to the device on X2/CLKIN. The internal machine cycle is half this clock rate.
X1	Output from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. This signal does not go to the high-impedance state when OFF is active (low).
CLKIN2	Divide-by-one input clock for driving the internal machine rate.
TOUT	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide.

SUPPLY PINS

VDD1 - VDD4	Power supply for data bus
VDD5 - VDD6	Power supply for address bus
VDD7 - VDD8	Power supply for inputs and internal logic
VDD9 - VDD10	Power supply for address bus
VDD11 - VDD12	Power supply for memory control signals
VDD13 - VDD14	Power supply for inputs and internal logic
VDD15 - VDD16	Power supply for memory control signals
VSS1 - VSS2	Ground for memory control signals
VSS3 - VSS6	Ground for data bus
VSS7 - VSS10	Ground for address bus
VSS11 - VSS12	Ground for memory control signals
VSS13 - VSS16	Ground for inputs and internal logic

SERIAL PORT SIGNALS

CLKR, TCLKR	Receive clock. External clock signal for clocking data from DR (data receive) or TDR (TDM data receive) into the RSR (serial port receive shift register). Must be present during serial port transfers. If the serial port is not being used, these signals can be sampled as an input via the IN0 bit of the serial port control (SPC) or TDR serial port control (TSPC) registers.
CLKX, TCLKX	Transmit clock. Clock signal for clocking data from the DR or TDR to the DX (data transmit) or TDX (TDM data transmit pins). CLKX can be an input if the MCM bit in the serial port control register is set to 0. It can also be driven by the device at 1/4 the CLKOUT1 frequency when the MCM bit is set to 1. If the serial port is not being used, this pin can be sampled as an input via the IN1 bit of the SPC or TSPC register. This signal goes into the high-impedance state when OFF is active (low).
DR, TDR	Serial data receive. Serial data is received in the RSR (serial port receive shift register) via DR or TDR.

Signal name	Signal description
DX, TDX	Serial port transmit. Serial data transmitted from XSR (serial port transmit shift register) via DX or TDX. This signal is in the high-impedance state when not transmitting and when OFF is active (low).
FSR, TFSR/TADD	Frame synchronization pulse for receive. The falling edge of FSR or TFSR initiates the data receive process, which begins the clocking of the RSR. TFSR becomes an input/output (TADD) pin when the serial port is operating in the TDM mode (TDM bit = 1). In TDM mode, this pin is used to input/output the address of the port. This signal goes into the high-impedance state when OFF is active (low).
FSX, TFSX/TFRM	Frame synchronization pulse for transmit. The falling edge of FSX/TFSX initiates the data transmit process, which begins the clocking of the XSR. Following reset, the default operating condition of FSX/TFSX is an input. This pin may be selected by software to be an output when the TXM bit in the serial control register is set to 1. This signal goes to the high-impedance state when OFF is active (low). When operating in TDM mode (TDM bit = 1), TFSX becomes TFRM, the TDM frame synchronization pulse.
TEST SIGNALS	
TCK	JTAG test clock. This is normally a free-running clock with a 50% duty cycle. The changes of TAP (test access port) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	JTAG test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	JTAG test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. This signal also goes to the high-impedance state when OFF is active (low).
TMS	JTAG test mode select. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{\text{TRST}}$	JTAG test reset. Asserting this signal gives the JTAG scan system control of the operations of the device. If this signal is not connected or is driven low, the device operates in its functional mode and the JTAG signals are ignored.
EMU0	Emulator pin 0. When TRST is driven low, EMU0 must be high for activation of the OFF condition (see EMU1/OFF). When TRST is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output put via JTAG scan.
EMU1/$\overline{\text{OFF}}$	Emulator 1/OFF. When TRST is driven high, EMU1/OFF is used as an interrupt to or from the emulator system and is defined as input/output via JTAG scan. When TRST is driven low, EMU1/OFF is configured as OFF. When the OFF signal is active (low), all output drivers are in the high-impedance state. OFF is used exclusively for testing and emulation purposes (not for multiprocessing applications). For the OFF condition, the following conditions apply: ° TRST = Low ° EMU0 = High ° EMU1/OFF = Low
RESERVED	Reserved (Case Y only). This pin should be left unconnected.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

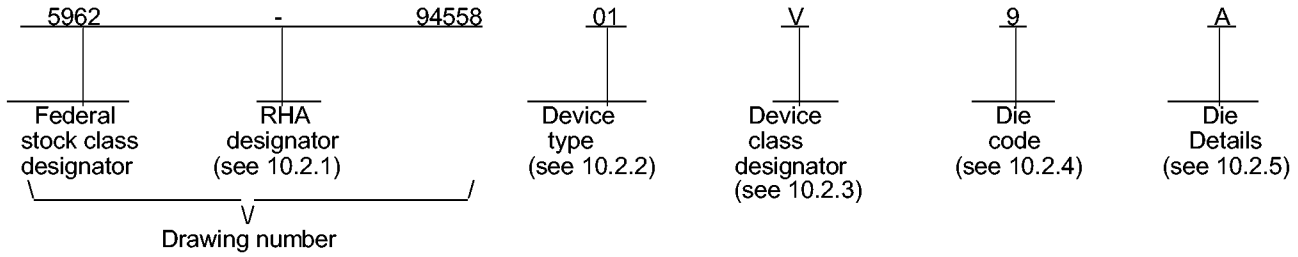
6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

Appendix A

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	320C50A	Digital signal processor, 40 MHz
02 1/	320C50A	Digital signal processor, 50 MHz
03	320C50	Digital signal processor, 50 MHz
04	320C50	Digital signal processor, 66 MHz
05	320C50	Digital signal processor, 40 MHz

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Die type	Figure number
03 - 05	A-1

10.2.5.2. Die bonding pad locations and electrical functions.

Die type	Figure number
03 - 05	A-1

1/ Device type 01 and 02 are not available as QML die only.

10.2.5.3. Interface materials.

Die type	Figure number
03 - 05	A-1

10.2.5.4. Assembly related information.

Die type	Figure number
03 - 05	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.5.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figures A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

6.0 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

Appendix A

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 408.7 mm x 384.9mm.
Die thickness: 15 mm.

Interface materials.
Top metallization: TiW 2kA / AlSiCu 56kA
Backside metallization: Polysilicon

Glassivation.
Type: Ox / Cu
Thickness: 3 kA / 9 kA

Substrate: Polysilicon

Assembly related information.
Substrate potential: Ground
Special assembly instructions: None

Appendix A

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
1	5347.4	9670.8	$\overline{IAQ}$	41	106.3	1783.3	CLK
2	5161.8	9670.8	TRST	42	106.3	1353.6	V_{DD5}
3	4908.6	9670.8	V_{SS1}	43	106.3	4417.7	V_{DD6}
4	4773.6	9670.8	V_{SS2}	44	1513.4	106.3	V_{SS7}
5	4573.4	9670.8	MP/MC	45	1648.4	106.3	V_{SS8}
6	4139.3	9670.8	D15	46	2128.3	106.3	A0
7	3851.3	9670.8	D14	47	2403.3	106.3	A1
8	3515.3	9670.8	D13	48	2637.3	106.3	A2
9	3273.3	9670.8	D12	49	2912.2	106.3	A3
10	3024.8	9670.8	D11	50	3132.7	106.3	A4
11	2777.3	9670.8	D10	51	3407.7	106.3	A5
12	2421.0	9670.8	D9	52	3628.2	106.3	A6
13	2121.1	9670.8	D8	53	3903.1	106.3	A7
14	1702.6	9670.8	V_{DD1}	54	4123.6	106.3	A8
15	1567.6	9670.8	V_{DD2}	55	4398.6	106.3	A9
16	106.3	8552.8	V_{SS3}	56	4569.6	106.3	V_{DD7}
17	106.3	8417.8	V_{SS4}	57	4704.6	106.3	V_{DD8}
18	106.3	7859.8	D7	58	4896.7	106.3	TDI
19	106.3	7616.8	D6	59	5319.6	106.3	V_{SS9}
20	106.3	7321.3	D5	60	5454.8	106.3	V_{SS10}
21	106.3	7096.3	D4	61	5646.0	106.3	CLKMD1
22	106.3	6871.3	D3	62	5886.6	106.3	A10
23	106.3	6646.3	D2	63	6161.6	106.3	A11
24	106.3	6323.9	D1	64	6527.3	106.3	A12
25	106.3	6098.9	D0	65	6802.3	106.3	A13
26	106.3	5818.7	TMS	66	7036.3	106.3	A14
27	106.3	5498.0	V_{DD3}	67	7311.2	106.3	A15
28	106.3	5363.0	V_{DD4}	68	8202.2	106.3	V_{DD9}
29	106.3	4942.2	TCK	69	8337.2	106.3	V_{DD10}
30	106.3	4764.3	NC	70	8649.0	106.3	$\overline{RD}$
31	106.3	4601.2	V_{SS5}	71	9195.5	106.3	WE
32	106.3	4466.2	V_{SS6}	72	10274.3	1253.8	V_{SS11}
33	106.3	4041.0	$\overline{INT1}$	73	10274.3	1388.8	V_{SS12}
34	106.3	3789.2	$\overline{INT2}$	74	10274.3	1902.0	$\overline{DS}$
35	106.3	3537.4	$\overline{INT3}$	75	10274.3	2236.6	$\overline{IS}$
36	106.3	3201.4	$\overline{INT4}$	76	10274.3	2524.8	$\overline{PS}$
37	106.3	2949.6	NMI	77	10274.3	2882.6	$\overline{R/W}$
38	106.3	2697.8	DR	78	10274.3	3168.8	$\overline{STRB}$
39	106.3	2445.9	TDR	79	10274.3	3365.0	BR
40	106.3	2035.1	FSR	80	10274.3	3625.7	NC

Figure A-1

Appendix A

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
81	10274.3	3795.5	CLKIN2
82	10274.3	3950.6	X2/CLKIN
83	10274.3	4126.6	X1
84	10274.3	4296.2	NC
85	10274.3	4459.4	V_{DD11}
86	10274.3	4594.4	V_{DD12}
87	10274.3	4766.7	TDO
88	10274.3	5085.1	V_{SS13}
89	10274.3	5220.1	V_{SS14}
90	10274.3	5375.3	CLKMD2
91	10274.3	5579.4	FSX
92	10274.3	5866.1	TFSX/TFRM
93	10274.3	6086.8	DX
94	10274.3	6379.1	TDX
95	10274.3	6599.8	HOLDA
96	10274.3	6820.5	XF
97	10274.3	7180.3	CLKOUT1
98	10274.3	7558.5	IACK
99	10274.3	8089.5	V_{DD13}
100	10274.3	8224.5	V_{DD14}
101	10274.3	8724.3	NC
102	10274.3	8859.3	NC
103	9201.4	9670.8	EMU0
104	8796.6	9670.8	EMU1/OFF
105	8540.1	9670.8	V_{SS15}
106	8405.1	9670.8	V_{SS16}
107	7927.9	9670.8	TOUT
108	7690.0	9670.8	TCLKX
109	7456.5	9670.8	CLKX
110	7133.8	9670.8	TFSR/TADD
111	6956.1	9670.8	TCLKR
112	6771.8	9670.8	RS
113	6587.5	9670.8	READY
114	6403.1	9670.8	HOLD
115	6016.9	9670.8	BIO
116	5780.7	9670.8	V_{DD15}
117	5645.7	9670.8	V_{DD16}

Figure A-1

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-03-06

Approved sources of supply for SMD 5962-94558 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9455801QXA	3/	SMJ320C50AGFAM40
5962-9455801QYA	3/	SMJ320C50AHFGM40
5962-9455802QXA	3/	SMJ320C50AGFAM50
5962-9455802QYA	3/	SMJ320C50AHFGM50
5962-9455803QXA	01295	SMJ320C50GFAM50
5962-9455803QYA	01295	SMJ320C50GFGM50
5962-9455803Q9A	01295	SMJ320C50KGDM50B
5962-9455804QXA	01295	SMJ320C50GFAM66
5962-9455804QYA	01295	SMJ320C50HFGM66
5962-9455804NZD	01295	SMJ320C50PQM66
5962-9455804Q9A	01295	SMJ320C50KGDM66B
5962-9455805Q9A	01295	SMJ320C50KGDM40B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448