REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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CHECKED BY Charles Reusing

APPROVED BY William K. Heckman

DRAWING APPROVAL DATE 22 AUGUST 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
CASCADABLE 64 X 8 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89664

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1351

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89664	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Shift rate
01	See 6.6	64 X 8 FIFO	15 MHz
02	See 6.6	64 X 8 FIFO	25 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	See figure 1, (28-lead, 1.490" x .310" x .200"), dual-in-line package
Y	F-11 (28-lead, .740" x .380" x .090"), flat package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to +7.0 V dc
DC Input voltage	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Y and 3	See MIL-M-38510, appendix C
Case X	26°C/W 1/
Junction temperature (T_J) 2/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
2/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life tests.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard and bulletin. Unless otherwise specified, the following specification, standard, and bulletin, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (reference MIL-M-38510, 3.1.3.8) shall be subjected to and pass the Internal Water-Vapor Content (reference test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical test for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.4	V
Input high voltage	V_{IH} 2/		1, 2, 3	All	2.2		V
Input low voltage	V_{IL} 2/		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
DC supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 0 V and 3 V, f = 0	1, 2, 3	All		125	mA
Operating supply current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 0 V and 3 V	1, 2, 3	All		3/	
Input capacitance	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d	7, 8	All			
Operating frequency	f_O 4/		9, 10, 11	01		15	MHz
				02		25	
SI high time	t_{PHSI} 4/	See figure 5	9, 10, 11	01	23		ns
				02	11		
SI low time	t_{PLSI} 4/		9, 10, 11	01	25		ns
				02	24		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data setup to SI	t_{SSI} 5/	See figure 5	9, 10, 11	All	0		ns
Data hold from SI	t_{HSI} 5/		9, 10, 11	01	30		ns
				02	20		
Delay, SI high to IR low	t_{DLIR}		9, 10, 11	01		35	ns
				02		21	
Delay, SI low to IR high	t_{DHIR}		9, 10, 11	01		40	ns
				02		23	
SO high time	t_{PHSO} 4/		9, 10, 11	01	23		ns
				02	11		
SO low time	t_{PLSO} 4/		9, 10, 11	01	25		ns
				02	24		
Delay, SO high to OR low	t_{DLOR}		9, 10, 11	01		35	ns
				02		21	
Delay, SO low to OR high	t_{DHOR}		9, 10, 11	01		40	ns
				02		23	
Data Setup to OR high	t_{SOR}		9, 10, 11	All	0		ns
Data hold from SO low	t_{HSO}		9, 10, 11	All	0		ns
Fallthrough, bubbleback time	t_{BT}		9, 10, 11	01	10	65	ns
				02	10	60	
Data setup to IR	t_{SIR} 6/		9, 10, 11	All	5		ns
Data hold from IR	t_{HIR} 6/		9, 10, 11	01	30		ns
				02	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input ready pulse high	t_{PIR} 7/	See figure 5	9, 10, 11	All	6		ns
Output ready pulse high	t_{POR} 8/		9, 10, 11	All	6		ns
$\overline{OE}$ low to low Z	t_{DLZOE} 9/ 10/		9, 10, 11	01		35	ns
				02		30	
$\overline{OE}$ high to high Z	t_{DHZOE} 9/ 10/		9, 10, 11	01		35	ns
				02		30	
SI low to HF high	t_{DHHF}		9, 10, 11	01		65	ns
				02		55	
SO low to HF low	t_{DLHF}		9, 10, 11	01		65	ns
				02		55	
SO or SI low to AFE low	t_{DLAFE}		9, 10, 11	01		65	ns
				02		55	
SO or SI low to AFE high	t_{DHAFE}		9, 10, 11	01		65	ns
				02		55	
$\overline{MR}$ pulse width	t_{PMR}		9, 10, 11	01	55		ns
				02	45		
$\overline{MR}$ high to SI high	t_{DSI}		9, 10, 11	01	25		ns
				02	10		
$\overline{MR}$ low to OR low	t_{DOR}		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to IR high	t_{DIR}		9, 10, 11	01		55	ns
				02		45	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
$\overline{MR}$ low to output low	t_{LZMR} 11/	See figure 5	9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to AFE high	t_{AFE}		9, 10, 11	01		55	ns
				02		45	
$\overline{MR}$ low to HF low	t_{HF}		9, 10, 11	01		55	ns
				02		45	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4, circuit A.
2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3/ Subgroups 1, 2, and 3 tests for I_{CC2} shall be tested to the calculated limit for initial test and after any design or process changes which may affect this parameter. To calculate I_{CC2} at any given operating frequency, use $I_{CC1} + (1\ mA/mHz) \times (1/f_{osi} + 1/f_{oso})/2$.
4/ $1/f_O \ge (t_{PHSI} + t_{PLSI})$, $1/f_O \ge (t_{PHSO} + t_{PLSO})$.
5/ The parameters t_{SSI} and t_{HSI} apply when memory is not full.
6/ The parameters t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubblethrough (t_{BT}) conditions exist.
7/ At any given operating condition $t_{PIR} \ge (t_{PHSO}$ required).
8/ At any given operating condition $t_{POR} \ge (t_{PHSI}$ required).
9/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
10/ The parameter t_{DHZOE} transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the load in figure 4, circuit B. The parameter t_{DLZOE} is measured ±100 mV from steady-state voltage with the load in figure 4, circuit B.
11/ All data outputs will be at low level after reset goes high until data is entered into the FIFO.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

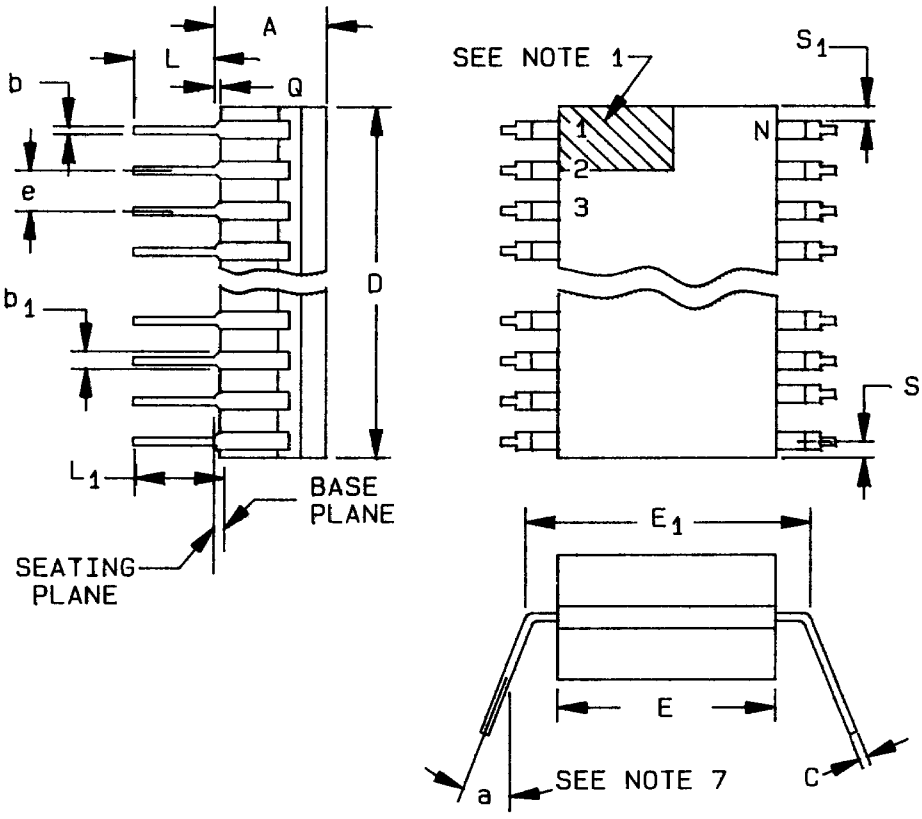

FIGURE 1. Case X (28-pin, 1.490" x .310" x .200"), dual-in-line package.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89664
		REVISION LEVEL	SHEET 8

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Dimensions					
	Inches		Millimeters		
Symbol	Min	Max	Min	Max	Notes
A	---	.200	---	5.08	
b	.014	.023	0.36	0.58	8
b_1	.038	.065	0.97	1.65	2, 8
c	.008	.015	0.20	0.38	8
D	---	1.490	---	37.85	4
E	.220	.310	5.59	7.87	4
E_1	.290	.320	7.37	8.13	7

Dimensions					
	Inches		Millimeters		
Symbol	Min	Max	Min	Max	Notes
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L_1	.150	---	3.81	---	
Q	.015	.060	0.38	1.52	3
S	---	.100	---	2.54	6
S_1	.005	---	0.13	---	6
α	0°	15°	0°	15°	

NOTES:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .023 (0.58 mm) for leads number 1, 14, 15, and 28 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all four corners (leads number 1, 14, 15, and 28) shall apply.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
8. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
9. Twenty-six spaces.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 1. Case X (28-pin, 1.490" x .310" x .200"), dual-in-line package - Continued.

Device types	All
Case outlines	X, Y, and 3
Terminal number	Terminal symbol
1	AFE
2	HF
3	IR
4	SI
5	DI_0
6	DI_1
7	GND
8	DI_2
9	DI_3
10	DI_4
11	DI_5
12	DI_6
13	DI_7
14	NC
15	$\overline{OE}$
16	DO_7
17	DO_6
18	DO_5
19	DO_4
20	DO_3
21	DO_2
22	GND
23	DO_1
24	DO_0
25	OR
26	SO
27	$\overline{MR}$
28	V_{CC}

FIGURE 2. Terminal connections.

Mode	Input control				Output control	
	SI	SO	$\overline{MR}$	$\overline{OE}$	IR	OR
Read	X	See note 1	H	L	X	H
Write	See note 2	X	H	X	H	X
Reset	X	X	L	X	X	X
Disable	X	X	X	H	X	X

NOTES:
1. High to low transition.
2. Low to high transition.

FIGURE 3. Truth table.

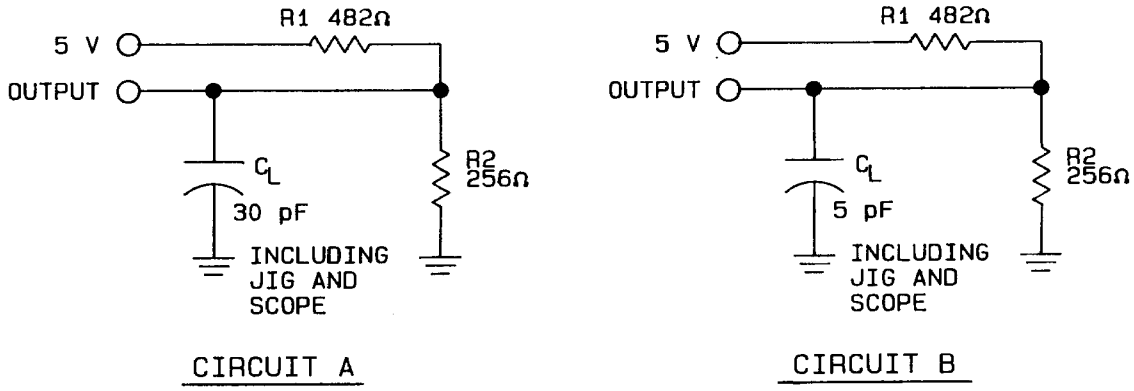
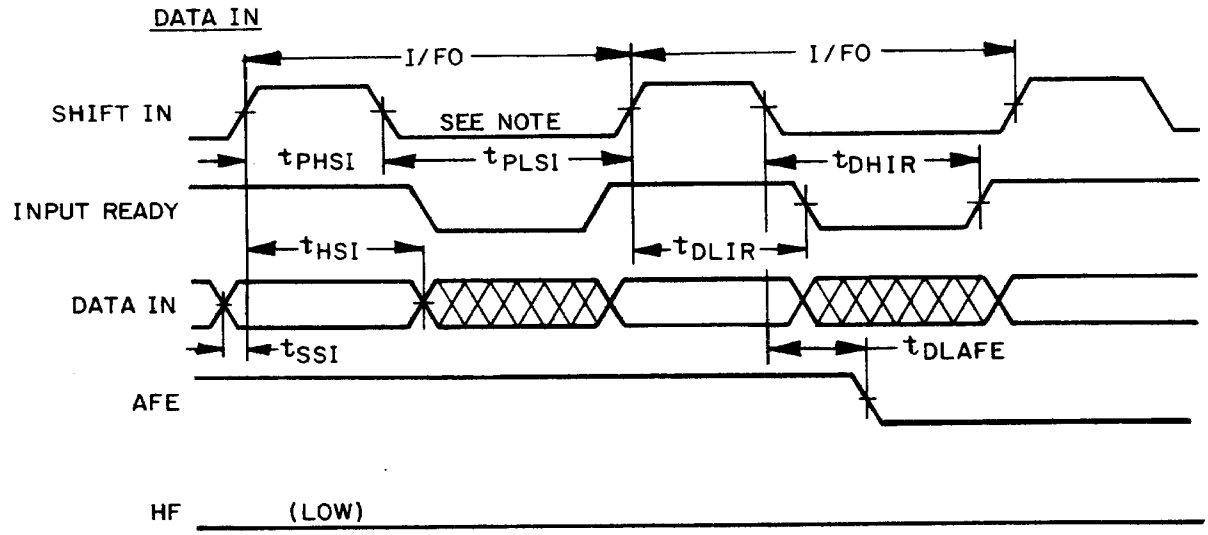
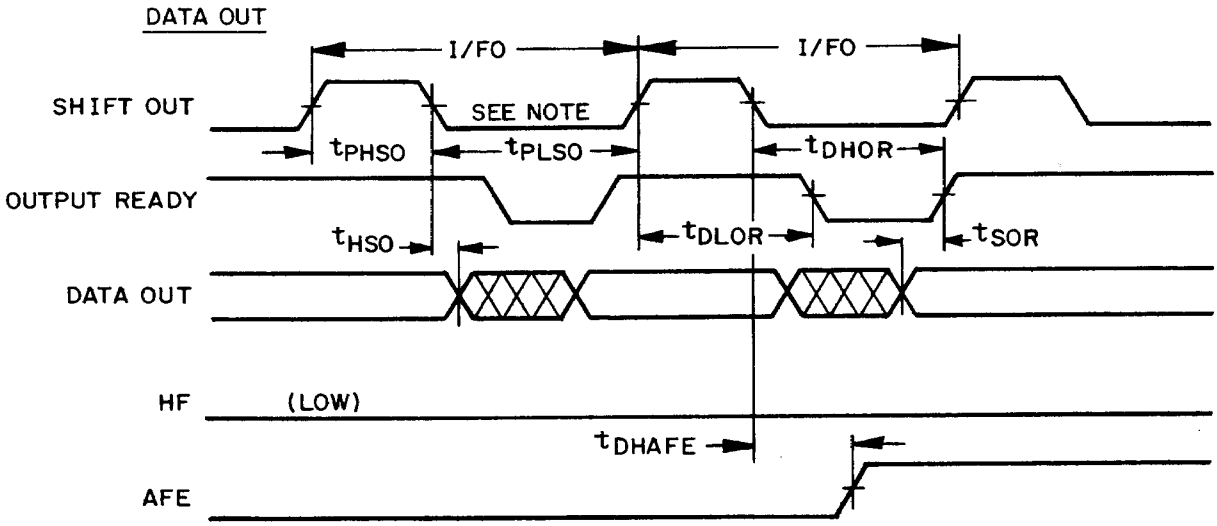


FIGURE 4. Output load circuit.



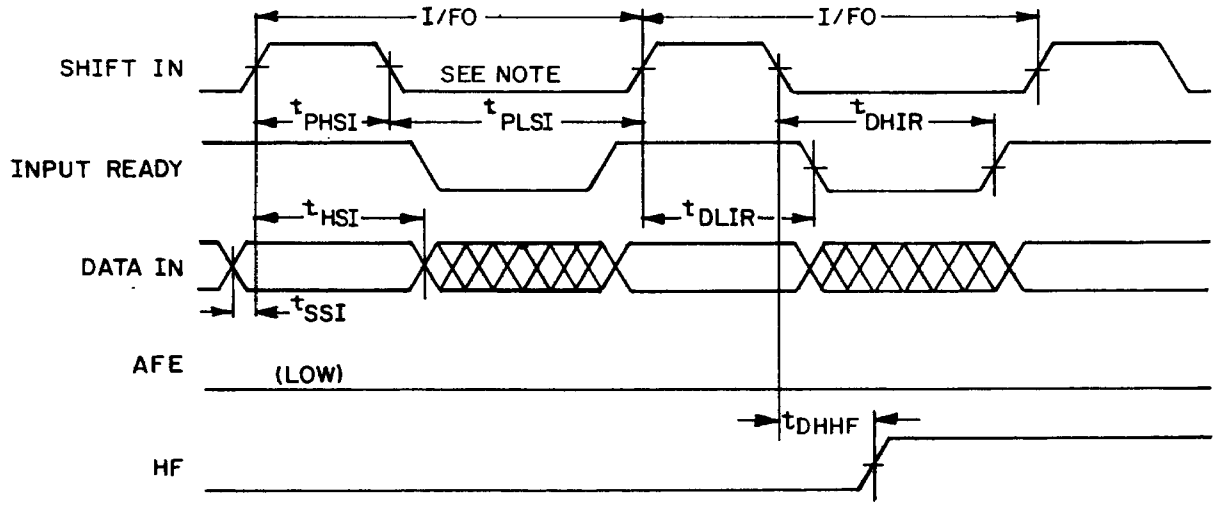
NOTE: FIFO contains 8 words.



NOTE: FIFO contains 9 words.

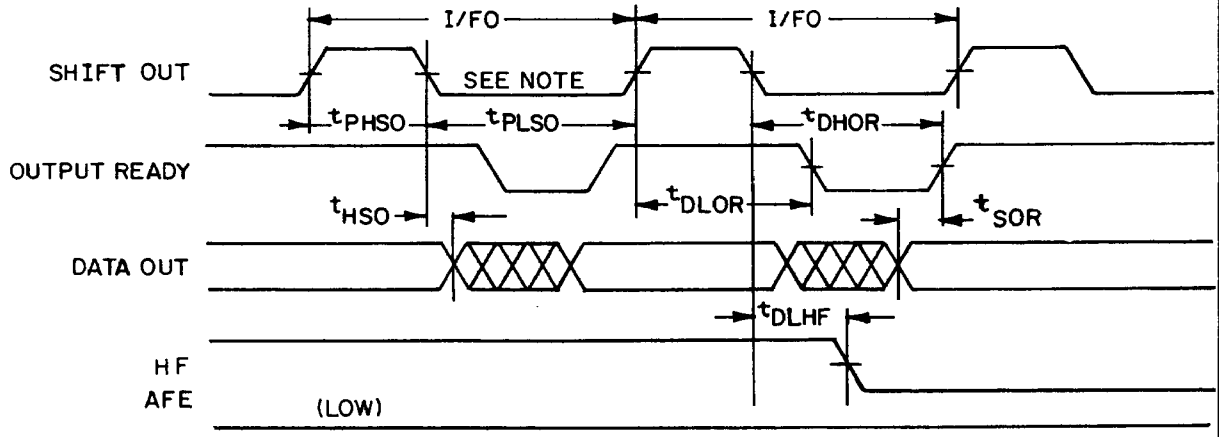
FIGURE 5. Timing waveforms.

DATA IN



NOTE: FIFO contains 31 words.

DATA OUT



NOTE: FIFO contains 32 words.

OUTPUT ENABLE

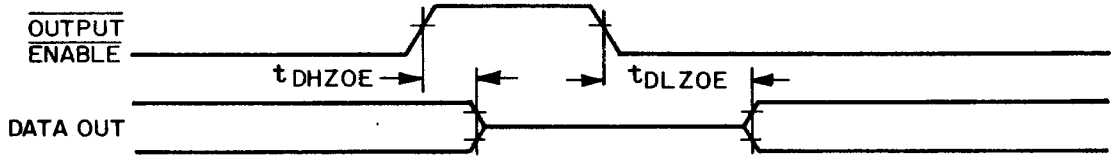
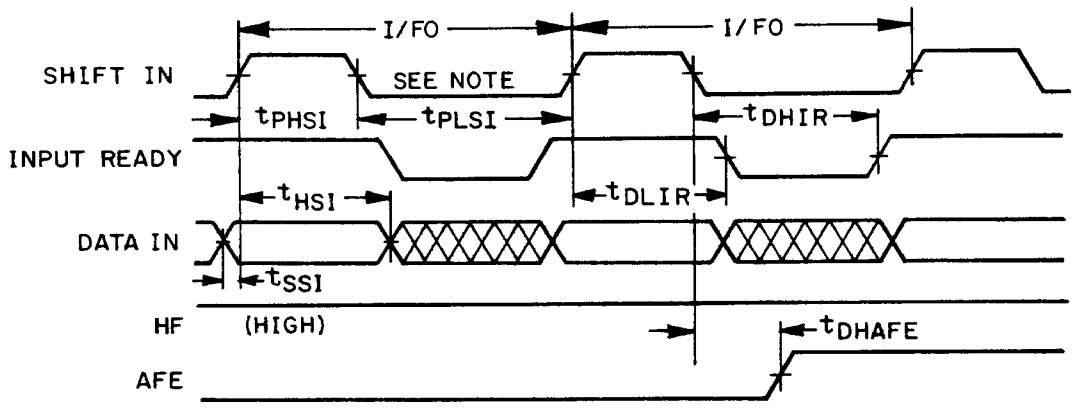


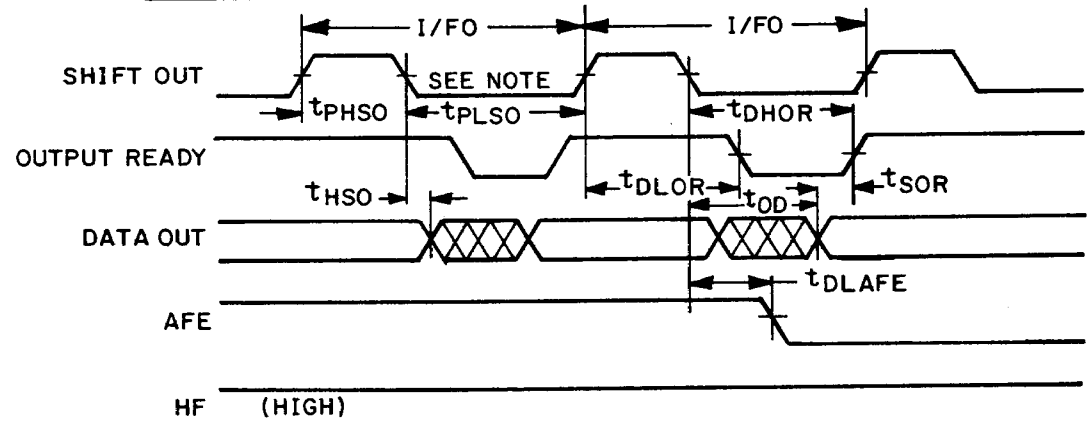
FIGURE 5. Timing waveforms - Continued.

DATA IN



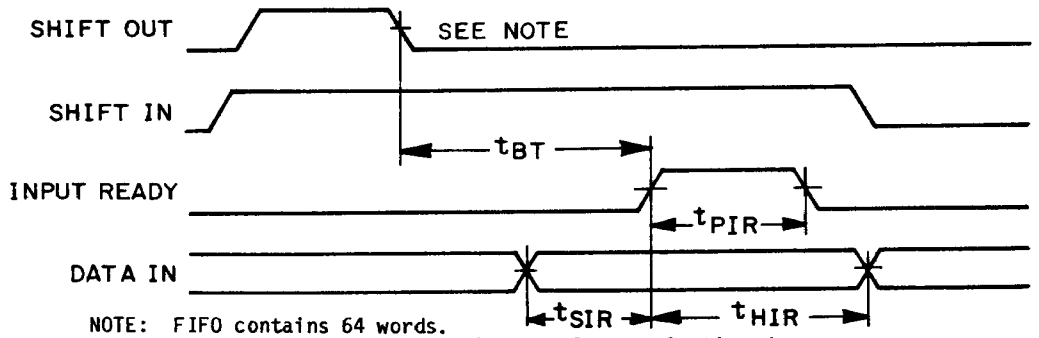
NOTE: FIFO contains 55 words.

DATA OUT



NOTE: FIFO contains 56 words.

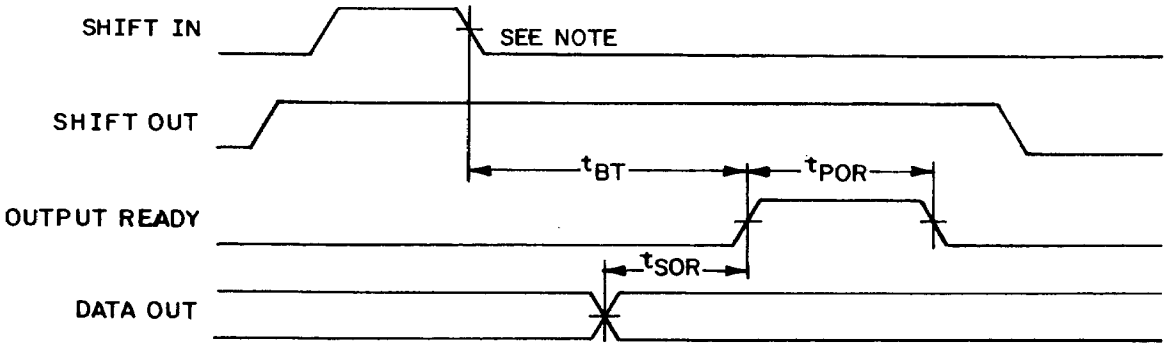
BUBBLEBACK, DATA OUT TO DATA IN



NOTE: FIFO contains 64 words.

FIGURE 5. Timing waveforms - Continued.

FALLTHROUGH, DATA IN TO DATA OUT



NOTE: FIFO is empty.

MASTER RESET

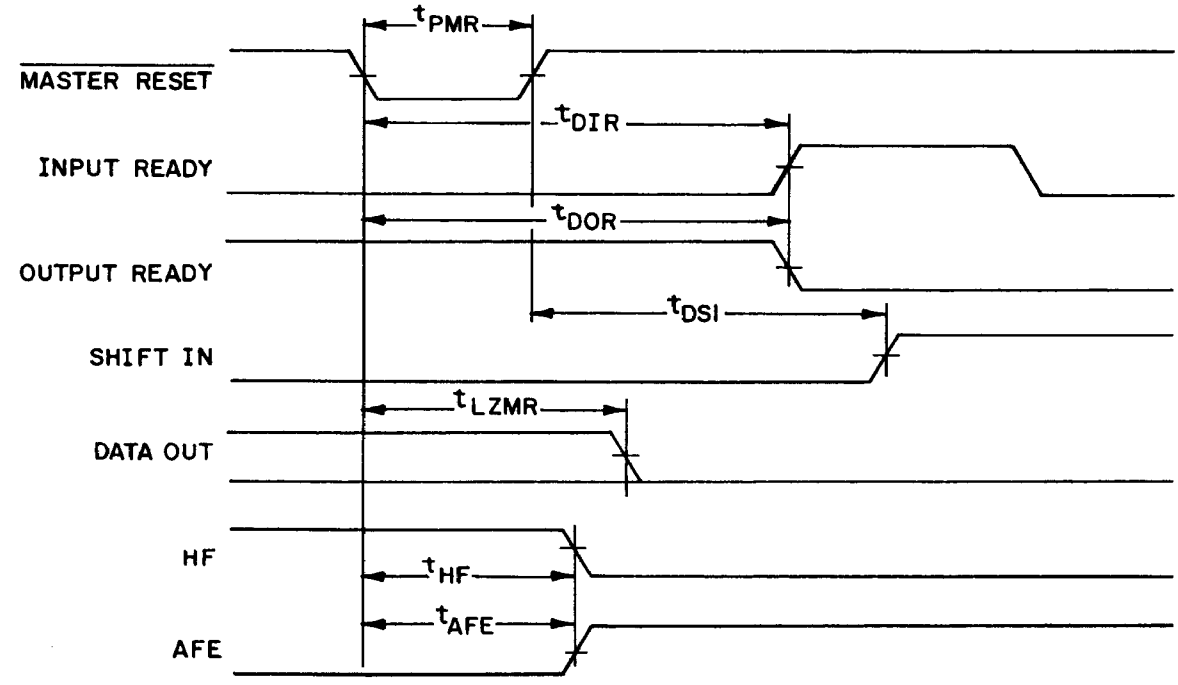


FIGURE 5. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after any design or process changes which may affect input or output capacitance. Sample size is 15 devices with no failures and all input and ouput terminals tested.

d. Subgroup 7 and 8 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-833 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroups 1 and 7.
** For subgroup 4, see 4.3.1c.
*** For subgroups 7 and 8, see 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8966401XX	65786	CY7C408A-15DMB	
5962-8966401YX	65786	CY7C408A-15KMB	
5962-89664013X	65786	CY7C408A-15LMB	
5962-8966402XX	65786	CY7C408A-25DMB	
5962-8966402YX	65786	CY7C408A-25KMB	
5962-89664023X	65786	CY7C408A-25LMB	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134