REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make changes to table I, table II, paragraphs 4.2a, 4.3.1b, and 4.3.2b. Change the case operating temperature to 110°C maximum.	1988 MAY 4	M. A. Frye

REV		A	A	A																					
PAGE	24	25	26	27																					
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A												
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
13 August 1987

AMSC N/A

PREPARED BY: Rick C. Officer

CHECKED BY: D. A. DiCenzo

APPROVED BY: M. A. Frye

SIZE: A

CODE IDENT. NO.: 67268

REV: A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, NMOS, 64K X 4 DRAM, MONOLITHIC SILICON

DWG NO. 5962-87676

PAGE 1 OF 27

5962-E872

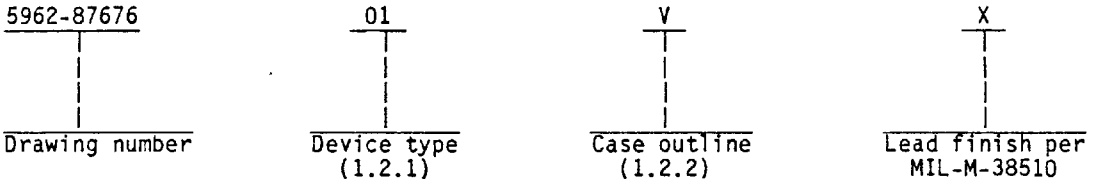
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Refresh
01	MT4067-12	64K x 4 bit DRAM	120 ns	256 cycles (4 ms)
02	MT4067-15	64K x 4 bit DRAM	150 ns	256 cycles (4 ms)
03	MT4067-20	64K x 4 bit DRAM	200 ns	256 cycles (4 ms)
04	MT4067-10	64K x 4 bit DRAM	100 ns	256 cycles (4 ms)

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package
X	See figure 1 (18-terminal, .505" x .305" x .100"), rectangular chip carrier package

1.3 Absolute maximum ratings.

Voltage on any pin relative to V_{SS}	-1.5 V to +7.0 V
Short-circuit output current	50 mA
Power dissipation (P_D)	1.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance (θ_{JC}):	
Case V	(See MIL-M-38510, appendix C)
Case X	50°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Power supply and signal reference (V_{SS})	0.0 V dc
High level input voltage (V_{IH})	2.4 V dc to 6.5 V dc
Low level input voltage (V_{IL})	-1.0 V dc to +0.8 V dc
Case operating temperature (T_C)	-55°C to +110°C
Refresh cycle time	4.0 ms

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2. APPLICABLE DOCUMENTS

2.1. Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +110°C$	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage 5/	V_{OH}	V_{IL} = 0.8 V, I_{OH} = -5 mA, V_{IH} = 2.4 V	All	1,2,3	2.4		V
Low level output voltage 5/	V_{OL}	V_{IL} = 0.8 V, I_{OL} = 5 mA, V_{IH} = 2.4 V	All	1,2,3		0.4	V
High level input leakage current	I_{IH}	V_{CC} = 5.5 V, V_I = 6.5 V	All	1,2,3		10	µA
Low level input leakage current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.0 V	All	1,2,3		-10	µA
High level output leakage current	I_{OH}	V_{CC} = 5.5 V, V_O = 6.5 V	All	1,2,3		10	µA
Low level output leakage current	I_{OL}	V_{CC} = 5.5 V, V_O = 0.0 V	All	1,2,3		-10	µA
Average operating 6/ current during READ or WRITE cycle	I_{CC1}	T_C = minimum cycle	All	1,2,3		55	mA
Standby current	I_{CC3}	after 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high	All	1,2,3		8	mA
Average refresh current 6/ ($\overline{RAS}$ only REFRESH)	I_{CC4}	T_C = minimim cycle, $\overline{CAS}$ high, $\overline{RAS}$ cycling	All	1,2,3		45	mA
Average page-mode current 6/	I_{CC2}	$T_C(P)$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling	All	1,2,3		55	mA
Standby current ($\overline{CAS}$ before $\overline{RAS}$ refresh) 7/	I_{CC5}	T_C = minimum cycle, $\overline{RAS}$ and $\overline{CAS}$ cycling	All	1,2,3		55	mA
Input capacitance A_0 - A_7, D_{IN} 7/	C_{I1}	T_C = +25°C See 4.3.1c	All	4		5	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ 7/	C_{I2}	T_C = +25°C See 4.3.1c	All	4		8	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +110°C$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Output capacitance D_{OUT} 7/	C_O	$T_C = +25°C$ See 4.3.1c	All	4		7	pF
Access time from $\overline{RAS}$ 8/	$t_{a(R)}$	See figures 4 and 5	01	9,10,11		120	ns
			02			150	ns
			03			200	ns
			04			100	ns
Access time from $\overline{CAS}$ 9/	$t_{a(C)}$		01	9,10,11		60	ns
			02			75	ns
			03			100	ns
			04			50	ns
Output disable time after $\overline{CAS}$ high 10/	$t_{dis(CH)}$		All	9,10,11		40	ns
Page-mode cycle time 11/	$t_{c(P)}$		01	9,10,11	100		ns
			02		120		ns
			03		225		ns
			04		90		ns
Read cycle time	$t_{c(rd)}$		01	9,10,11	220		ns
			02		250		ns
			03		330		ns
			04		195		ns
Write cycle time	$t_{c(W)}$		01	9,10,11	220		ns
			02		250		ns
			03		330		ns
			04		195		ns
Read-write/read-modify-write cycle time 11/	$t_{c(rdW)}$		01	9,10,11	290		ns
			02		315		ns
			03		410		ns
			04		250		ns
Pulse duration, $\overline{CAS}$ high (page mode)	$t_{w(CH)P}$		01,04	9,10,11	30		ns
			02		35		ns
			03		40		
Pulse duration, $\overline{CAS}$ low	$t_{w(CL)}$		01	9,10,11	60	10000	ns
			02		75	10000	ns
			03		100	10000	ns
			04		50	10000	ns
Pulse duration, $\overline{RAS}$ high (precharge time) (page mode) 12/	$t_{w(RH)P}$		01	9,10,11	90		ns
			02		90		ns
			03		120		ns
			04		80		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +110°C$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Pulse duration, $\overline{RAS}$ high (precharge time) (non-page mode)	$t_{w(RH)}$		01	9,10,11	90		ns
			02		90		ns
			03		120		ns
			04		80		ns
Pulse duration, $\overline{RAS}$ low	$t_{w(RL)}$	See figures 4 and 5	01	9,10,11	120	10000	ns
			02		150	10000	ns
			03		200	10000	ns
			04		100	10000	ns
Write pulse duration	$t_{w(W)}$		01	9,10,11	40		ns
			02		45		ns
			03		50		ns
			04		35		ns
Column address setup time 11/	$t_{su(CA)}$		All	9,10,11	0		ns
Row address setup time 11/	$t_{su(RA)}$		All	9,10,11	0		ns
Data setup time 11/ 13/	$t_{su(D)}$		All	9,10,11	0		ns
Read command setup time 11/	$t_{su(rd)}$		All	9,10,11	0		ns
Early write command setup time before $\overline{CAS}$ low 14/	$t_{su(WCL)}$		All	9,10,11	0		ns
Write command setup time before $\overline{CAS}$ high	$t_{su(WCH)}$		01	9,10,11	40		ns
			02		45		ns
			03		55		ns
			04		35		ns
Write command setup time before $\overline{RAS}$ high	$t_{su(WRH)}$		01	9,10,11	40		ns
			02		45		ns
			03		55		ns
			04		35		ns
Column address hold time after $\overline{CAS}$ low	$t_{h(CLCA)}$		01,02, 03	9,10,11	30		ns
			04		20		ns
Row address hold time	$t_{h(RA)}$		01	9,10,11	20		ns
			02		20		ns
			03		25		ns
			04		15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +110°C$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Column address hold time after $\overline{RAS}$ low	$t_{h(RLCA)}$		01	9,10,11	80		ns
			02		100		ns
			03		130		ns
			04		70		ns
Data hold time after $\overline{CAS}$ low 13/	$t_{h(CLD)}$	See figures 4 and 5	01	9,10,11	40		ns
			02		45		ns
			03		55		ns
			04		35		ns
Data hold time after $\overline{RAS}$ low	$t_{h(RLD)}$		01	9,10,11	100		ns
			02		120		ns
			03		135		ns
			04		85		
Data hold time after $\overline{W}$ low 13/	$t_{h(WLD)}$		01	9,10,11	40		ns
			02		45		ns
			03		55		ns
			04		35		ns
Read command hold time after $\overline{CAS}$ high 11/	$t_{h(CHrd)}$		All	9,10,11	0		ns
Read command hold time after $\overline{RAS}$ high	$t_{h(RHrd)}$		01	9,10,11	20		ns
			02		25		ns
			03		25		ns
			04		10		ns
Write command hold time after $\overline{CAS}$ low	$t_{h(CLW)}$		01	9,10,11	40		ns
			02		45		ns
			03		55		ns
			04		35		ns
Write command hold time after $\overline{RAS}$ low	$t_{h(RLW)}$		01	9,10,11	100		ns
			02		120		ns
			03		135		ns
			04		85		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{RLCH}		01	9,10,11	120		ns
			02		150		ns
			03		200		ns
			04		110		ns
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CHRL}		01,02, 03	9,10,11	20		ns
			03		20		ns
			04		15		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{CLRH}		01	9,10,11	60		ns
			02		75		ns
			03		100		ns
			04		50		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +110°C$	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$ before $\overline{RAS}$ refresh only)	t_{RLCHR}	See figures 4 and 5	01	9,10,11	25		ns
			02		30		ns
			03		40		ns
			04		20		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$ before $\overline{RAS}$ refresh only) 15/	t_{CLRL}		All	9,10,11	10		ns
Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only) 14/ 16/	t_{CLWL}		01	9,10,11	50		ns
			02		60		ns
			03		100		ns
			04		40		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RLCL}		01	9,10,11	30	60	ns
			02		30	75	ns
			03		30	100	ns
			04		25	50	
Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only) 14/ 16/	t_{RLWL}		01	9,10,11	110		ns
			02		135		ns
			03		200		ns
			04		90		ns
Refresh time interval 17/ 18/	t_{rf}		All	9,10,11		4.0	ms
Transition time (rise and fall)	t_t		All	9,10,11	3	100	ns
Output disable time after $\overline{OE}$ high	$t_{dis(GH)}$		All	9,10,11		40	ns
Output enable time after $\overline{OE}$ low 19/	$t_{en(GL)}$		01	9,10,11		60	ns
			02			75	ns
			03			100	ns
			04			35	ns

1/ An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles (READ, WRITE, READ-MODIFY-WRITE, $\overline{RAS}$ refresh) before proper device operation is assured.

2/ AC characteristics assume transition time (t_T) = 5 ns.

3/ V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.

4/ In addition to meeting the transition rate specification, all input signals must make the transition between V_{IL} and V_{IH} (or V_{IH} and V_{IL}) in a monotonic manner.

5/ V_{SS} is common for all voltages.

6/ Specified values are obtained with the output load equal to 2 TTL loads and 100 pF to V_{SS}.

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7/ Capacitance measured with a Boonton meter or equivalent or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and V_{CC} equal to 5.0 V. Capacitance shall be measured only for the initial qualification and after process or design changes which may effect terminal capacitance.

8/ Assumes that $t_{RLCL} <$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds the value shown.

9/ Assumes that $t_{RLCL} \geq t_{RLCL}$ (max).

10/ $t_{dis(CH)}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

11/ Some parameters are conditionally guaranteed that are specified to aid device application. They are not necessarily directly verified by a specific test, however, the vendor uses device characterizations and design specifications to insure all device parameters are within specified performance limits.

12/ If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for $t_{c(P)}$. Footnote 20/ applies to determine valid data out.

13/ These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.

14/ $t_{su(WCL)}$, t_{CLWL} and t_{RLWL} are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{su(WCL)} \geq t_{su(WCL)}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CLWL} \geq t_{CLWL}$ (min) and $t_{RLWL} \geq t_{RLWL}$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

15/ Enables on-chip refresh and address counters.

16/ During a READ-WRITE or READ-MODIFY-WRITE cycle the minimum specifications for t_{RWD} and t_{CWD} must be modified by adding 40 ns to each specification due to $\overline{OE}$ delay.

17/ A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625 µs so that all 256 $\overline{RAS}$ address combinations are executed within 4 ms (regardless of sequence). Distributed refresh is recommended.

18/ A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). This refresh mode must be executed within 4 ms.

19/ If $\overline{OE}$ is taken low then high (V_{IH}) D_{OUT} goes open. If $\overline{OE}$ is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.

20/ If $\overline{CAS}$ = V_{IH} or $\overline{OE}$ = V_{IH} data output is high impedance. If $\overline{CAS}$ = V_{IL} and $\overline{OE}$ = V_{IL} data output may contain data from the last valid READ cycle.

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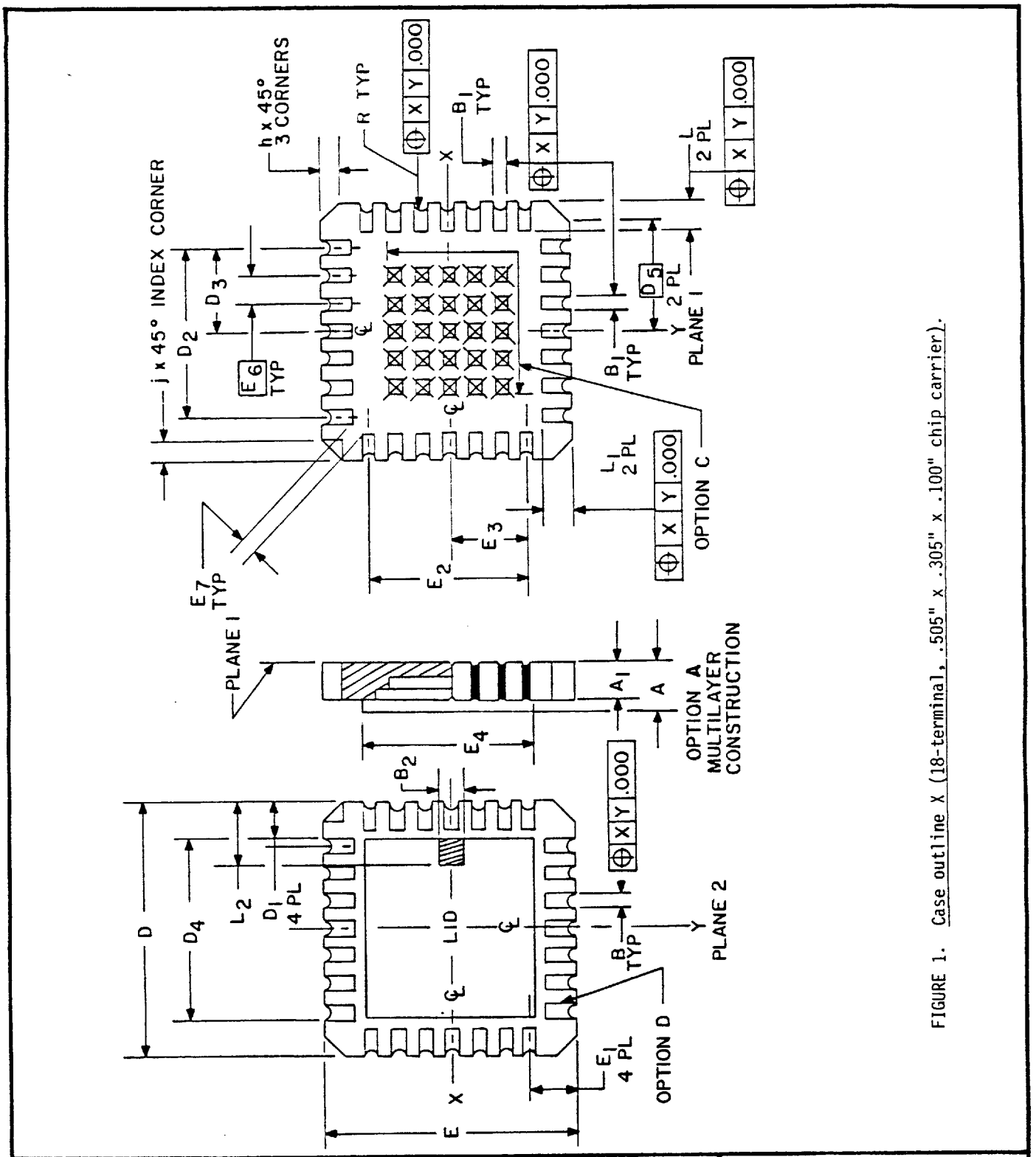

FIGURE 1. Case outline X (18-terminal, .505" x .305" x .100" chip carrier).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87676
		REVISION LEVEL A	SHEET 10

DESC FORM 193A
SEP 87

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9004697 1391703 798

Symbol	Dimensions shown in			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.060	.100	1.52	2.34
A_1	.050	.088	1.27	2.24
A_2	--	--	--	--
B	--	--	--	--
B_1	.022	.028	5.60	7.10
B_2	.022	.041	5.60	1.04
D	.280	.305	7.11	7.75
D_1	.070 REF		1.91 REF	
D_2	.150 REF		3.81 REF	
D_3	.075 BSC		1.78 BSC	
D_4	--	.305	--	7.75
D_5	.120 BSC		3.05 BSC	
E	.480	.505	12.19	12.33
E_1	.145 REF		3.68 REF	
E_2	.200 REF		5.08 REF	

FIGURE 1. Case outline X (18-terminal, .505" x .305" x.100" chip carrier) - Continued.

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Symbol	Dimensions shown in			
	Inches		Millimeters	
	Min	Max	Min	Max
E_3	.100 REF		2.54 REF	
E_4	--	.365	--	9.27
E_5	--		--	
E_6	.050 BSC		1.27 BSC	
E_7	.015	--	.380	--
h	.035	.045	.890	1.14
j	.010	.025	.380	6.40
L	.040	.060	1.02	1.40
L_1	.040	.060	1.02	1.40
L_2	.040	.155	1.02	3.94
N	18		18	
R	.007	.011	1.80	2.80
ND	4		4	
NE	5		5	

FIGURE 1. Case outline X (18-terminal, .505" x .305" x .100" chip carrier) - Continued.

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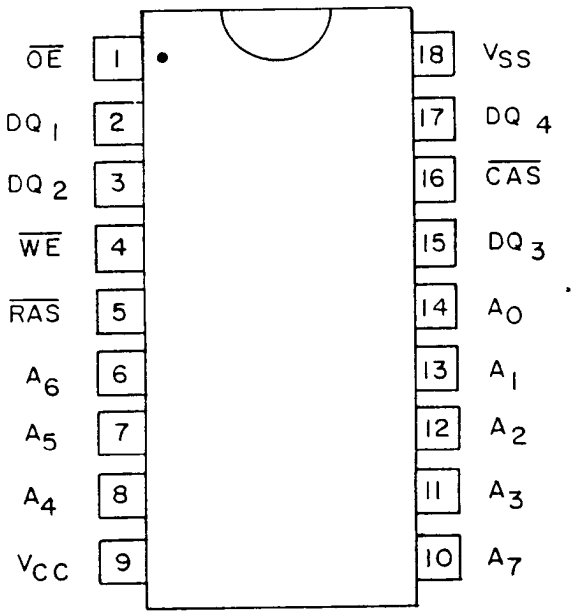
Case V



Top view

FIGURE 2. Terminal connections.

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		REVISION LEVEL	SHEET 13

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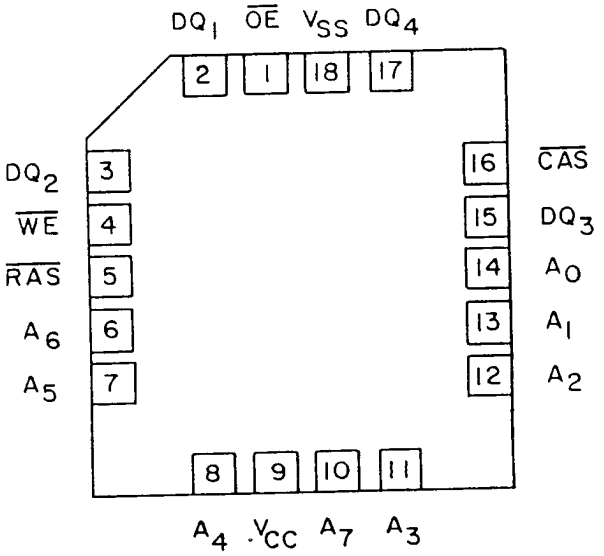
Case X



Top view

FIGURE 2. Terminal connections - Continued.

Device types 01, 02, 03, and 04

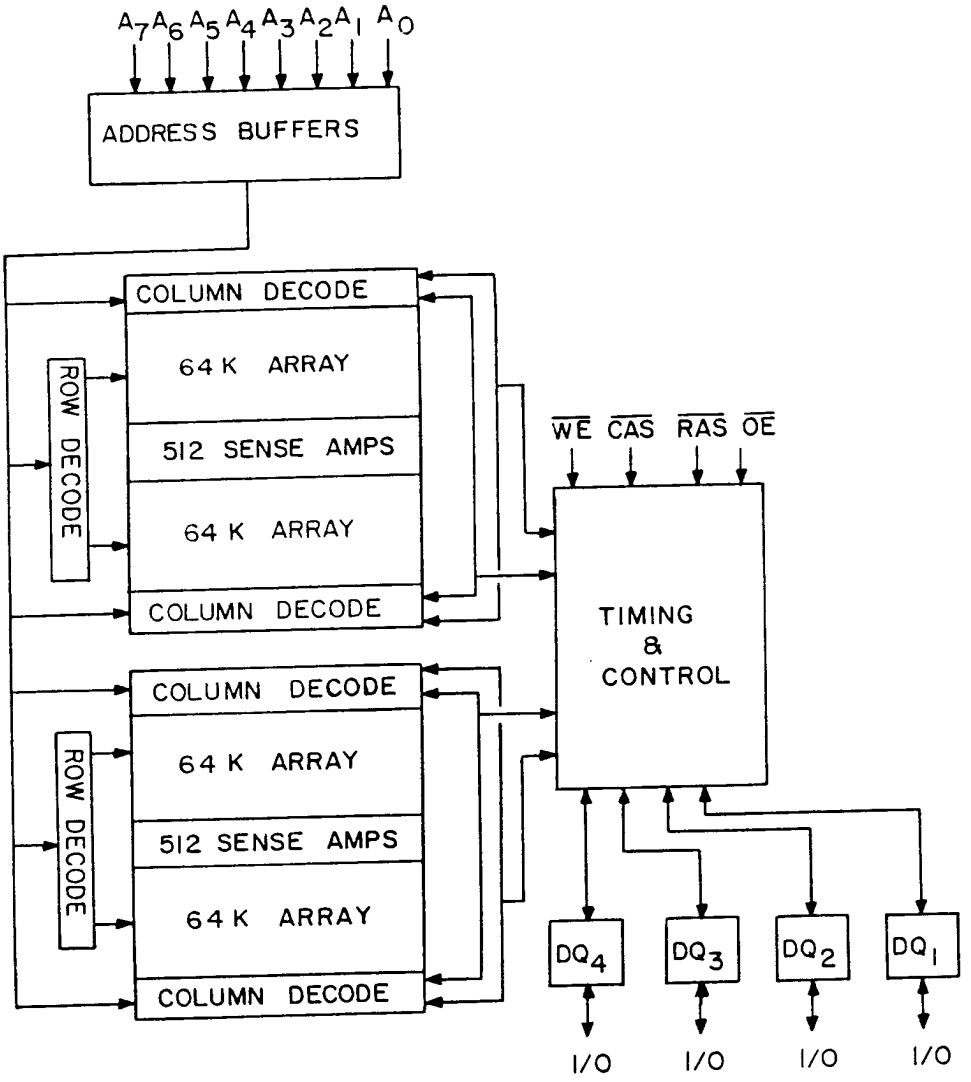


FIGURE 3. Logic diagram.

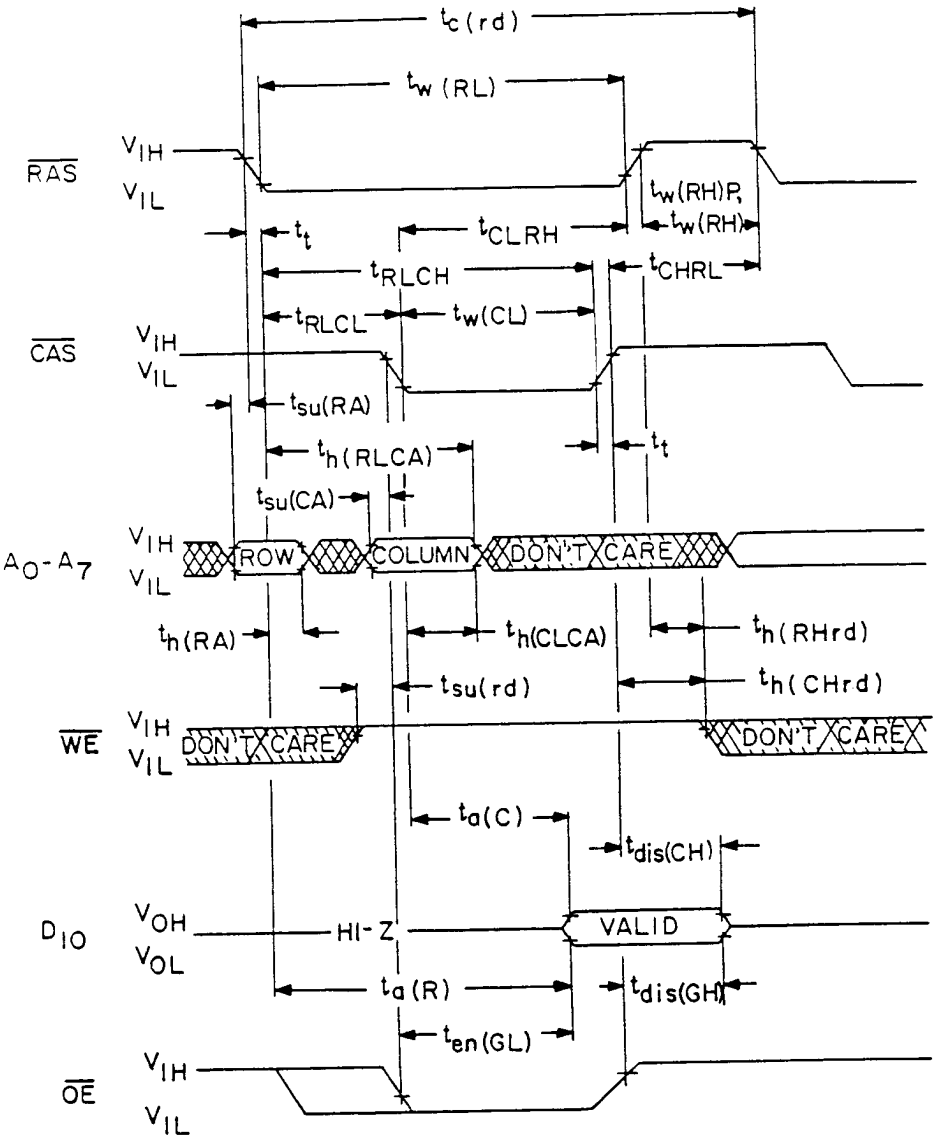


FIGURE 4. Switching waveforms (read cycle timing).

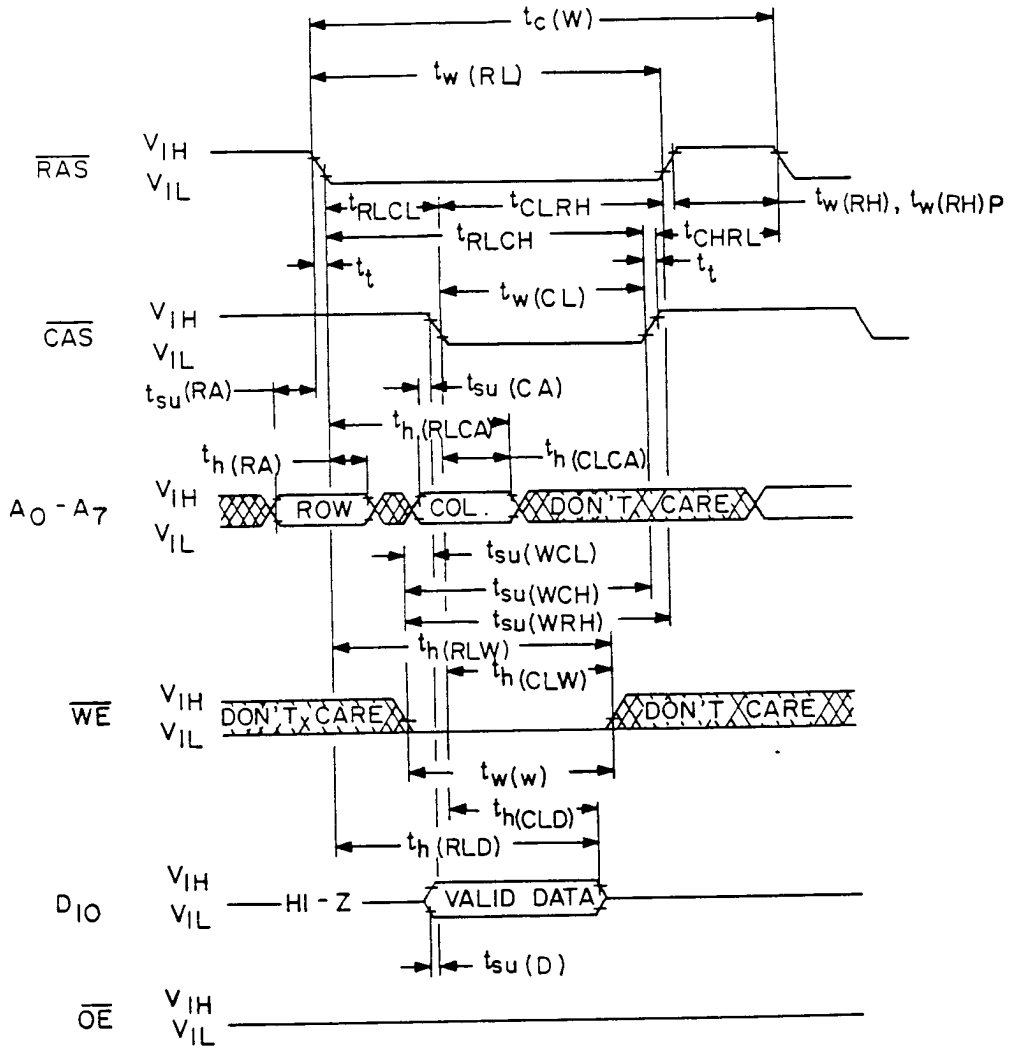


FIGURE 4. Switching waveforms (early write cycle timing) - Continued.

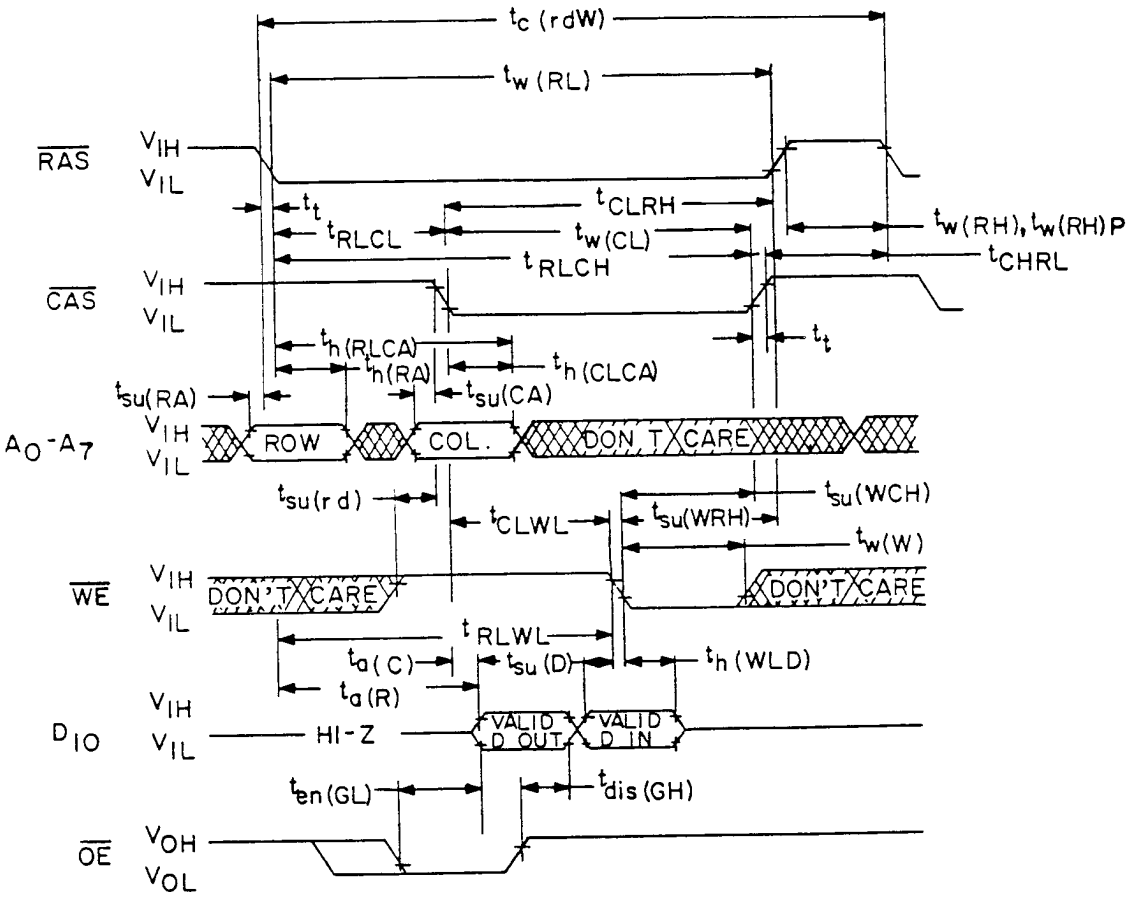


FIGURE 4. Switching waveforms (read-write/read-modify-write cycle timing) - Continued.

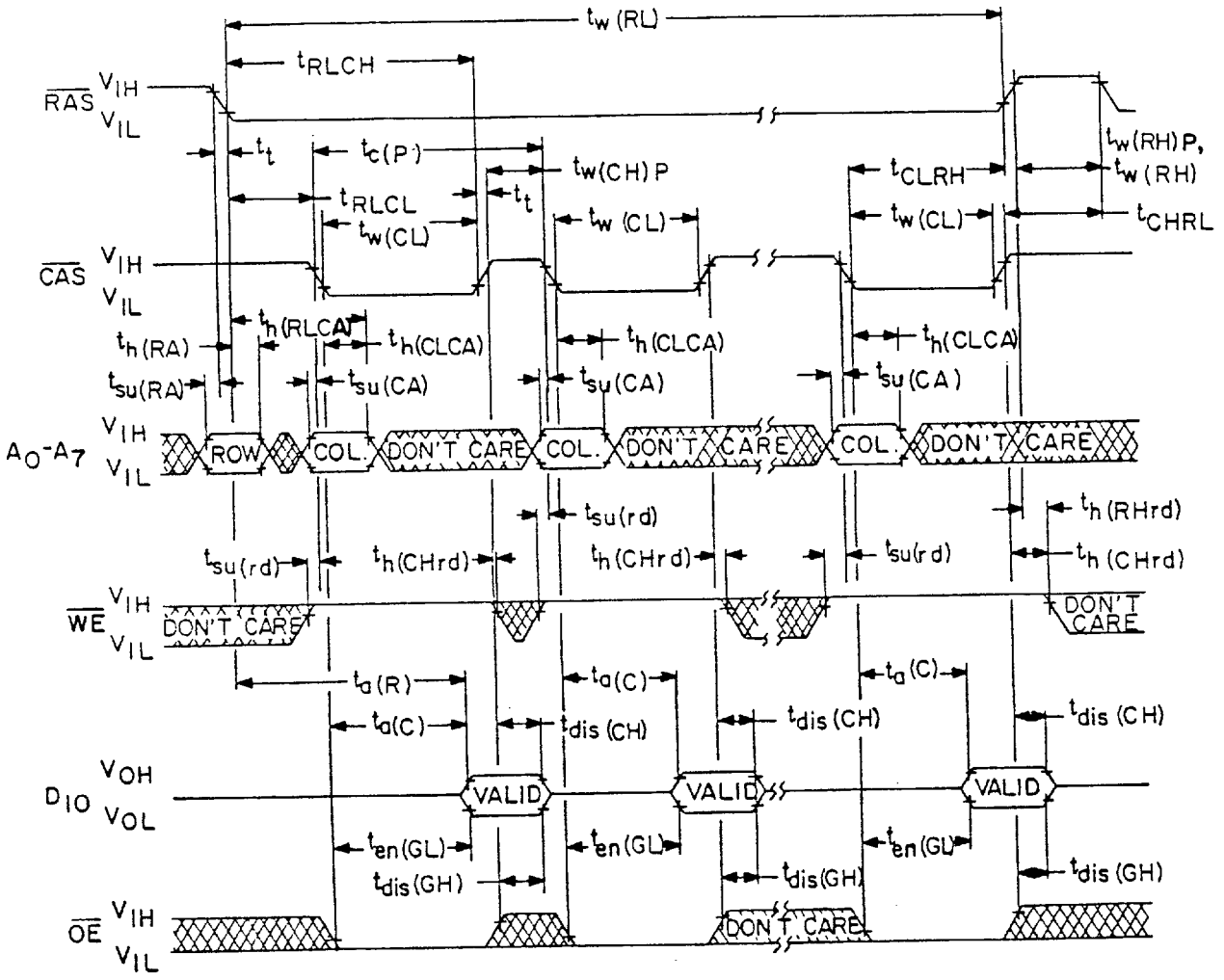


FIGURE 4. Switching waveforms (page-mode read cycle timing) - Continued.

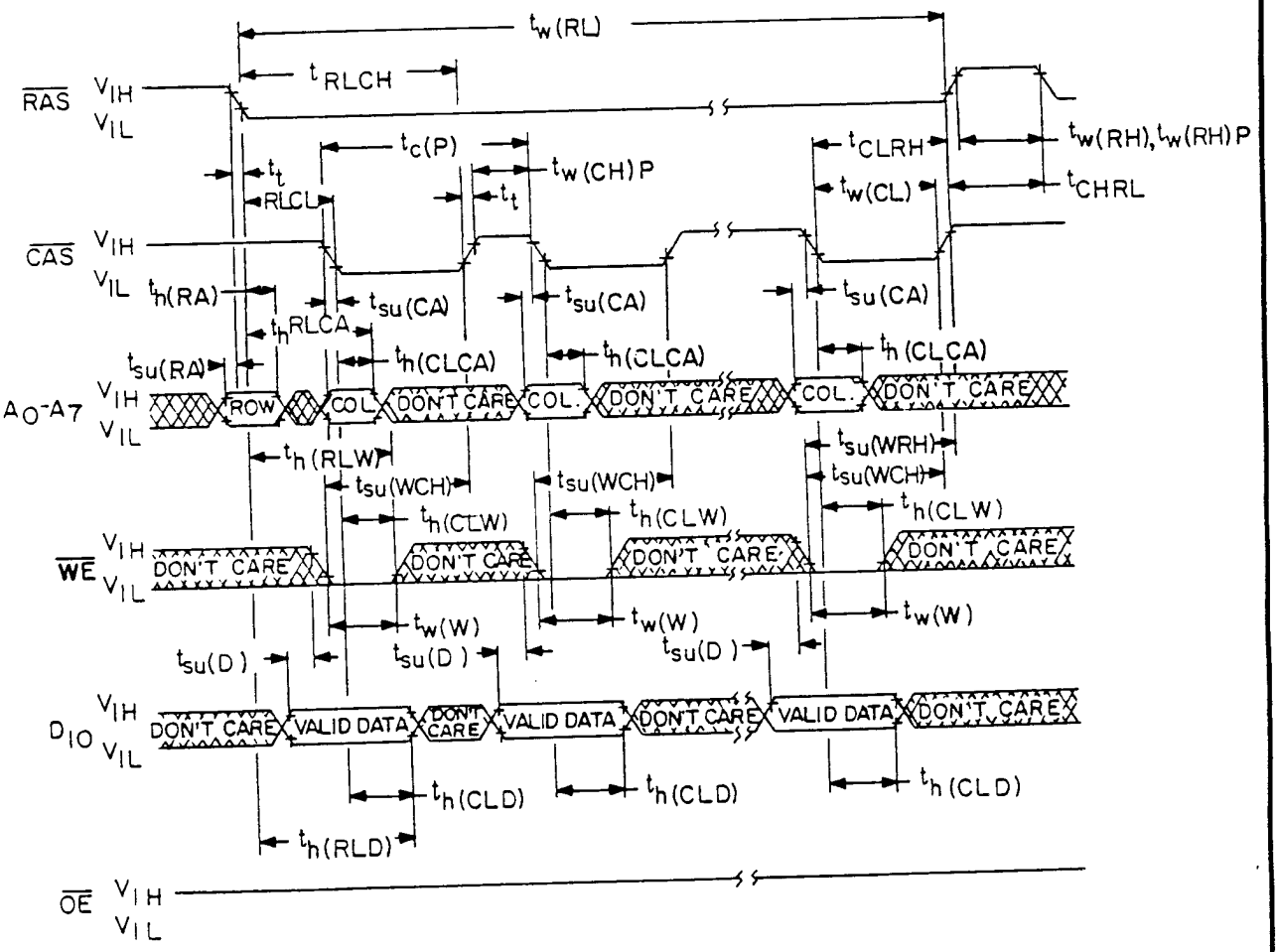


FIGURE 4. Switching waveforms (page-mode early write cycle timing) - Continued.

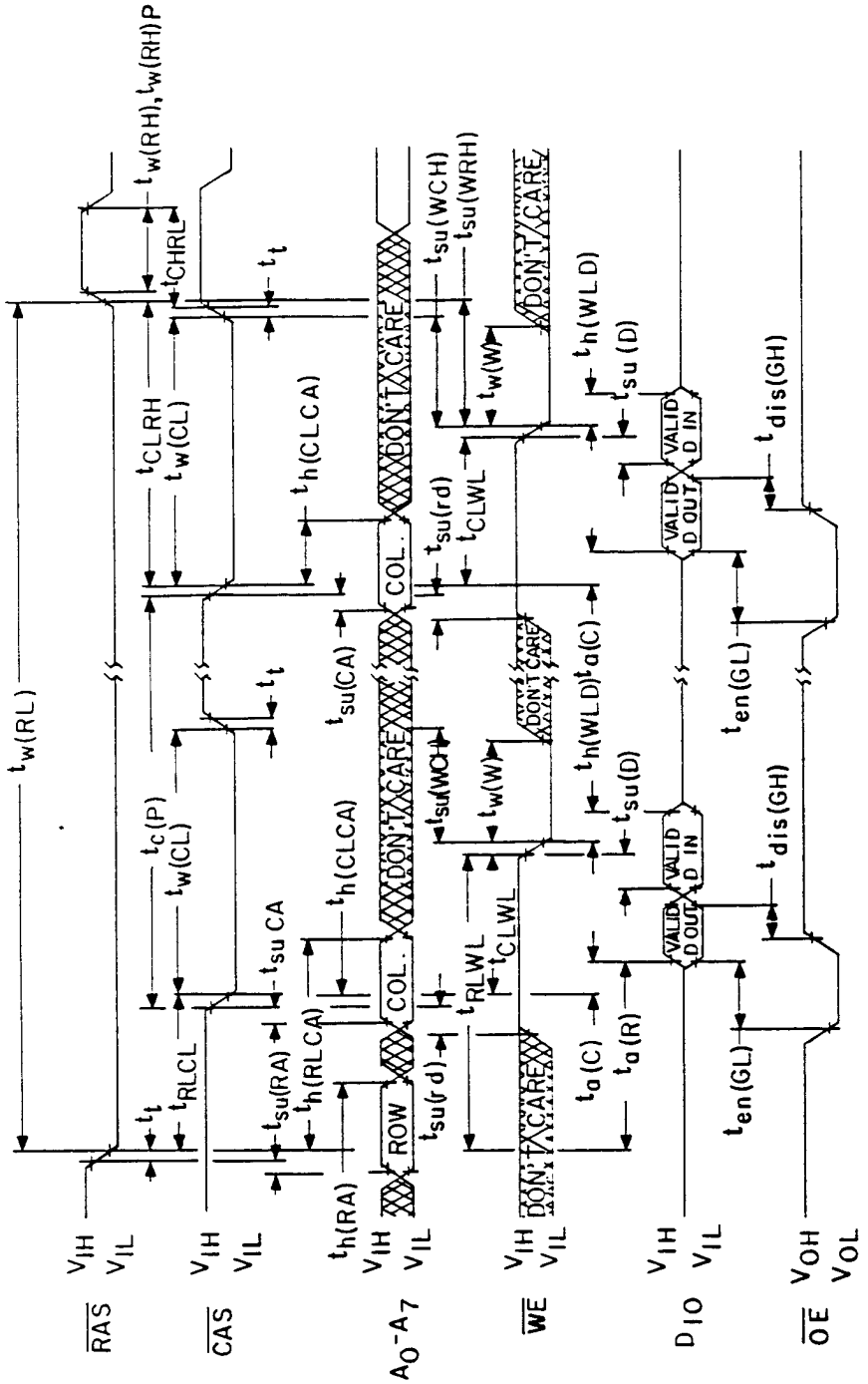


FIGURE 4. Switching waveforms (page-mode read-modify-write cycle time) - Continued.

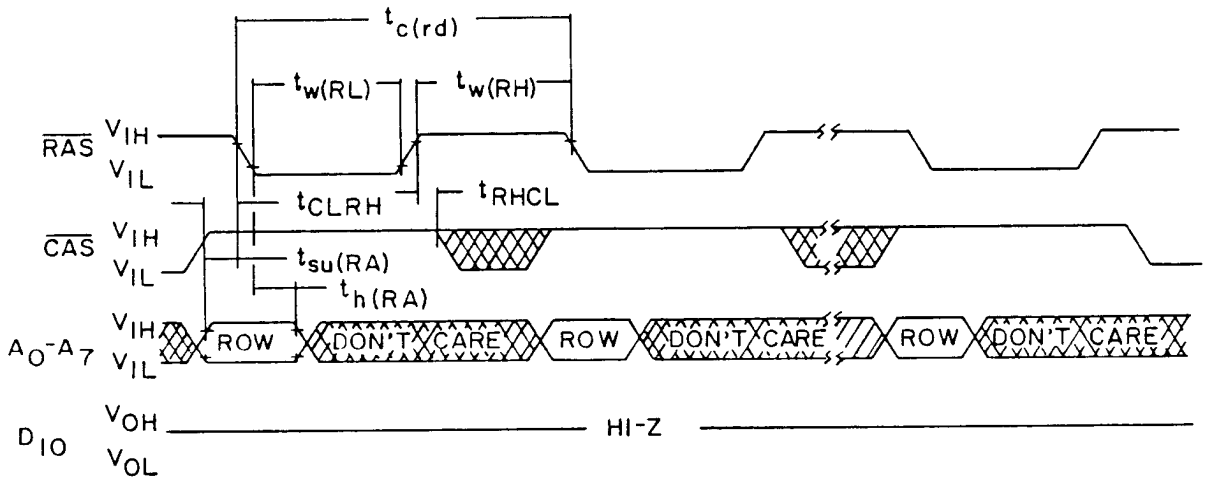


FIGURE 4. Switching waveforms ($\overline{RAS}$-only refresh cycle timing) - Continued.

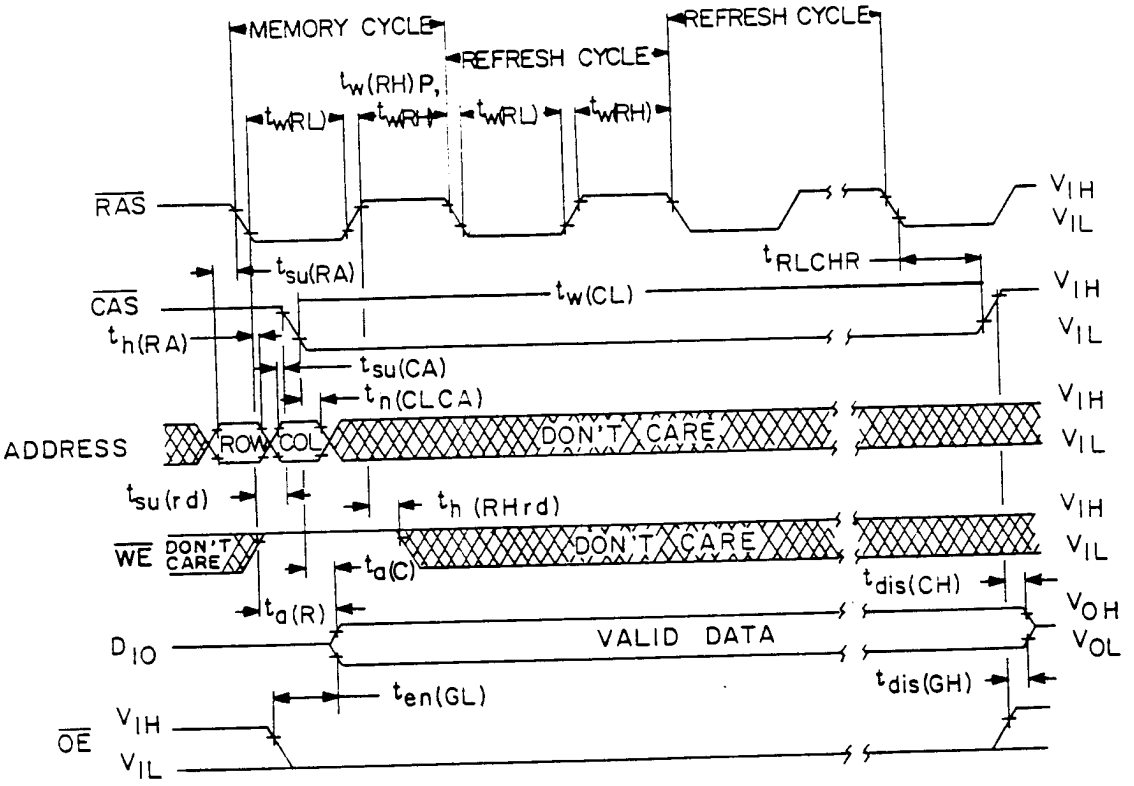


FIGURE 4. Switching waveforms (hidden refresh cycle timing) - Continued.

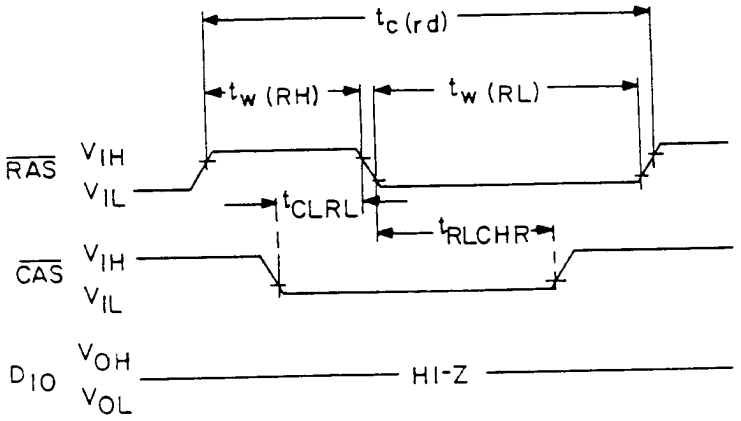
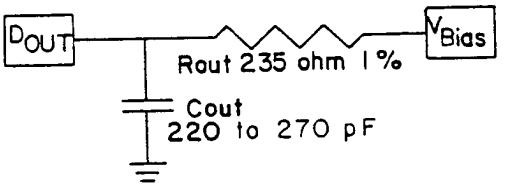


FIGURE 4. Switching waveforms (automatic $\overline{CAS}$-before $\overline{RAS}$ refresh cycle timing) - Continued.



This figure represents the output loading for the I_{OL}/I_{OH} test
V_{Bias} = 1.2 V for I_{OH}, 1.6 V for I_{OL}. The capactive load is
imposed by the test system and it's interface to the device under test.

FIGURE 5. Load circuit.

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3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, 8, and 9 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	2, 10
Final electrical test parameters (method 5004)	1, 2*, 3, 10*, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 10, 11

*PDA applies to subgroups 2 and 10.

1/ Subgroups 10 and 11 requires the complete array to be tested.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8767601VX	6Y440	MT4067C-12
5962-8767601XX	6Y440	MT4067EC-12
5962-8767602VX	6Y440	MT4067C-15
5962-8767602XX	6Y440	MT4067EC-15
5962-8767603VX	6Y440	MT4067C-20
5962-8767603XX	6Y440	MT4067EC-20
5962-8767604VX	6Y440	MT4067C-10
5962-8767604XX	6Y440	MT4067EC-10

1/ Caution. Do not use this number for item acquisition. Item acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
6Y440	Micron Technology, Inc. 2805 E. Columbia Road Boise, ID 83706