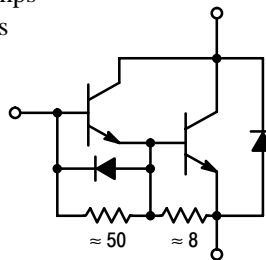


SWITCHMODE™ Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

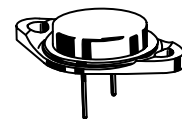
The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated SWITCHMODE applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 1.0 μs (max) Inductive Crossover Time — 20 Amps
 - 2.5 μs (max) inductive Storage Time — 20 Amps
- Operating Temperature Range -65 to +200°C
- Performance Specified for
 - Reversed Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



MJ10015
MJ10016

**50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 AND 500 VOLTS
250 WATTS**



**CASE 197-05
TO-204AE TYPE
(TO-3 TYPE)**

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	V_{CEO}	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous	I_C	50		Adc
— Peak (1)	I_{CM}	75		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	15		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250		Watts
@ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJ10015 MJ10016

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (1)

Collector–Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$, $V_{\text{clamp}} = \text{Rated } V_{\text{CEO}}$)	MJ10015 MJ10016	$V_{\text{CEO(sus)}}$	400 500	— —	— —	Vdc
Collector Cutoff Current ($V_{\text{CEV}} = \text{Rated Value}$, $V_{\text{BE(off)}} = 1.5\text{ Vdc}$)		I_{CEV}	—	—	0.25	mAdc
Emitter Cutoff Current ($V_{\text{EB}} = 2.0\text{ Vdc}$, $I_C = 0$)		I_{EBO}	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{\text{S/b}}$	See Figure 7	
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 8	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 20\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$) ($I_C = 40\text{ Adc}$, $V_{\text{CE}} = 5.0\text{ Vdc}$)	h_{FE}	25 10	— —	— —	—
Collector–Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 50\text{ Adc}$, $I_B = 10\text{ Adc}$)	$V_{\text{CE(sat)}}$	— —	— —	2.2 5.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$)	$V_{\text{BE(sat)}}$	—	—	2.75	Vdc
Diode Forward Voltage (2) ($I_F = 20\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTIC

Output Capacitance ($V_{\text{CB}} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 100\text{ kHz}$)	C_{ob}	—	—	750	pF
--	-----------------	---	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	($V_{\text{CC}} = 250\text{ Vdc}$, $I_C = 20\text{ A}$, $I_{\text{B1}} = 1.0\text{ Adc}$, $V_{\text{BE(off)}} = 5\text{ Vdc}$, $t_p = 25\text{ }\mu\text{s}$ Duty Cycle $\leq 2\%$).	t_d	—	0.14	0.3	μs
Rise Time		t_r	—	0.3	1.0	μs
Storage Time		t_s	—	0.8	2.5	μs
Fall Time		t_f	—	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	($I_C = 20\text{ A(pk)}$, $V_{\text{clamp}} = 250\text{ V}$, $I_{\text{B1}} = 1.0\text{ A}$, $V_{\text{BE(off)}} = 5.0\text{ Vdc}$)	t_{sv}	—	1.0	2.5	μs
Crossover Time		t_c	—	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

(2) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads.

Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

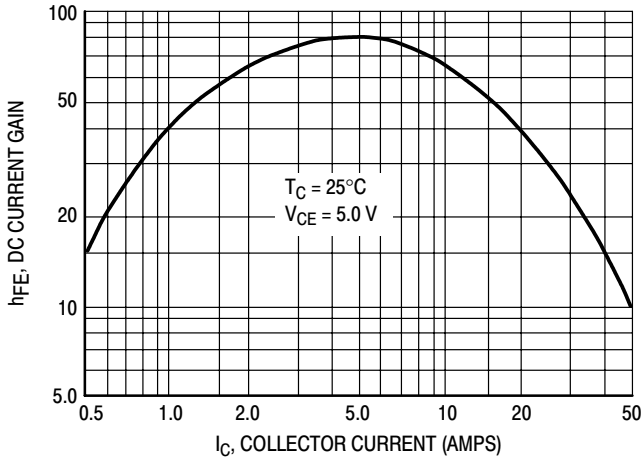


Figure 1. DC Current Gain

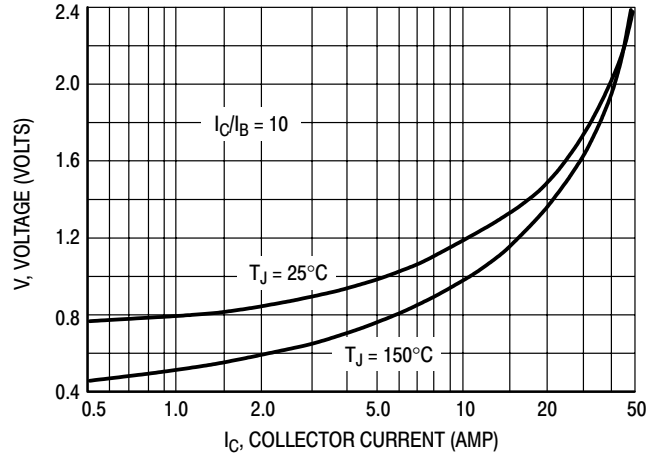


Figure 2. Collector-Emitter Saturation Voltage

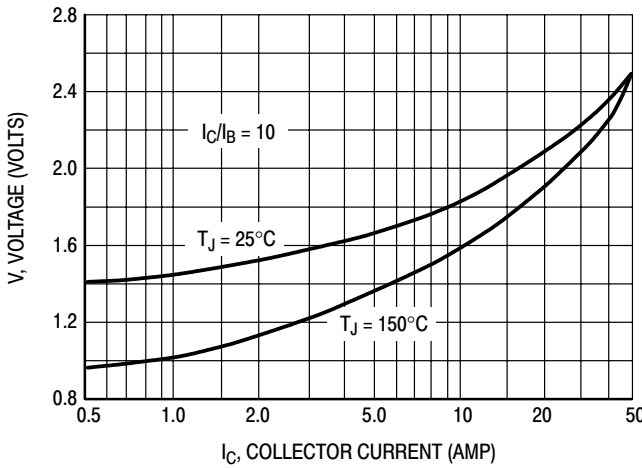


Figure 3. Base-Emitter Saturation Voltage

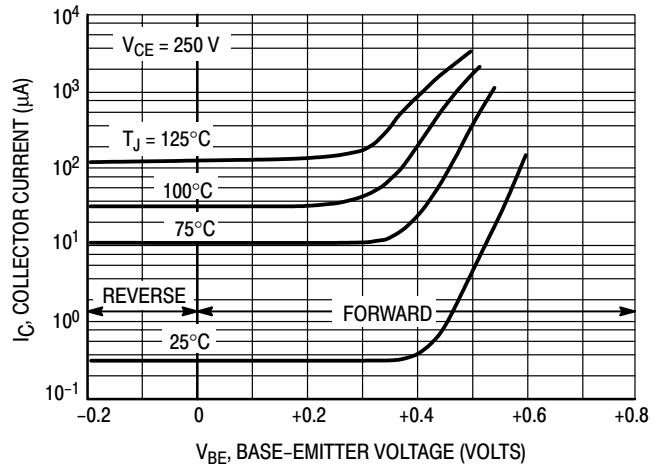


Figure 4. Collector Cutoff Region

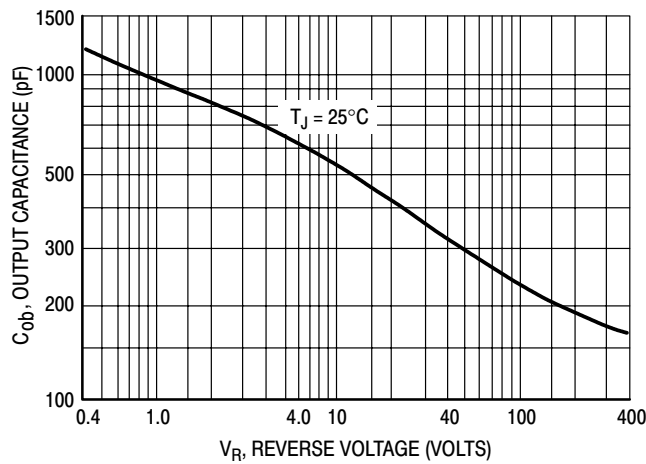


Figure 5. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	V _{CEO(sus)}	V _{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 100 mA</p>	<p>INDUCTIVE TEST CIRCUIT</p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = V_{CEO(sus)}</p>	<p>L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V</p>	<p>V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 = \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{Cpk})}{V_{Clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

*Adjust -V such that V_{BE(off)} = 5 V except as required for RBSOA (Figure 8).

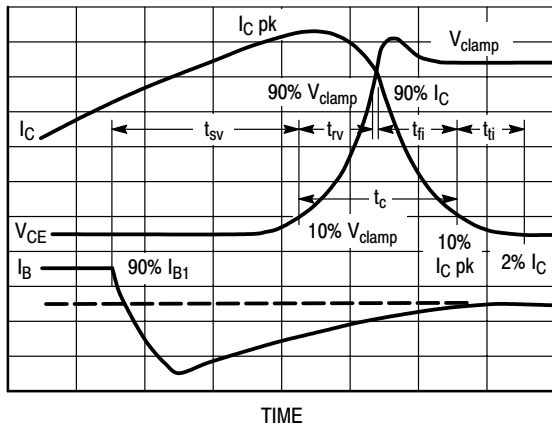


Figure 6. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage

waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, t_{rv} + t_{fi} ≈ t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

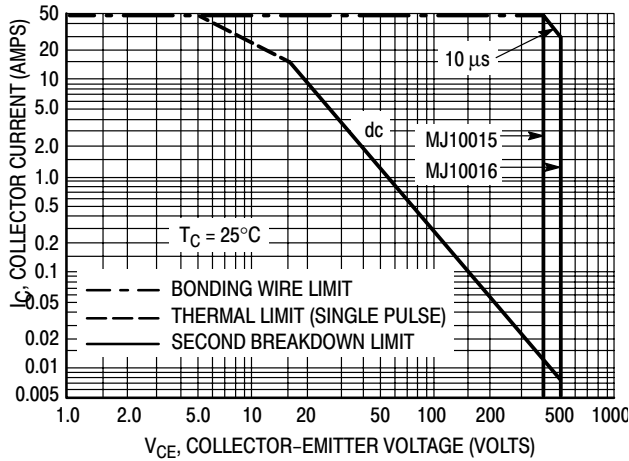


Figure 7. Forward Bias Safe Operating Area

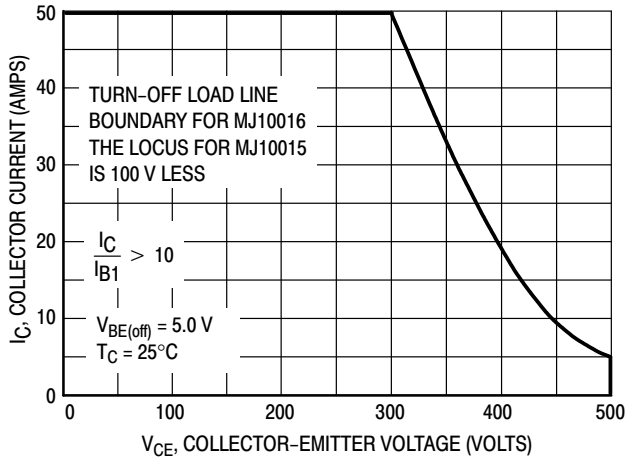


Figure 8. Reverse Bias Switching Safe Operating Area

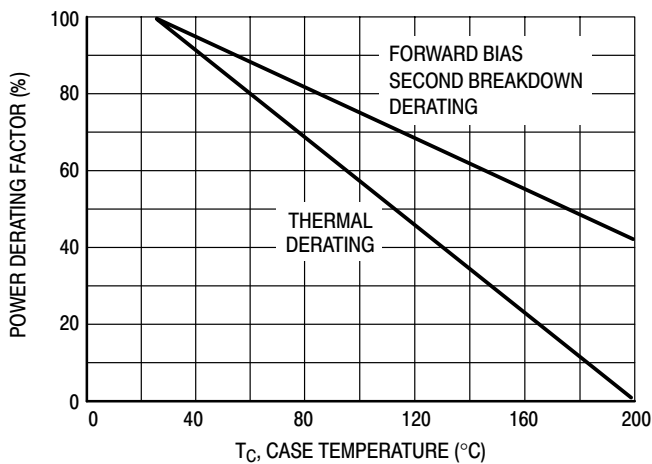


Figure 9. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

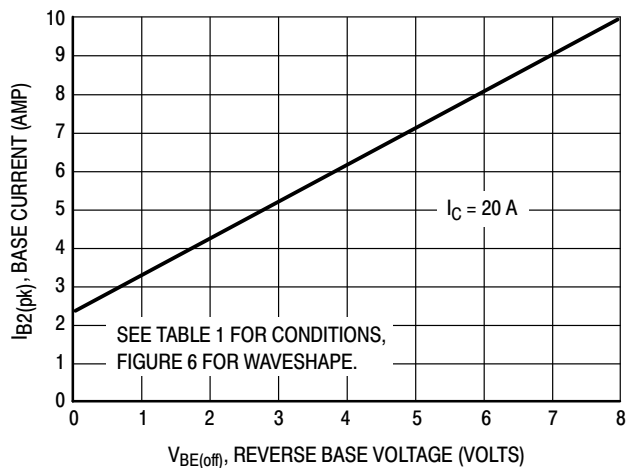
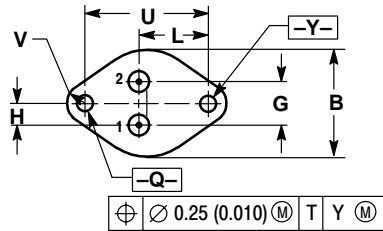
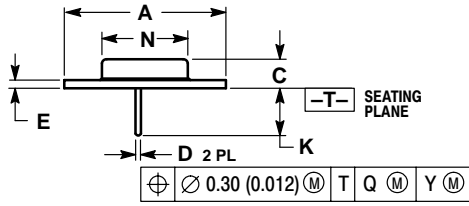


Figure 10. Typical Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

MJ10015 MJ10016

PACKAGE DIMENSIONS

TO-204AE (TO-3)
CASE 197A-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

Notes

SWITCHMODE is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com

French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com

English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 1-303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:

001-800-4422-3781

Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

Phone: 81-3-5740-2700

Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.