REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Reword paragraph 4.3.1d. Update vendor's part numbers. Editorial changes throughout.	22 June 1987	

REV STATUS OF PAGES	REV	A				A						A					A
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Defense Electronics
Supply Center
Dayton, Ohio

Original date of drawing:
18 September 1986

AMSC N/A

PREPARED BY Sandra Rooney

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MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 2K X 8 BIT BIPOLAR PROM, MONOLITHIC SILICON

SIZE A	CODE IDENT. NO. **14933**	DWG NO. 5962-85526
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5962-E423

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85526	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27PS191	2048 X 8-bit bipolar PROM (three-state)	75 ns
02	27PS191A	2048 X 8-bit bipolar PROM (three-state)	65 ns
03	27PS291	2048 X 8-bit bipolar PROM (three-state)	75 ns
04	27PS291A	2048 X 8-bit bipolar PROM (three-state)	65 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline	
J	D-3 (24-lead, 1/2" X 1 1/4"), dual-in-line package	Dip 24.6
K	F-6 (24-lead, 3/8" X 5/8"), flat package	Flp, 24
L	D-9 (24-lead, 1/4" X 1 1/4"), dual-in-line package	Dip 24.3
X	C-12 (32-terminal, .450" X .550"), rectangular chip carrier	Lcc type E32
3	C-4 (28-terminal, .450" X .450"), square chip carrier	Lcc type G28

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to + 150°C
Maximum power dissipation (P_D) 1/	1.02 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}): 2/	
Cases J, K, L	See MIL-M-38510, appendix C
Case X	80°C/W 3/
Case 3	80°C/W 3/
DC voltage applied to outputs (except during programming)	-0.5 V to $+V_{CC}$ maximum
DC voltage applied to outputs during programming	21 V
Output current into outputs during programming (maximum duration of 1 s)	250 mA
DC input current	-30 mA to +5 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2/ Heat sinking is recommended to reduce the junction temperature.

3/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed device. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = MIN, I_{OH} = -2.0 mA $V_{IN} = V_{IH}$ or V_{IL}	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = MIN, I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL}	1,2,3	All		0.50	V
Input high level	V_{IH}	Guaranteed input logical high voltage for all inputs 1/	1,2,3	All	2.0		V
Input low level	V_{IL}	Guaranteed input logical low voltage for all inputs 1/	1,2,3	All		0.8	V
Input low current	I_{IL}	V_{CC} = MAX, V_{IN} = 0.45 V	1,2,3	All		-250	µA
Input high current	I_{IH}	V_{CC} = MAX, $V_{IN} = V_{CC}$	1,2,3	All		40	µA
Output short circuit current	I_{OS}	V_{CC} = MAX, V_{OUT} = 0.0 V 2/	1,2,3	All	-15	-90	mA
Power supply current	I_{CC}	All inputs = GND	1,2,3	All		185	mA
Power down supply current	I_{CCD}	$\overline{CS}_1$ = 2.7 V All other inputs = GND	1,2,3	All		80	mA
Input clamp voltage	V_I	V_{CC} = MIN, I_{IN} = -18 mA	1,2,3	All		-1.2	V
Output leakage current	I_{CEX}	V_{CC} = MAX, $V_O = V_{CC}$	1,2,3	All		40	µA
		V_{CS_1} = 2.4 V, V_O = 0.4 V				-40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input capacitance	C_{IN}	V_{IN} = 2.0 V at f = 1 MHz 3/	4	All		8	pF
Output capacitance	C_{OUT}	V_{OUT} = 2.0 V at f = 1 MHz 3/	4	All		14	pF
Address access time	t_{AA}	See figures 4 and 5 4/	9,10,11	01, 03 02, 04		75 65	ns ns
Enable access time	t_{EA}	See figures 4 and 5 5/	9,10,11	01, 03 02, 04		90 75	ns ns
Enable recovery time	t_{ER}	See figures 4 and 5 5/	9,10,11	01, 03 02, 04		45 30	ns ns
Power switched address access time	t_{AAPS}	See figures 4 and 5	9,10,11	01, 03 02, 04		90 75	ns ns

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

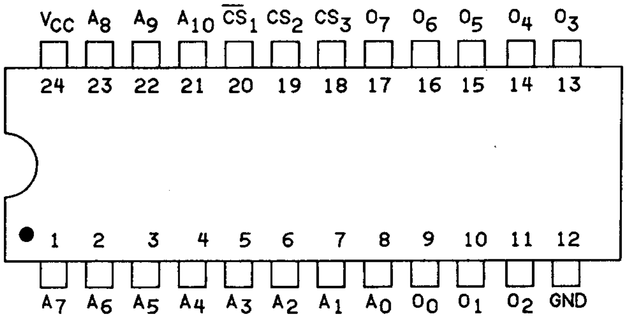
2/ Not more than one output should be shorted at a time. Duration of the short circuit should not be more than 1 second.

3/ These parameters are not 100 percent tested, but are tested initially and after any design or process change affecting C_{IN} or C_{OUT}.

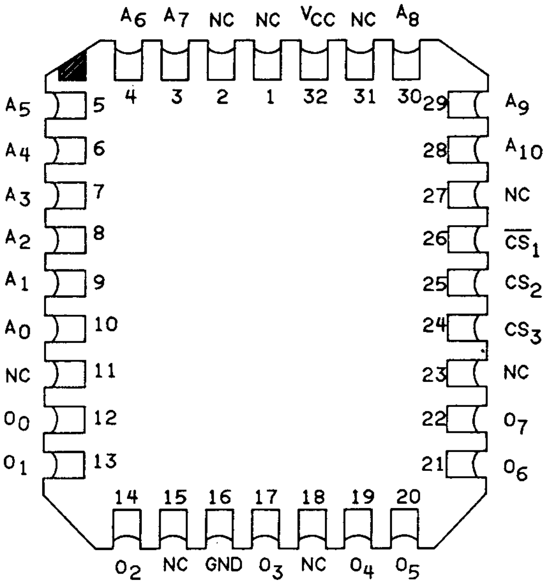
4/ t_{AA} is tested with switch S_1 closed and C_L = 30 pF.

5/ t_{EA} is tested with C_L = 30 pF to the 1.5 V level; S_1 is open for high impedance to high tests and closed for high impedance to low tests. t_{ER} is tested with C_L = 5 pF. High to high impedance tests are made with S_1 open to an output voltage of V_{OH} -0.5 V with S_1 open; low-to-high impedance tests are made to the V_{OL} +0.5 V level with S_1 closed.

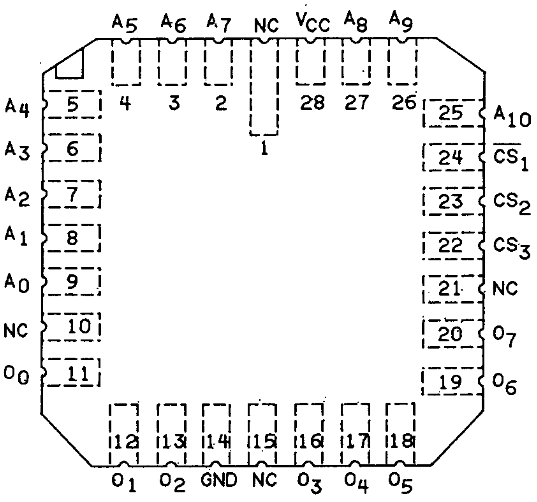
Cases J, K, and L



Case X



Case 3



NOTE: Pin 1 is marked for orientation

FIGURE 1. Terminal connections.

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Word no.	Enable		Address													Data						
	$\overline{CS_1}$	CS_2	CS_3	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
NA	L	H	H	X	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
	L	H	L	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
	L	L	H	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
	H	H	H	X	X	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC

NOTES:
NA = Not applicable.
X = Input may be high level, low level, or open circuit.
OC = Open circuit (high resistance output).

FIGURE 2. Truth table.

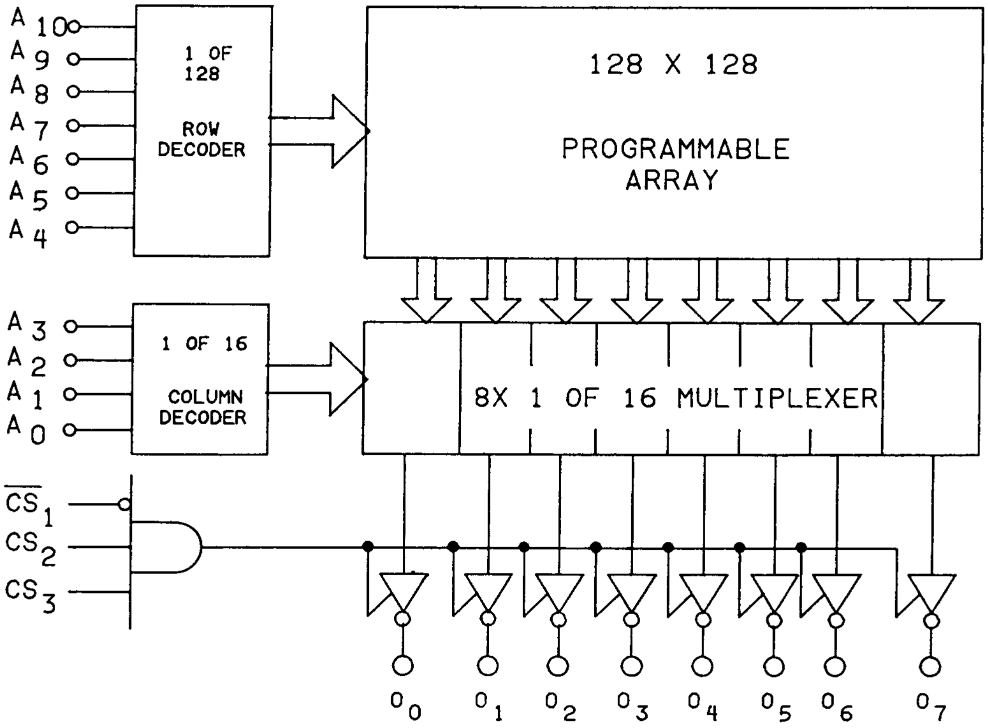

FIGURE 3. Logic diagram.

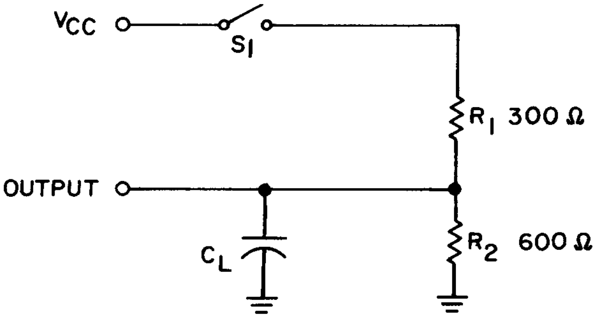

FIGURE 4. Switching test circuit.

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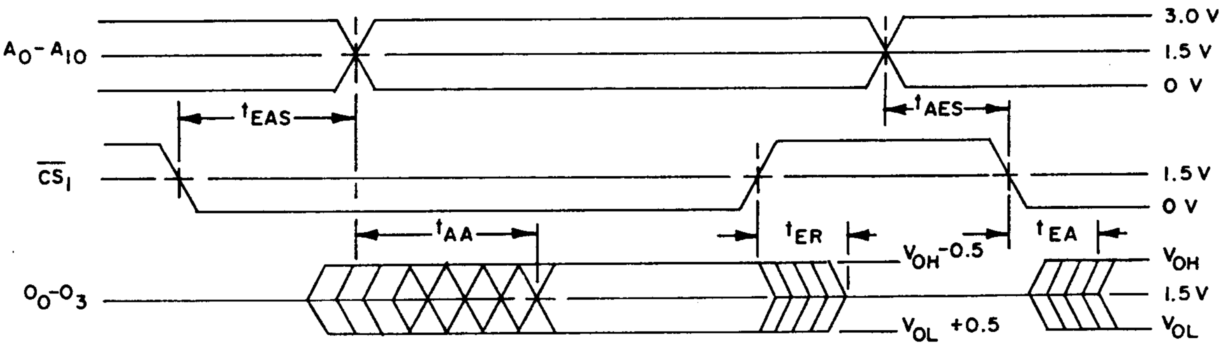


NOTE: Level on output while $\overline{CS}_1$, is high or CS_2 or CS_3 are low is determined externally.

KEY TO SWITCHING WAVEFORMS

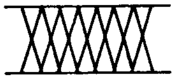
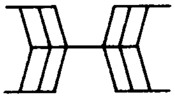
Waveform	Inputs	Outputs
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown
	Does not apply	Center line is high impedance off-state

FIGURE 5. Switching waveform.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}/C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test pattern shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. The group C, subgroup sample shall include devices tested in accordance with paragraph 4.3.1d.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1 2/, 2, 3, 7 2/ 3/, 8 3/, 9, 10, 11
Final electrical test parameters (method 5004) for programmed devices	1 2/, 2, 3, 7 2/ 3/, 8 3/, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7 3/, 8 3/, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7 3/, 8 3/
Additional electrical subgroups for group C periodic inspections	---

1/ Any or all subgroups may be combined when using high speed memory testers.

2/ PDA applies to subgroups 1 and 7.

3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

4.4 Programming procedures for method A.

a. Connect the device in the electrical configuration for programming. The waveforms on figure 6 and the programming characteristics of table III shall apply to these procedures.

b. Terminate all outputs to V_{ONP} through a pull-up resistor R.

c. Apply V_{CCP} to V_{CC}.

d. Connect $\overline{CS}_1$ to V_{ILP}; connect CS_2 and CS_3 to V_{IHP}.

e. Address the PROM with the binary address of the selected word to be programmed.

f. After a delay of t_1, apply V_{OP} for a duration of t_p + rise time of CS_1 input + t_2 to the output selected for programming. After a delay of t_2 + rise time of programmed output, apply V_{CS_1P} for a duration of t_P + rise time of programmed output + t_3 to the CS_1 input; $\overline{CS}_1$ is then reduced to V_{ILP}.

g. After a delay of t_4, opening of the fuse is verified. During verification, V_{CC} remains unchanged at V_{CCP}.

h. The outputs should be programmed one at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low-level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.

i. Repeat steps 4.4a through 4.4g for all bits to be programmed.

j. If any unit does not verify as programmed, it shall be considered a programming reject.

TABLE III. Programming characteristics for method A.

Test	Symbol	Conditions T_C = +25°C 1/ 2/ 3/ 4/	Limits Min	Limits Max	Unit
V_{CC} during programming	V_{CCP}		5.0	5.5	V
Input high level during programming	V_{IHP}		2.4	5.5	V
Input low level during programming	V_{ILP}		0.0	0.45	V
CS_1 voltage during programming	$V_{\overline{CS}_1P}$		14.5	15.5	V

See footnotes at end of table.

TABLE III. Programming characteristics for method A - Continued.

Test	Symbol	Conditions T_C = +25°C 1/ 2/ 3/ 4/	Limits		Unit
			Min	Max	
Output voltage during programming	V_{OP}		19.5	20.5	V
Voltage on outputs not to be programmed	V_{ONP}		0	V_{CCP} +0.3	V
Current into outputs not to be programmed	I_{ONP}			20	mA
Rate of output voltage change	$d(V_{OP})/dt$		20	250	V/µs
Rate of $\overline{CS}_1$ voltage change	$d(V_{\overline{CS}_1})/dt$		100	1000	V/µs
Programming period	t_p		50	100	µs

1/ All delays between edges are specified from completion of the first edge to beginning of the second edge: i.e., not to the midpoints.

2/ Delays t_1, t_2, t_3, and t_4 must be greater than 100 ns, maximum delays of 1 µs are recommended to minimize heating during programming.

3/ During t_v, the output being programmed is switched to the load R and read to determine if the fuse is open.

4/ Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

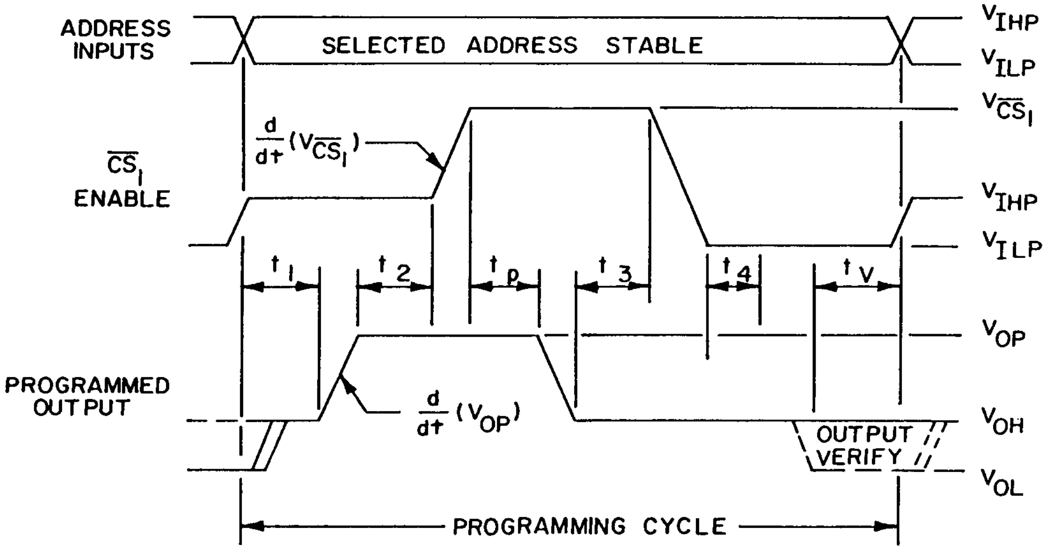

FIGURE 6. Programming waveform.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8552601JX	34335	AM27PS191/BJA	---
5962-8552601KX	34335	AM27PS191/BKA	---
5962-8552601XX	34335	AM27PS191/BUA	---
5962-85526013X	34335	AM27PS191/B3A	---
5962-8552602JX	34335	AM27PS191A/BJA	---
5962-8552602KX	34335	AM27PS191A/BKA	---
5962-8552602XX	34335	AM27PS191A/BUA	---
5962-85526023X	34335	AM27PS191A/B3A	---
5962-8552603LX	34335	AM27PS291/BLA	---
5962-8552604LX	34335	AM27PS291A/BLA	---

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Programming procedure	Fusable link
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	A	Platinum silicide fuse

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