Ultra Fast USB 2.0 SD/MMC Flash Media Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB2244/USB2244i is a USB 2.0 compliant, high speed Bulk Only Mass Storage Class Peripheral Controller intended for reading and writing to SD/MMC Flash Media Cards.

The SMSC USB2244/USB2244i is a fully integrated, single chip solution capable of ultra high performance operation. Average sustained transfer rates exceeding 35MB/s are possible if the media and host can support those rates. Provisions to read/write secure media formats is also provided.

General Features

- 36-pin QFN (6x6mm) lead-free RoHS compliant package
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media
- Product name with “i” denotes the version that supports the industrial temperature range of -40ºC to 85ºC
- Support included for secure media format on a licensed, customized basis
  - SD Secure

Hardware Features

- Single Chip Flash Media Reader/Writer
  - Secure Digital 2.0
    - HS-SD, HC-SD, TransFlash™ and reduced form factor media
  - MultiMediaCard Specification 4.2
    - 1/4/8 bit MMC
- SDIO and MMC Streaming Mode support
- Extended configuration options
  - Socket switch polarities, etc.
- Media Activity LED
- GPIO configuration and polarity
  - Up to 8 GPIOs for special function use: LED indicators, power control to memory devices, etc. The number of actual GPIO’s depends on the implementation configuration used.
  - One GPIO with up to 200 mA drive
- On Board 24MHz Crystal Driver Circuit
- Internal Card Power FET
  - 200mA
  - "Fold-back" short circuit current protected
- 8051 8-bit microprocessor
  - 60MHz - single cycle execution
  - 64KB ROM; 14KB RAM
- Internal Regulator for 1.8V core operation
- Optimized pinout improves signal routing, easing implementation and allowing for improved signal integrity

Mask Programmable Features

- VID/PID/Language ID
- 28-character Manufacturer ID and Product string
- 12-hex digit (max) Serial Number string
- Customizable Vendor specific data LED blink interval or duration

Software Features

- Optimized for low latency interrupt handling
- Reduced memory footprint
- Please see the USB2244/USB2244i Software Release Notes for additional Software Features.

Applications

- Flash Media Card Reader/Writer
- Printers
- Desktop and Mobile PCs
- Consumer A/V
- Media Players/Viewers
- Vista ReadyBoost™
- Compatible with Microsoft Vista, Windows XP, Windows ME, Windows 2K SP4, Apple OSx, and Linux Mass Storage Class Drivers

ORDER NUMBER:

USB2244/USB2244i-AEZG-XX for 36 pin, QFN Lead-Free RoHS Compliant Package

“XX” in the order number indicates the internal ROM firmware revision level. Please contact your SMSC sales representative for more information.

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Chapter 1 Acronyms

MMC: MultiMediaCard

PLL: Phase-Locked Loop

QFN: Quad Flat no Leads

RoHS: Restriction of Hazardous Substances Directive

SD: Secure Digital

SDIO: Secure Digital Input/Output

SDC: Secure Digital Controllerl

SIE: Serial Interface Engine

Chapter 2 Block Diagram

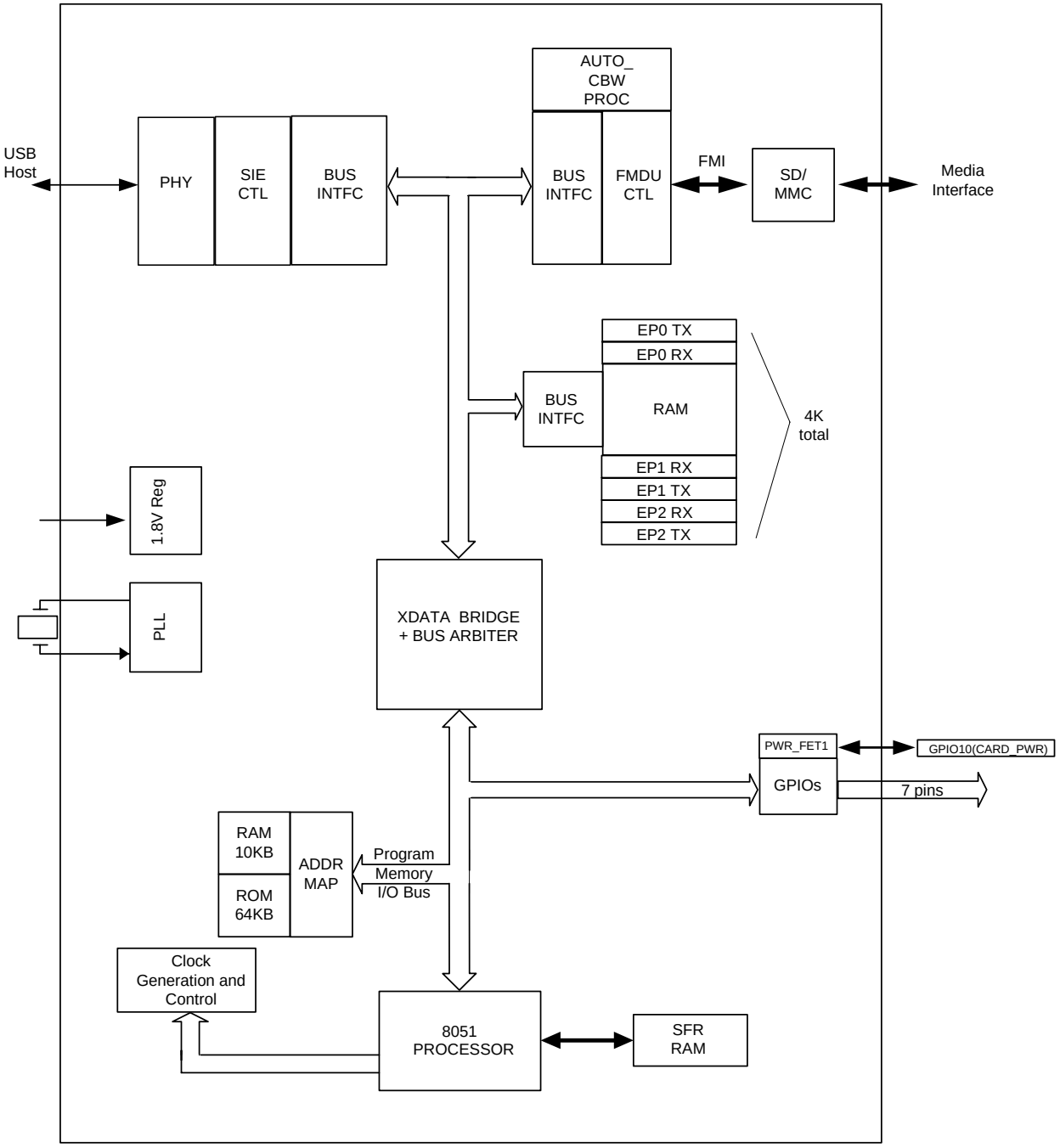


Figure 2.1 USB2244/USB2244i Block Diagram

Chapter 3 Pin Table

3.1 36-Pin Package

Table 3.1 USB2244/2244i 36-Pin QFN Package

SD/MMC INTERFACE (12 Pins)			
SD_D0	SD_D1	SD_D2	SD_D3
SD_D4	SD_D5	SD_D6	SD_D7
SD_CLK	SD_CMD	SD_WP	GPIO15 (SD_nCD)
USB INTERFACE (7 PINS)			
USB+	USB-	RBIAS	
XTAL1 (CLKIN)	XTAL2	VDDA33	VDD18PLL
MISC (13 PINS)			
GPIO1 (LED1)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK
GPIO10 (CRD_PWR)	GPIO12	GPIO14	(4) NC
TEST	nRESET		
DIGITAL, POWER (4 PINS)			
(3)VDD33	VDD18		
TOTAL 36			

Chapter 4 Pin Configuration

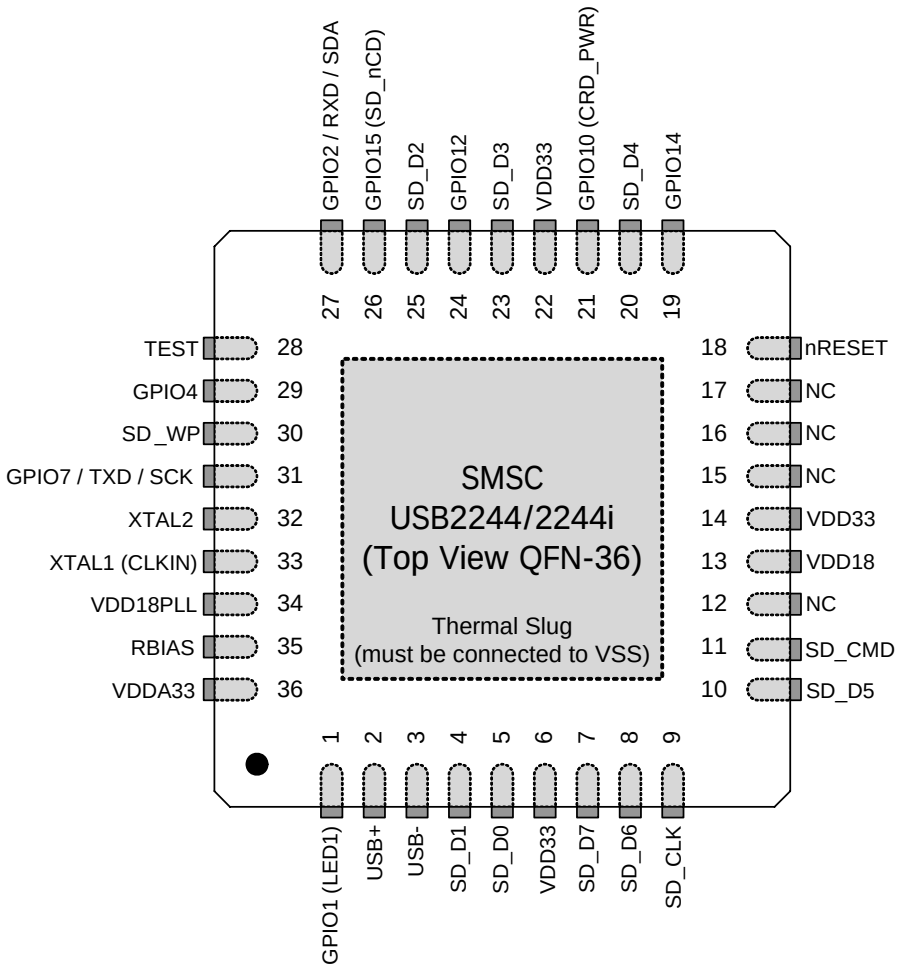


Figure 4.1 USB2244/USB2244i 36 Pin QFN Diagram

Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 Pin Descriptions

Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
SECURE DIGITAL INTERFACE				
SD Data	SD_D[7:0]	7 8 10 20 23 25 4 5	I/O12PU	The bi-directional signals should have weak pull-up resistors. The register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE_CTL
SD Clock	SD_CLK	9	O12	This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD Command	SD_CMD	11	I/O12PU	This is a bi-directional signal that connects to the CMD signal of SD/MMC device. The bi-directional signal should have an internal weak pull-up resistor. The pull-up register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE CTL
SD Write Protect	SD_nWP	30	I/O12	This pin is designated as the Secure Digital card mechanical write detect pin.
SD Card Detect GPIO	GPIO15 (SD_nCD)	26	I/O12	This is a GPIO designated as the Secure Digital card detection pin.
USB INTERFACE				
USB Bus Data	USB+ USB-	2 3	I/O-U	These pins connect to the USB bus data signals.
USB Transceiver Bias	RBIAS	35	I-R	A 12.0k , 1.0% resistor is attached from VSSA to this pin in order to set the transceiver's internal bias currents.

Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions (continued)

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
24MHz Crystal or external clock input	XTAL1 (CLKIN)	33	ICLKx	This pin can be connected to one terminal of the crystal or it can be connected to an external 24 clock when a crystal is not used.
24MHz Crystal	XTAL2	32	OCLKx	This is the other terminal of the crystal, or it can be left open when an external clock source is used to drive XTAL1(CLKIN). It may not be used to drive any external circuitry other than the crystal circuit.
3.3V Analog Power	VDDA33	36		3.3V Analog Power
1.8V PLL Power	VDD18PLL	34		This pin is the 1.8V Power for the PLL. +1.8V Filtered analog power for internal PLL. This pin must have a 1.0µF(or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
MISC				
General Purpose I/O	GPIO1 (LED1)	1	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. In addition, as an output, the GPIO1 can use output controlled by the LED1_GPIO1 register.
General Purpose I/O	GPIO2 / RXD / SDA	27	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			I	RXD: In addition to the above, the signal can be used as input to the RXD of UART in the device, when the TXD_RXD_SEL bit in UTIL_CONFIG1 register is cleared to "0".
			I/O12	SDA: This is the data pin when used with an external serial EEPROM.
General Purpose I/O	GPIO4	29	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO7 / TXD / SCK	31	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			O12	TXD: In addition, as an output, the GPIO7 can be used as an output TXD of UART in the device, when the GPIO2/TXD bit in UTL_CONFIG register is set to "1"
			O12	SCK: This is the clock output when used with an external EEPROM.
General Purpose I/O	GPIO10 (CRD_PWR)	21	I/O200	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
				CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.
General Purpose I/O	GPIO14	19	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
RESET Input	nRESET	18	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1µs wide.

Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions (continued)

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
TEST Input	TEST	28	I	This signal is used for testing the chip. User should normally tie this pin low externally if the test function is not used.
No Connects	NC			No Connect. No trace or signal should be routed/attached to these pins.
DIGITAL / POWER				
+1.8V Core power	VDD18	13		All VDD18 pins must be connected together on the circuit board. +1.8V core power. This pin must have a 1.0µF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
3.3V Power & Regulator Input.	VDD33	6 14 22		3.3V Power & Regulator Input.
Ground	VSS	SLUG		Ground Reference

5.2 Buffer Type Descriptions

Table 5.3 USB2244/USB2244i Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
IS	Input with Schmitt trigger.
I/O12	Input/Output buffer with 12mA sink and 12mA source.
I/O200	Input/Output buffer 12mA with FET disabled, 100/200mA source only when the FET is enabled.
I/O12PU	Input/Output buffer with 12mA sink and 12mA source with a pull-up resistor.
O12	Output buffer with 12mA source.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog Input/Output Defined in USB specification.
I-R	RBIAS.

Chapter 6 Pin Reset State Table

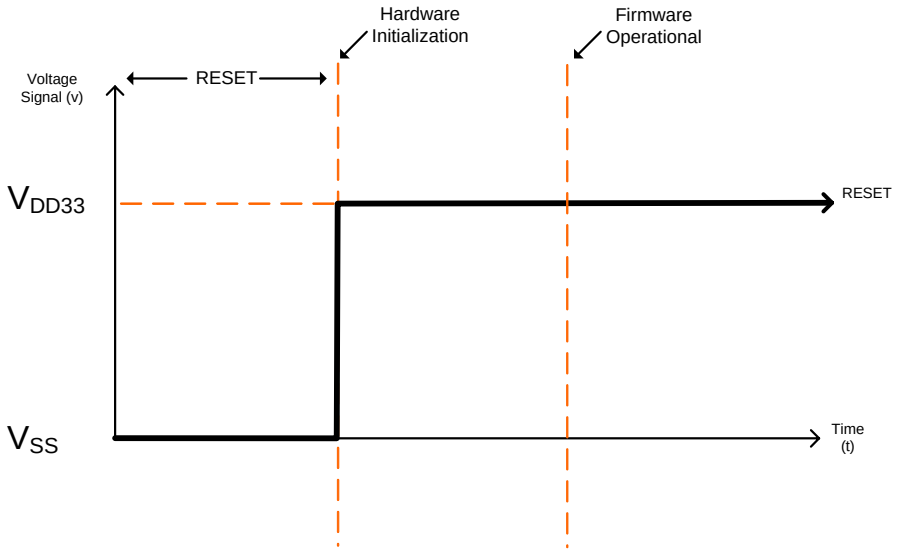


Figure 6.1 Pin Reset States

LEGEND	
yes	hardware enables function
--	hardware disables function
z	hardware disables output driver
pu	hardware enables pullup
pd	hardware enables pulldown
hw	hardware controls function, but state is protocol dependent
(fw)	firmware controls function through registers
VDD	hardware supplies power through pin, applicable only to CARD_PWR pins
none	hardware disables pad

Figure 6.2 Legend for Pin Reset States Table

6.1 36-Pin Reset States

Table 6.1 USB2244/USB2244i Pin Reset States

		RESET STATE				Post-Reset State SD Mode			
PIN	**PIN NAME**	**FUNCTION**	**OUT-PUT**	**PU/PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/PD**	**IN-PUT**
8	SD_D6	none	z	--	--	SD_D6	hw	pu	yes
7	SD_D7	none	z	--	--	SD_D7	hw	pu	yes
5	SD_D0	none	z	--	--	SD_D0	hw	pu	yes
4	SD_D1	none	z	--	--	SD_D1	hw	pu	yes
30	SD_WP	SD_WP	0	--	--	SD_WP	(fw)	(fw)	(fw)
25	SD_D2	none	z	--	--	SD_D2	hw	pu	yes
23	SD_D3	none	z	--	--	SD_D3	hw	pu	yes
20	SD_D4	none	z	--	--	SD_D4	hw	pu	yes
9	SD_CLK	none	z	--	--	SD_CLK	hw	--	yes
10	SD_D5	none	z	--	--	SD_D5	hw	pu	yes
11	SD_CMD	none	z	--	--	SD_CMD	hw	pu	yes
19	GPIO14	GPIO	z	pu	yes				
26	GPIO15 (SD_nCD)	GPIO	z	pu	yes				
24	GPIO12	GPIO	z	pu	yes				
27	GPIO2 / RXD / SDA	GPIO	0	--	--	RXD	z	pu	yes
29	GPIO4	GPIO	0	--	--				
31	GPIO7 / TXD / SCK	GPIO	0	--	--	TXD	hw	--	--
21	GPIO10(CARD_PWR)	GPIO	z	--	--	PWR	VDD	--	--
28	TEST	TEST	z	--	yes				
18	nRESET	nRESET	z	--	yes				
1	GPIO1 (LED1)	GPIO1	0	--	--				
17:15	NC	none	z	--	--	none	z	--	--
12	NC	none	z	--	--	none	z	--	--
2	USB+	USB+	z	--	--				
3	USB-	USB-	z	--	--				
35	RBIAS								
33	XTAL1 (CLKIN)								
32	XTAL2								

Chapter 7 DC Parameters

7.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3V supply voltage + 2) ≤ 6	V	
Voltage on GPIO10		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of this pin is enabled, this pin may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63V and T_A is less than 70^oC.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note 7.1 Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 7.2 When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

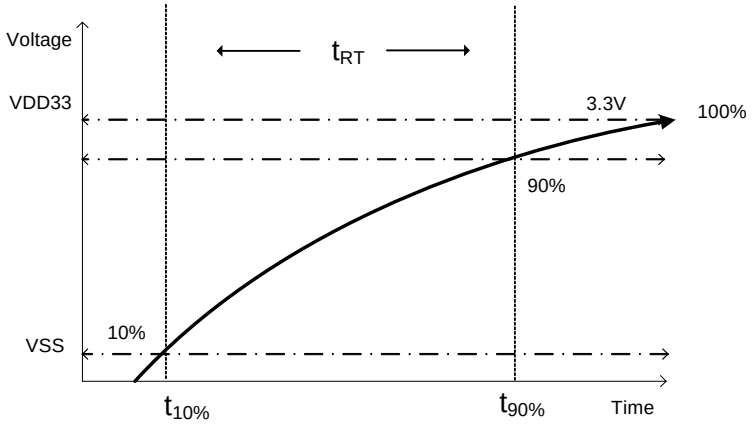


Figure 7.1 Supply Rise Time Model

7.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature					
Commercial Part	T_A	0	70	°C	
Industrial Part	T_A	-40	85	°C	
3.3V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	(Note 7.3)
3.3V supply rise time	t_{RT}	0	400	µs	
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DDA33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Note 7.3 A 3.3V regulator with an output tolerance of 1% must be used if the output of the internal power FET's must support a 5% tolerance.

7.3 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		420		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.4)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 7.5)						
I-R (Note 7.6)						
I/O200 Integrated Power FET for GPIO10						
High Output Current Mode	I_{OUT}	200			mA	$Vdrop_{FET}$ = 0.46V
Low Output Current Mode (Note 7.7)	I_{OUT}	100			mA	$Vdrop_{FET}$ = 0.23V
On Resistance (Note 7.7)	R_{DSON}			2.1	Ω	I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10µF
Supply Current Unconfigured	I_{CCINIT}		80	90	mA	
Supply Current Active Full Speed	I_{CC}		110	140	mA	
High Speed	I_{CC}		135	165	mA	
Supply Current Suspend	I_{CSBY}		350	700	µA	
Industrial Temperature Suspend	I_{CSBYI}		350	900	µA	

Note 7.4 Output leakage is measured with the current pins in high impedance.

Note 7.5 See The USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

Note 7.6 RBIAS is a 3.3V tolerant analog pin.

Note 7.7 Output current range is controlled by program software, software disables FET during short circuit condition.

Note 7.8 The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to

the settings listed in Table 10.1, “USB2244/USB2244i GPIO Usage (ROM Rev 0x00),” on page 22.

Note 7.9 The 3.3V supply should be at least at 75% of its operating condition before the 1.8V supply is allowed to ramp up.

7.4 Capacitance

T_A = 25°C; fc = 1MHz; V_{DD}, V_{DDP} = *1.8V*

Table 7.1 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 8 AC Specifications

8.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz ± 100ppm.

External Clock: 50% Duty cycle ± 10%, 24 MHz ± 100ppm, Jitter < 100ps rms.

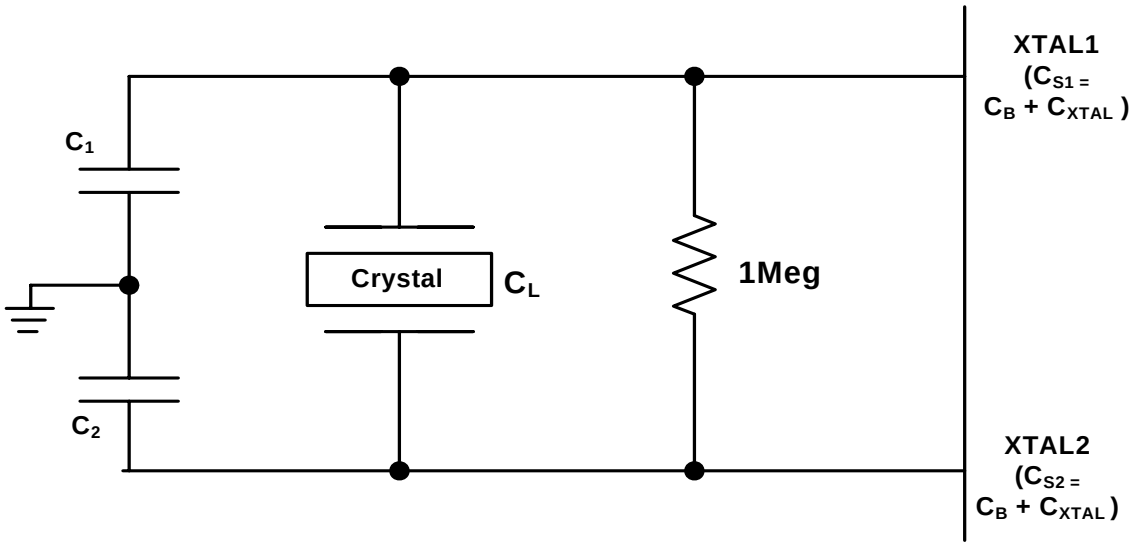


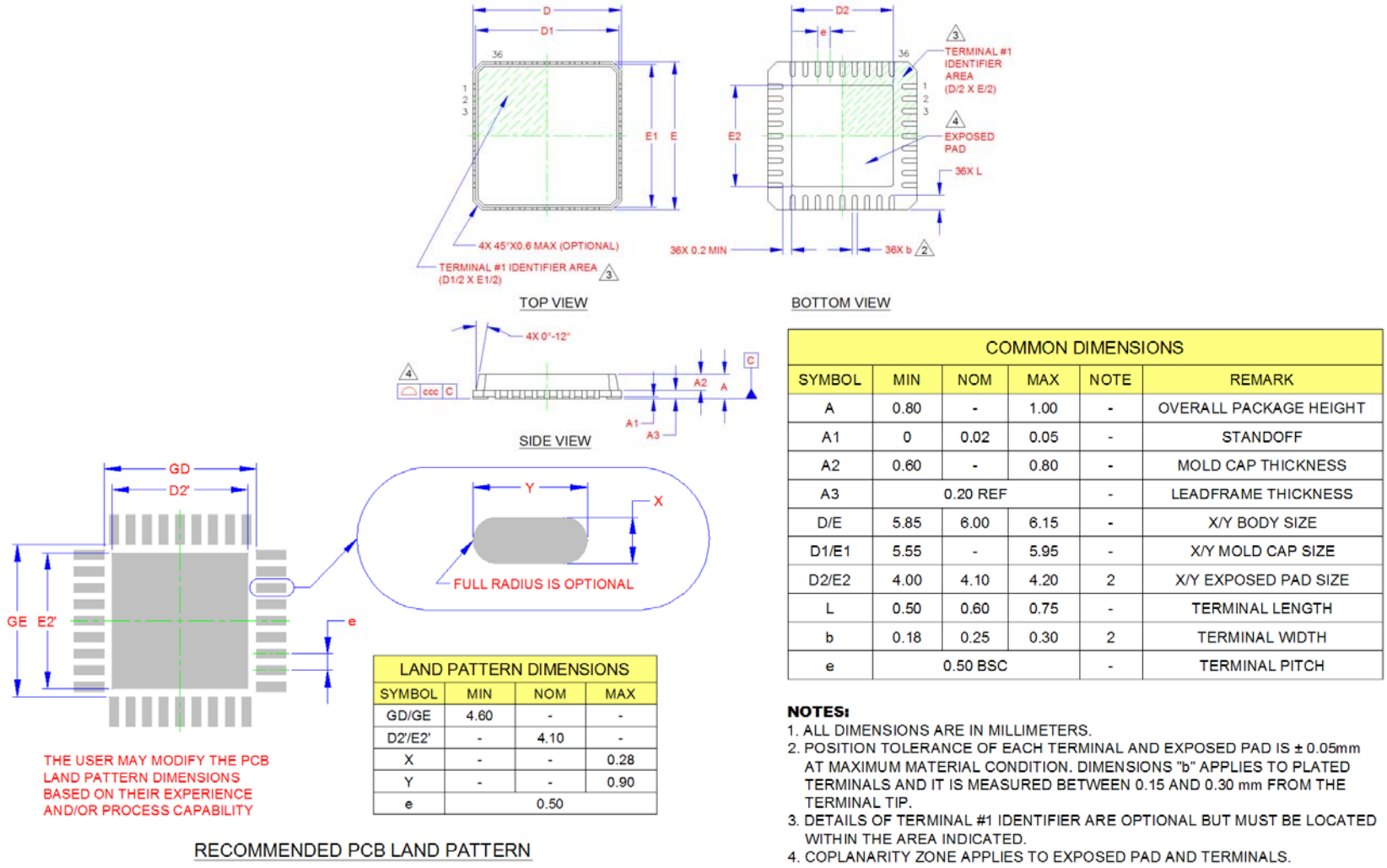
Figure 8.1 Typical Crystal Circuit

Note: C_B equals total board/trace capacitance.

$$\frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})} = C_L$$

Figure 8.2 Formula to Find Value of C_1 and C_2

Chapter 9 Package Outline



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	4.60	-	-
D2'/E2'	-	4.10	-
X	-	-	0.28
Y	-	-	0.90
e		0.50	

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	0.60	-	0.80	-	MOLD CAP THICKNESS
A3		0.20 REF		-	LEADFRAME THICKNESS
D/E	5.85	6.00	6.15	-	X/Y BODY SIZE
D1/E1	5.55	-	5.95	-	X/Y MOLD CAP SIZE
D2/E2	4.00	4.10	4.20	2	X/Y EXPOSED PAD SIZE
L	0.50	0.60	0.75	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e		0.50 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. COPLANARITY ZONE APPLIES TO EXPOSED PAD AND TERMINALS.

Figure 9.1 USB2244/USB2244i 36-QFN, 6x6mm Body, 0.5mm Pitch

Chapter 10 GPIO Usage

Table 10.1 USB2244/USB2244i GPIO Usage (ROM Rev 0x00)

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED1	LED indicator
GPIO2	H	RXD / SDA	Receive Port of Debugger / Serial EEPROM Data
GPIO4	USER	GPIO	User defined
GPIO7	H	TXD / SCK	Transmit Port of Debugger / Serial EEPROM Clock
GPIO10	L	CRD_PWR	Card Power Control
GPIO12	USER	GPIO	User defined
GPIO14	USER	GPIO	User defined
GPIO15	L	SD_nCD	Secure Digital card detect