MC100LVEL33

3.3V ECL ÷4 Divider

The MC100LVEL33 is an integrated ÷4 divider. The LVEL is functionally equivalent to the EL33 and works from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple LVEL33's in a system.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 630 ps Typical Propagation Delay
- 4.0 GHz Typical Maximum Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 130 devices

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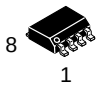
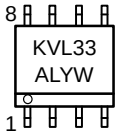
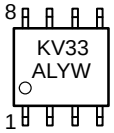
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



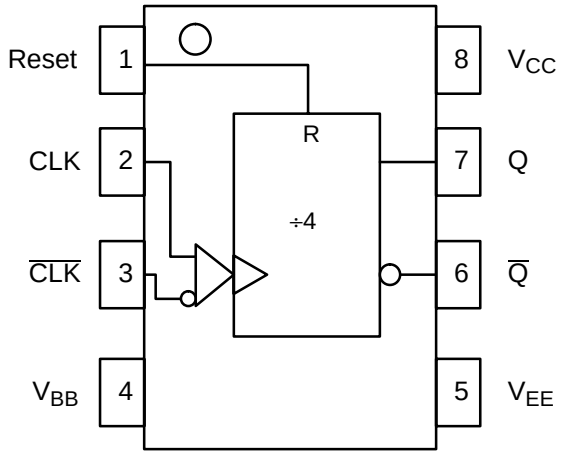
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL33D	SO–8	98 Units / Rail
MC100LVEL33DR2	SO–8	2500 / Reel
MC100LVEL33DT	TSSOP–8	98 Units / Rail
MC100LVEL33DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
Q, $\overline{Q}$	ECL Differential Data ÷4 Outputs
Reset	ECL Asynch Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		33	37		33	37		35	39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.4		 2.9 2.9	 1.1 1.3		 2.9 2.9	 1.1 1.3		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Other $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		33	37		33	37		35	39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.9		 –0.4 –0.4	 –2.2 –2.0		 –0.4 –0.4	 –2.2 –2.0		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Other $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency	3.4			3.8	4.0		3.8			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) Reset to Q	 510 460 500		 690 740 700	 540 490 520	 630	 720 770 720	 600 550 580		 780 830 780	 ps
t_{RR}	Reset Recovery	300			300			300			ps
t_{skew}	Duty Cycle Skew (Note 2.)			20			20			20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	ps

1. V_{EE} can vary ±0.3 V.
2. Duty cycle skew is the difference between T_{PLH} and T_{PHL}.
3. V_{PP} (min) is minimum input swing for which AC parameters are guaranteed.

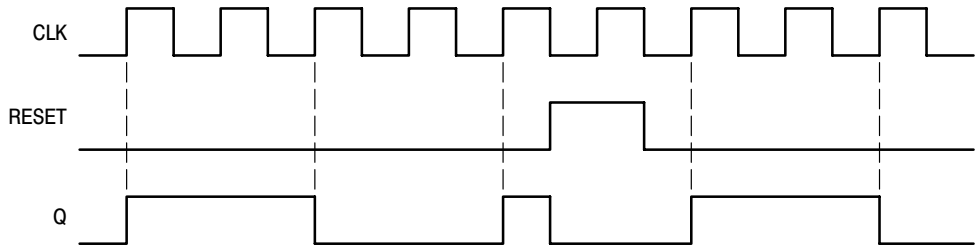


Figure 1. Timing Diagram

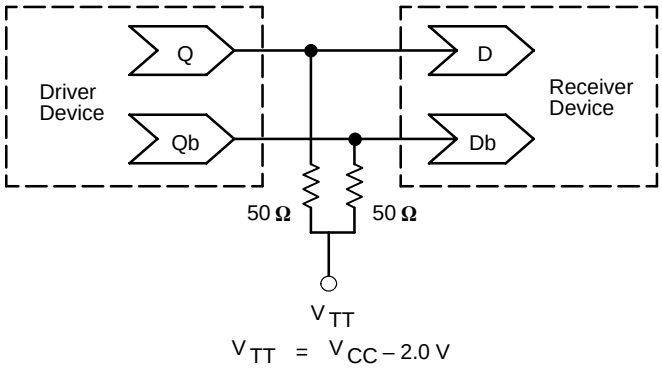


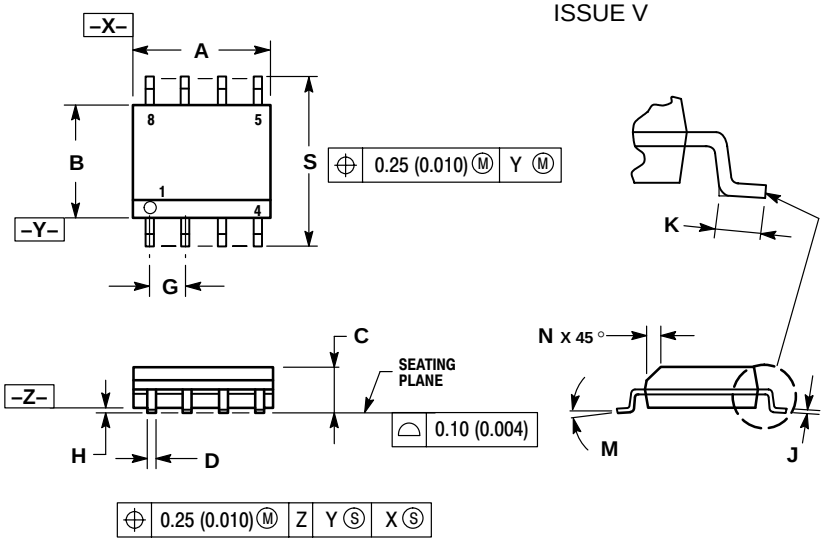
Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE V

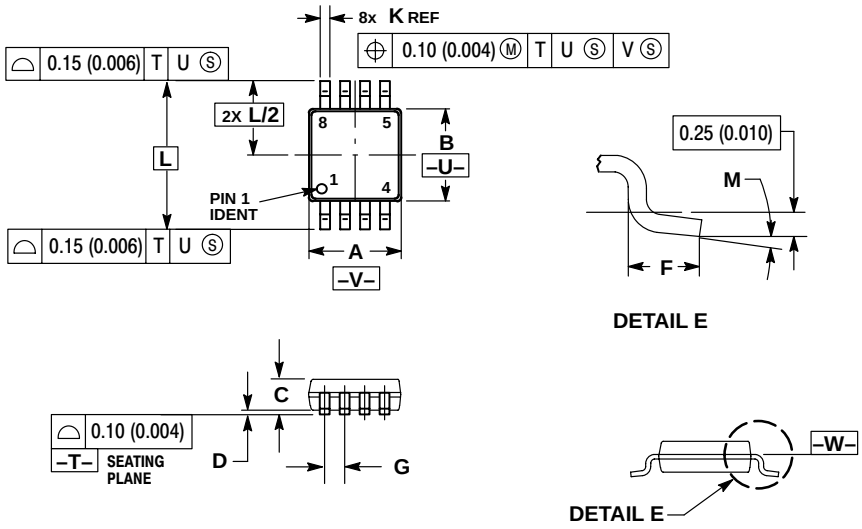


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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