

MC100LVEL31

3.3V ECL D Flip-Flop with Set and Reset

The MC100LVEL31 is a D flip-flop with set and reset. The device is functionally equivalent to the EL31 device but operates from a 3.3 V supply. With propagation delays and output transition times essentially equivalent to the EL31, the LVEL31 is ideally suited for those applications which require the ultimate in AC performance at low power supply voltages.

Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

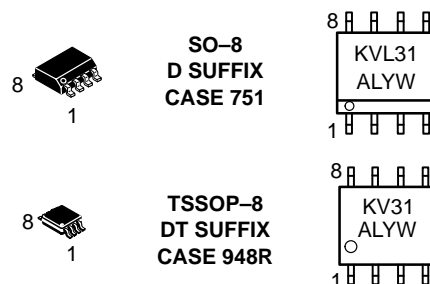
- 475 ps Typical Propagation Delay
- 2.9 GHz Toggle Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V}$ with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -3.0 \text{ V to } -3.8 \text{ V}$
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 121 devices



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MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

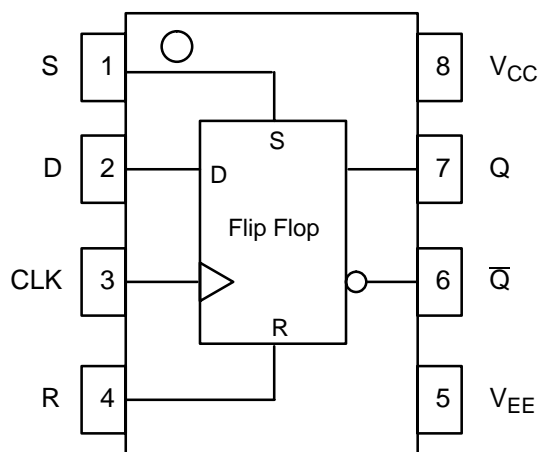
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL31D	SO-8	98 Units / Rail
MC100LVEL31DR2	SO-8	2500 / Reel
MC100LVEL31DT	TSSOP-8	98 Units / Rail
MC100LVEL31DTR2	TSSOP-8	2500 / Reel

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LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	ECL Clock Input
Q, \bar{Q}	ECL Differential Data Outputs
D	ECL Data Input
R	ECL Reset Input
S	ECL Set Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

D	S	R	CLK	Q	\bar{Q}
L	L	L	Z	L	H
H	L	L	Z	H	L
X	H	L	X	H	L
X	L	H	X	L	H
X	H	H	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 \pm 5%	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 \pm 5%	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which device damage may occur.

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LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.

LVNECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$; $V_{EE}=-3.3\text{ V}$ (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.

AC CHARACTERISTICS $V_{CC}=3.3\text{ V}$; $V_{EE}=0.0\text{ V}$ or $V_{CC}=0.0\text{ V}$; $V_{EE}=-3.3\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	2.7			2.9			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	365 385	465 475	580 620	375 395	475 485	590 630	415 435	530 525	630 670	ps
t_S t_H	Setup Time Hold Time	150 250	0 100		150 250	0 100		150 250	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	340 600			340 600			340 600			ps
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	120	220	320	120	220	320	120	220	320	ps

1. V_{EE} can vary $\pm 0.3\text{ V}$.

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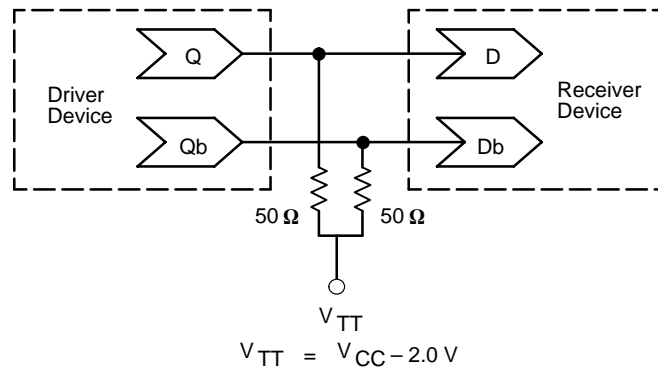


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

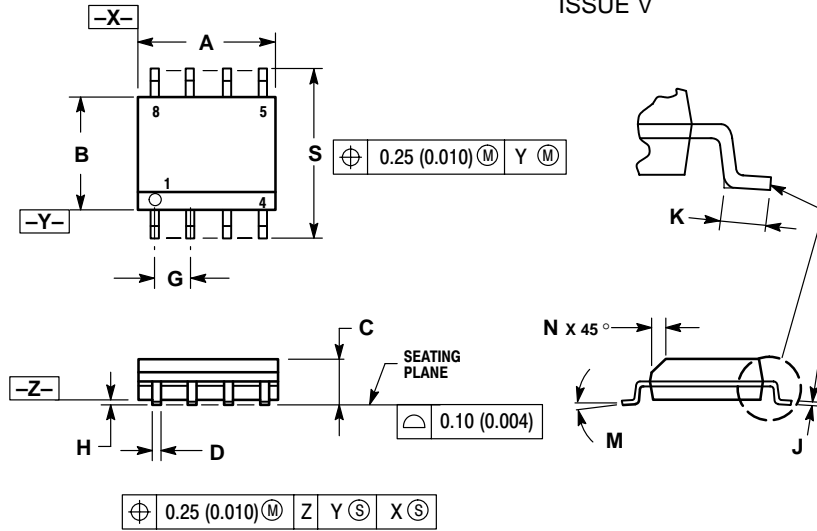
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE V



NOTES:

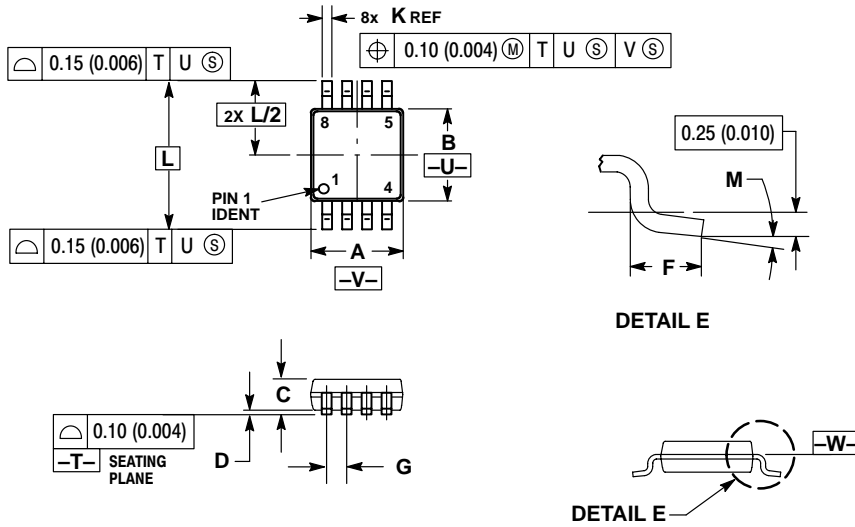
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

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