THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

TSPC603E

PRODUCT SPECIFICATION

PowerPC 603e™ RISC MICROPROCESSOR Family
PID6-603e Specification

DESCRIPTION

The PID6-603e implementation of PC603e (after named 603e) is a low-power implementation of reduced instruction set computer (RISC) microprocessors PowerPC™ family. The 603e implements 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits.

The 603e is a low-power 3.3-volt design and provides four software controllable power-saving modes.

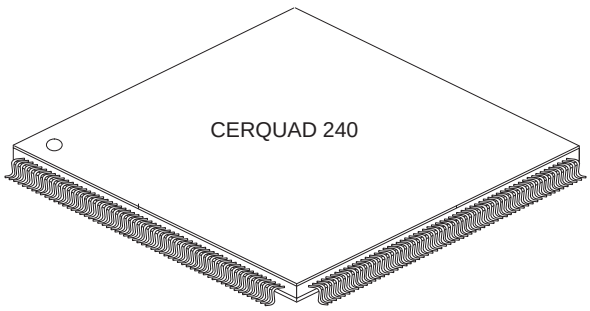
The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance ; however, the 603e makes completion appear sequential. The 603e integrates five execution units and is able to execute five instructions in parallel.

The 603e provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers that provide support for demand-paged virtual memory address translation and variable-sized block translation.

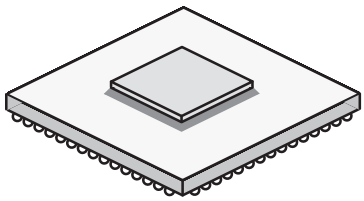
The 603e has a selectable 32 or 64-bit data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to complete for system resources through a central external arbiter. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

The 603e integrates in system testability and debugging features through JTAG boundary-scan capability.



A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier



G suffix
CBGA 255
Ceramic Ball Grid Array

MAIN FEATURES

- 2.4 SPECint95, 2.1 SPECfp95 @ 100 MHz (estimated)
- Superscalar (3 instructions per clock peak).
- Dual 16KB caches.
- Selectable bus clock.
- 32-bit compatibility PowerPC implementation.
- On chip debug support.
- P_D typical = 3.2 Watts (100 MHz), full operating conditions.
- Nap, doze and sleep modes for power savings.
- Branch folding.
- 64-bit data bus (32-bit data bus option).
- 4-Gbyte direct addressing range.
- Pipelined single/double precision float unit. IEEE 754 compatible FPU.
- IEEE P 1149-1 test mode (JTAG/C0P).
- f_{int} max = 100/120/133 MHz.
- f_{bus} max = 66 MHz.
- Compatible CMOS input
  TTL Output.

SCREENING / QUALITY / PACKAGING

This product is manufactured in full compliance with :

- MIL-STD-883 class B or According to TCS standards
- Upscreenings based upon TCS standards
- Full military temperature range (T_c = -55°C, T_c = +125°C)
  Industrial temperature range (T_c = -40°C, T_c = +110°C)
- V_{CC} = 3.3 V ± 5 %.
- 240 pin Cerquad or 255 pin CBGA packages

SUMMARY

A. GENERAL DESCRIPTION

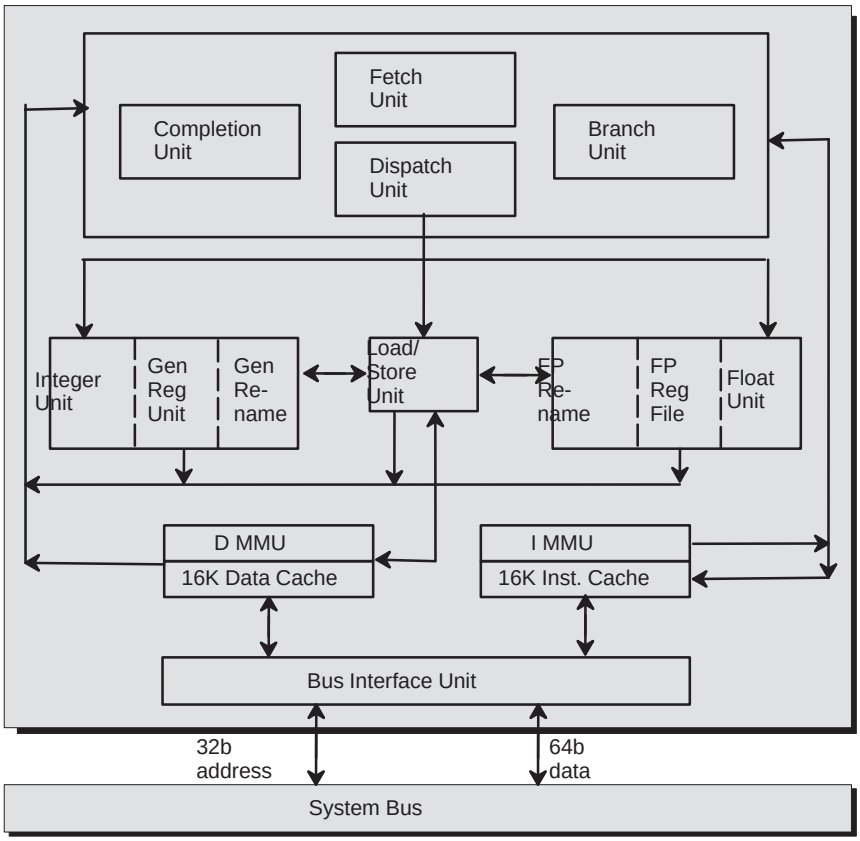


Figure 1 : Block diagram

1. INTRODUCTION

The 603e is a low-power implementation of the PowerPC microprocessor family of reduced instruction set commuter (RISC) microprocessors. The 603e implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603e provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603e to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance ; however, the 603e makes completion appear sequential.

The 603 e integrates five execution units - an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU) and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603e-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603e provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least recently used (LRU) replacement algorithm. The 603e also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The 603e has a selectable 32 - or 64-bit - data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603e provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol as a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 3.3 V CMOS process technology and maintains full interface compatibility with TTL devices.

2. PIN ASSIGNMENTS

2.1. CQFP 240 package

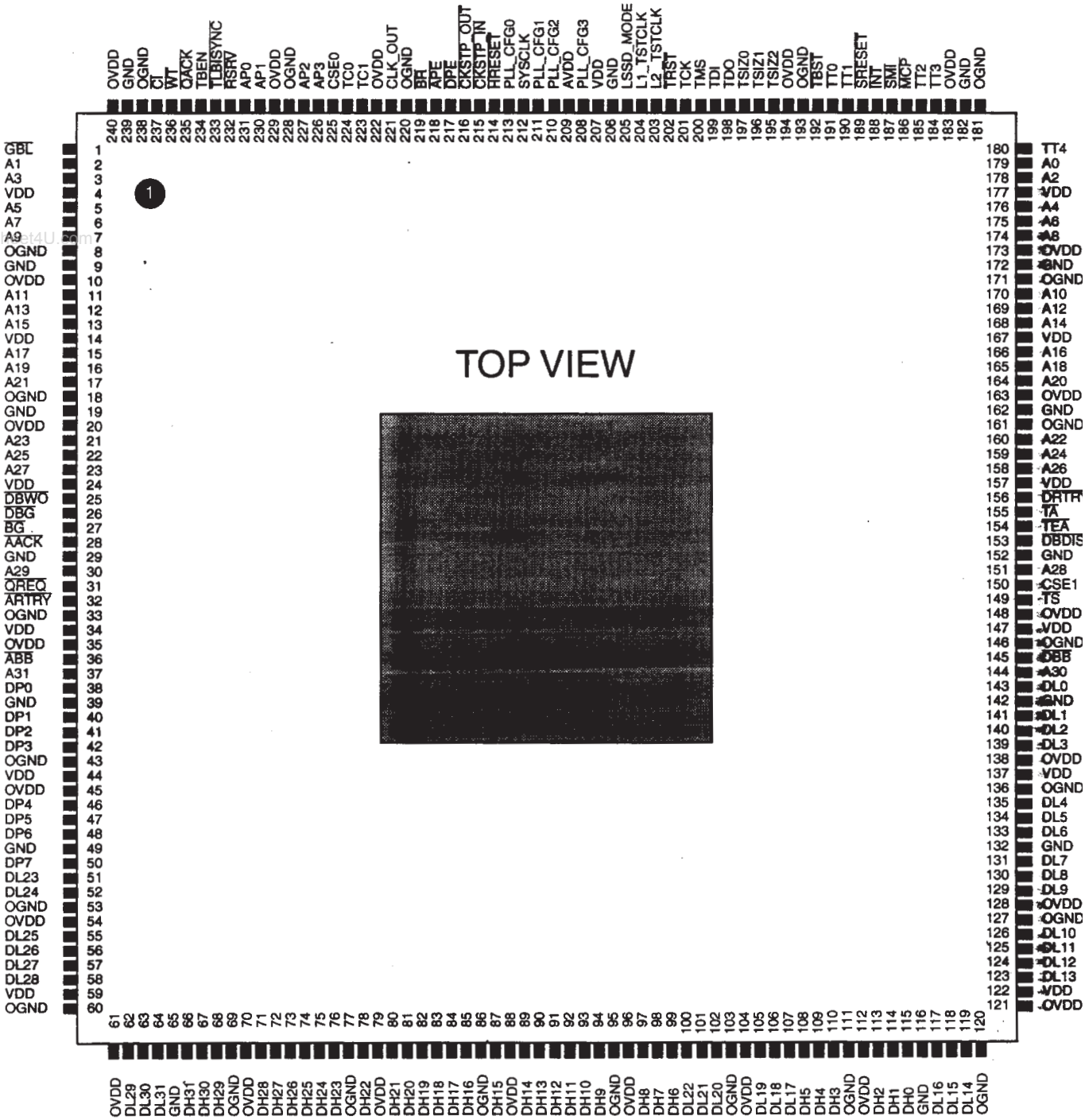


Figure 2 : CQFP 240 : Top view

2.2. CBGA255 package

Figure 3 (pin matrix) shows the pinout as viewed from the top of the CBGA package. The direction of the top surface view is shown by the side profile of the CBGA package.

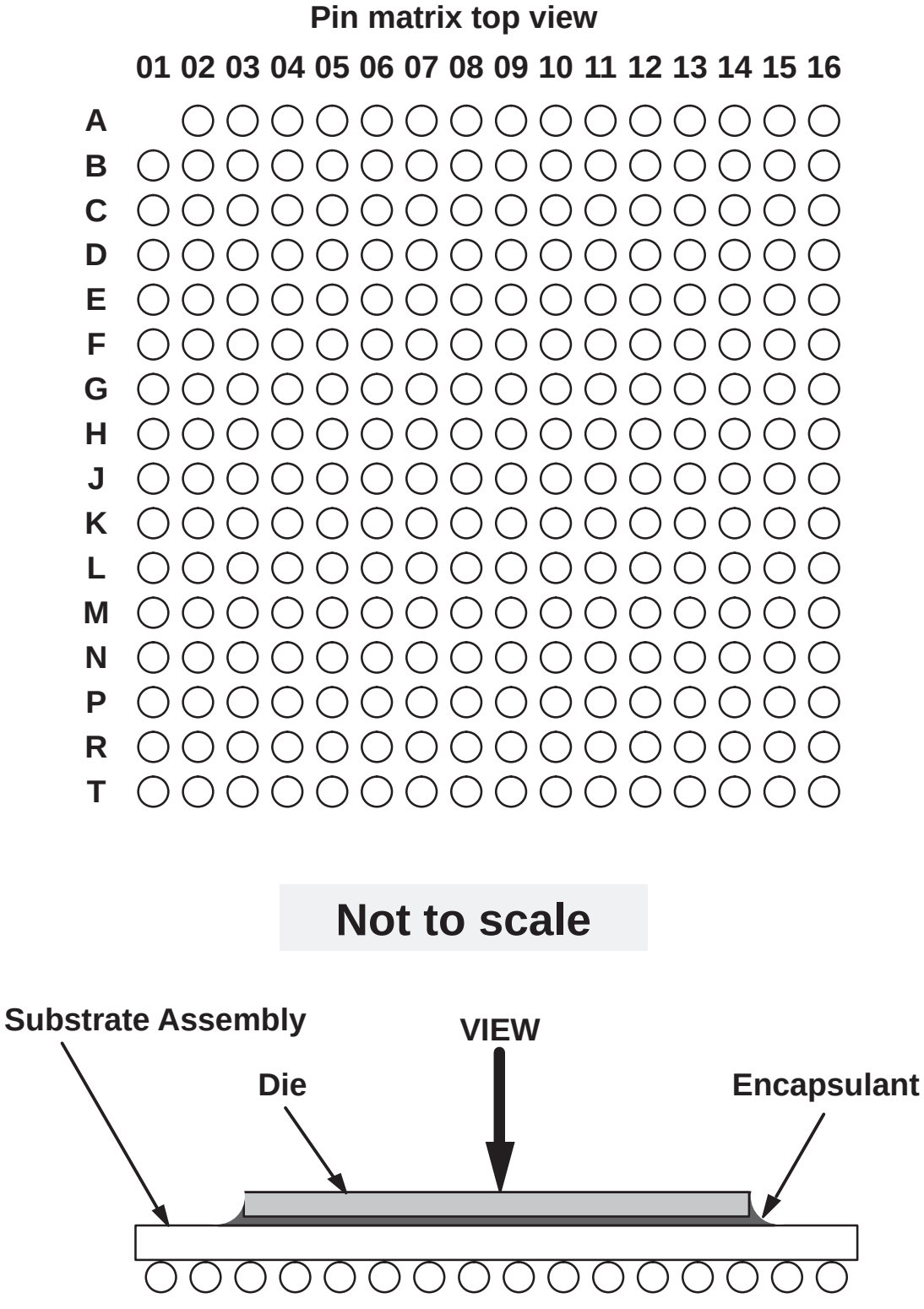


Figure 3 : CBGA 255 Top view

2.3. Pinout listing

Table 1 : Power and ground pins

	CQFP240 package		CBGA255 package	
	VCC	**GND**	**VCC**	**GND**
PLL (AVDD)	209		A10	
Internal logic	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12
Output drivers	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	

Table 2 : Signal pinout listing

Signal name	CQFP Pin number	CBGA Pin number	Active	I/O
A[0–31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, G02, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	28	L02	Low	Input
$\overline{\text{ABB}}$	36	K04	Low	I/O
AP[0–3]	231,230,227,226	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	218	A04	Low	Output
$\overline{\text{ARTRY}}$	32	J04	Low	I/O
$\overline{\text{BG}}$	27	L01	Low	Input
$\overline{\text{BR}}$	219	B06	Low	Output
$\overline{\text{CI}}$	237	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	215	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	216	A06	Low	Output
CLK_OUT	221	D07	-	Output
CSE[0-1]	225,150	B01, B05	High	Output
$\overline{\text{DBB}}$	145	J14	Low	I/O
$\overline{\text{DBG}}$	26	N01	Low	Input
$\overline{\text{DBDIS}}$	153	H15	Low	Input
$\overline{\text{DBWO}}$	25	G04	Low	Input
DH[0-31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0-31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O

Signal name	CQFP Pin number	CBGA Pin number	Active	I/O
DP[0-7]	38, 40, 41, 42, 46, 47, 48, 50	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	217	A05	Low	Output
$\overline{\text{DRTRY}}$	156	G16	Low	Input
$\overline{\text{GBL}}$	1	F01	Low	I/O
$\overline{\text{HRESET}}$	214	A07	Low	Input
$\overline{\text{INT}}$	188	B15	Low	Input
L1_TSTCLK[1]	204	D11	-	Input
L2_TSTCLK[1]	203	D12	-	Input
$\overline{\text{LSSD\_MODE}}$[1]	205	B10	Low	Input
$\overline{\text{MCP}}$	186	C13	Low	Input
PLL_CFG[0-3]	213, 211, 210, 208	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	235	D03	Low	Input
$\overline{\text{QREQ}}$	31	J03	Low	Output
$\overline{\text{RSRV}}$	232	D01	Low	Output
$\overline{\text{SMI}}$	187	A16	Low	Input
$\overline{\text{SRESET}}$	189	B14	Low	Input
SYSCLK	212	C09	-	Input
$\overline{\text{TA}}$	155	H14	Low	Input
TBEN	234	C02	High	Input
$\overline{\text{TBST}}$	192	A14	Low	I/O
TC[0–1]	224, 223	A02, A03	High	Output
TCK	201	C11	-	Input
TDI	199	A11	High	Input
TDO	198	A12	High	Output
$\overline{\text{TEA}}$	154	H13	Low	Input
$\overline{\text{TLBISYNC}}$	233	C04	Low	Input
TMS	200	B11	High	Input
$\overline{\text{TRST}}$	202	C10	Low	Input
$\overline{\text{TS}}$	149	J13	Low	I/O
TSIZ[0-2]	197, 196, 195	A13, D10, B12	High	I/O
TT[0-4]	191, 190, 185, 184, 180	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	236	D02	Low	Output
NC		B07, B08, C03, C06, C08, D05, D06, F03, H04, J16	Low	Input

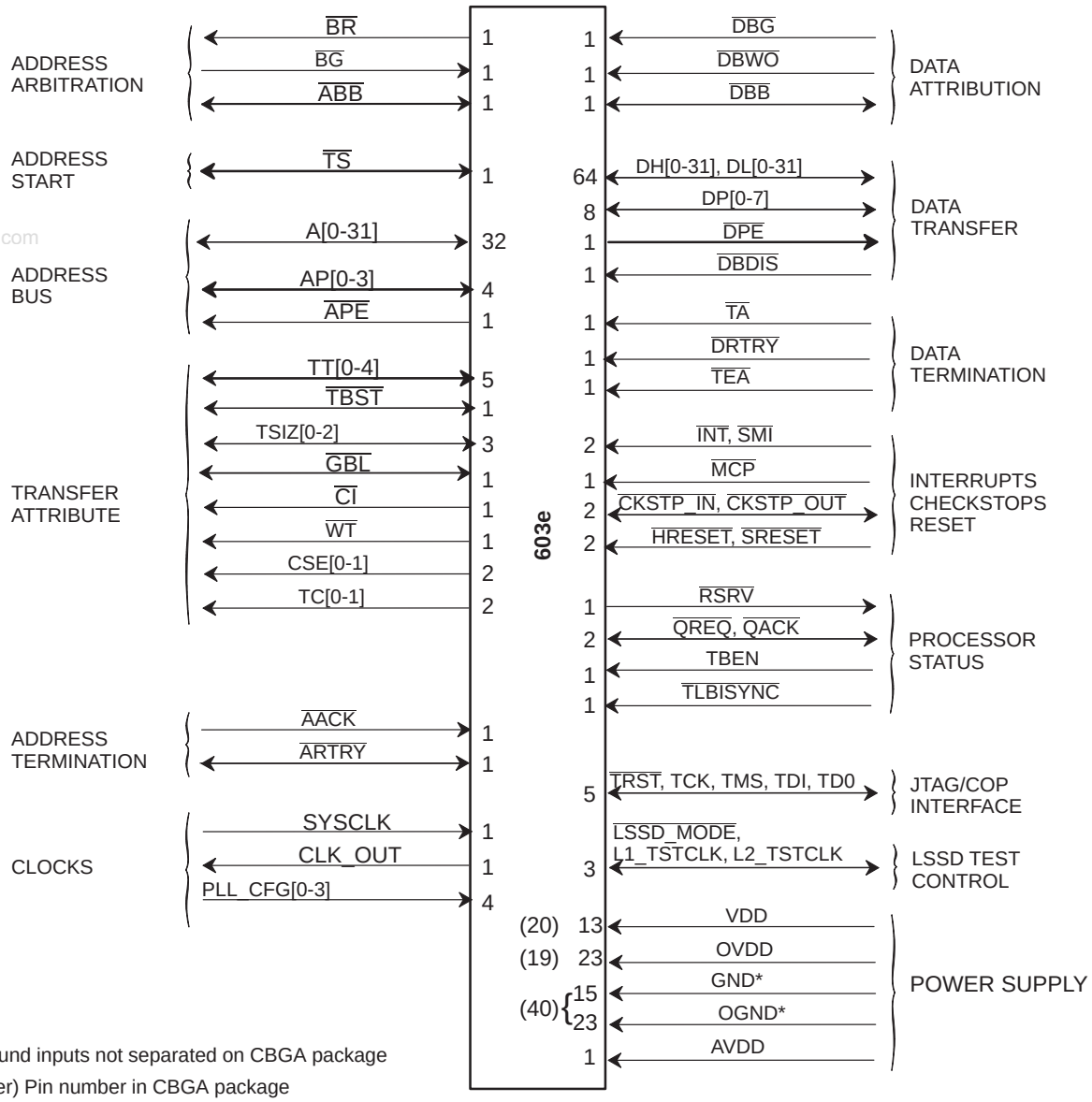
Notes :

1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. OVDD inputs supply power to the I/O drivers and VDD inputs supply power to the processor core. Future members of the 603 family may use different OVDD and VDD input levels.

3. SIGNAL DESCRIPTION

Figure 4, Table 3 and Table 4 describe the signal on the TSPC603e and indicate signal functions. The test signals, TRST, TMS, TCK, TDI and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

The 3 signals LSSD_MODE, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to VDD for normal machine operations.



(*) Ground inputs not separated on CBGA package

(number) Pin number in CBGA package

Figure 4 : Functional signal groups

Table 3 : Address and data bus signal index

Signal name	Mnemonic	Signal function	Signal type
Address bus	A[0-31]	if output, physical address of data to be transferred. if input, represents the physical address of a snoop operation.	I/O
Data bus	DH[0-31]	Represents the state of data, during a data write operation if output, or during a data read operation if input.	I/O
Data bus	DL[0-31]	Represents the state of data, during a data write operation if output, or during a data read operation if input.	I/O

Table 4 : Signal index

Signal name	Mnemonic	Signal function	Signal type
Address Acknowledge	$\overline{\text{AACK}}$	The address phase of a transaction is complete	Input
Address Bus Busy	$\overline{\text{ABB}}$	If output, the 603e is the address bus master If input, the address bus is in use	I/O
Address Bus Parity	AP[0-3]	If output, represents odd parity for each of 4 bytes of the physical address for a transaction If input, represents odd parity for each of 4 bytes of the physical address for snooping operations	I/O
Address Parity Error	$\overline{\text{APE}}$	Incorrect address bus parity detected on a snoop	Output
Address retry	$\overline{\text{ARTRY}}$	If output, detects a condition in which a snooped address tenure must be retried If input, must retry the preceding address tenure	I/O
Bus grant	$\overline{\text{BG}}$	May, with the proper qualification, assume mastership of the address bus	Input
Bus request	$\overline{\text{BR}}$	Request mastership of the address bus	Output
Cache Inhibit	$\overline{\text{CI}}$	A single-beat transfer will not be cached	Output
Test Clock	CLK_OUT	Provides PLL clock output for PLL testing and monitoring	Output
Checkstop Input	$\overline{\text{CKSTP\_IN}}$	Must terminate operation by internally gating off all clocks, and release all outputs	Input
Checkstop Output	$\overline{\text{CKSTP\_OUT}}$	Has detected a checkstop condition and has ceased operation	Output
Cache Set Entry	CSE[0-1]	Cache replacement set element for the current transaction reloading into or writing out of the cache	Output
Data Bus Busy	$\overline{\text{DBB}}$	If output, the 603e is the data bus master If input, another device is bus master	I/O
Data Bus Disable	$\overline{\text{DBDIS}}$	(For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle	Input
Data Bus Grant	$\overline{\text{DBG}}$	May, with the proper qualification, assume mastership of the data bus	Input
Data Bus Write Only	$\overline{\text{DBW0}}$	May run the data bus tenure	Input
Data Bus Parity	DP[0-7]	If output, odd parity for each of 8 bytes of data write transactions If input, odd parity for each byte of read data	I/O
Data Parity Error	$\overline{\text{DPE}}$	Incorrect data bus parity	Output
Data Retry	$\overline{\text{DRTRY}}$	Must invalidate the data from the previous read operation	Input
Global	$\overline{\text{GBL}}$	If output, a transaction is global If input, a transaction must be snooped by the 603e	I/O
Hard Reset	$\overline{\text{HRESET}}$	Initiates a complete hard reset operation	Input
Interrupt	$\overline{\text{INT}}$	Initiates an interrupt if bit EE of MSR register is set	Input
	$\overline{\text{LSSD\_MODE}}$	LSSD test control signal for factory use only	Input
	L1_TSTCLK	LSSD test control signal for factory use only	Input

Signal name	Mnemonic	Signal function	Signal type
	L2_TSTCLK	LSSD test control signal for factory use only	Input
Machine Check Interrupt	$\overline{\text{MCP}}$	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set	Input
PLL Configuration	PLL_CFG[0-3]	Configures the operation of the PLL and the internal processor clock frequency	Input
Quiescent Acknowledge	$\overline{\text{QACK}}$	All bus activity has terminated and the 603e may enter a quiescent (or low power) state	Input
Quiescent Request	$\overline{\text{QREQ}}$	Is requesting all bus activity normally to enter a quiescent (low power) state	Output
Reservation	$\overline{\text{RSRV}}$	Represents the state of the reservation coherency bit in the reservation address register	Output
System Management Interrupt	$\overline{\text{SMI}}$	Initiates a system management interrupt operation if the bit EE of MSR register is set	Input
Soft Reset	$\overline{\text{SRESET}}$	Initiates processing for a reset exception	Input
System Clock	SYSCLK	Represents the primary clock input for the 603e, and the bus clock frequency for 603e bus operation	Input
Transfer Acknowledge	$\overline{\text{TA}}$	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully	Input
Timebase Enable	TBEN	The timebase should continue clocking	Input
Transfer Burst	$\overline{\text{TBST}}$	If output, a burst transfer is in progress If input, when snooping for single-beat reads	I/O
Transfer Code	TC[0-1]	Special encoding for the transfer in progress	Output
Test clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)	Input
Test data input	TDI	Serial data input for the TAP	Input
Test data output	TDO	Serial data output for the TAP	Output
Transfer Error Acknowledge	$\overline{\text{TEA}}$	A bus error occurred	Input
TLBI Sync	$\overline{\text{TLBISYNC}}$	Instruction execution should stop after execution of a **tlbsync** instruction	Input
Test mode select	TMS	Selects the principal operations of the test-support circuitry	Input
Test reset	$\overline{\text{TRST}}$	Provides an asynchronous reset of the TAP controller	Input
Transfer Size	TSIZ[0-2]	For memory accesses, these signals along with $\overline{\text{TBST}}$ indicate the data transfer size for the current bus operation	I/O
Transfer start	$\overline{\text{TS}}$	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{\text{GBL}}$)	I/O
Transfer Type	TT[0-4]	Type of transfer in progress	I/O
Write-Through	$\overline{\text{WT}}$	A single-beat transaction is write-through	Output

B. DETAILED SPECIFICATIONS

1. SCOPE

This drawing describes the specific requirements for the microprocessor TSPC603e, in compliance with MIL-STD-883 class B or TCS standard screening.

2. APPLICABLE DOCUMENTS

1) MIL-STD-883 : Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A : General specifications for microcircuits.

3. REQUIREMENTS

3.1. General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2. Design and construction

3.2.1. Terminal connections

Depending on the package, the terminal connections shall be is shown in Figure 2 and Figure 4 (§ A. GENERAL DESCRIPTION).

3.2.2. Lead material and finish

Lead material and finish shall be as specified in MIL-STD-1835 (see enclosed § 8)

3.2.3. Hermetic Package

The macrocircuits are packaged in 240 pin ceramic quad flat packages (see § 8.1)

The precise case outlines are described at the end of the specification (§ 8.1) and into MIL-STD-1835.

3.3. Absolute maximum ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Table 5 : Absolute maximum rating for the 603e

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	-0.3	4.0	V
P_{LL} supply voltage	AV_{DD}	-0.3	4.0	V
I/O supply voltage	OV_{DD}	-0.3	4.0	V
Input voltage	V_{in}	-0.3	5.5	V
Storage temperature range	T_{stg}	-55	+150	°C

Note 1 : Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

Note 2 : **Caution** : Input voltage must not be greater than the OVDD supply voltage by more than 2.5 V at all times including during power-on reset.

Note 3 : **Caution** : OVDD voltage must not be greater than AVDD supply voltage by more than 2.5 V at all times including during power-on reset.

Note 4 : **Caution** : AVDD voltage must not be greater than OVDD supply voltage by more than 0.4 V at all times including during power-on reset.

3.4. Recommended operating conditions

These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not garanteed.

Parameter	Symbol	Min	Max	Unit
Core supply voltage	V_{DD}	3.135	3.465	V
P_{LL} supply voltage	AV_{DD}	3.135	3.465	V
I/O supply voltage	OV_{DD}	3.135	3.465	V
Input voltage	V_{in}	GND	5.5	V
Operating temperature	T_c	-55	+125	°C

3.5. Thermal characteristics

3.5.1 CQFP240 package

This section provides thermal management data for the 603e ; this information is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, wire-bond CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338.

3.5.1.1. Thermal characteristics

The thermal characteristics for a wire-bond CQFP package are as follows :

Thermal resistance (junction-to-case) (typical)= $R_{\theta jc}$ or θ_{jc} = 2.2°C/Watt.

Wire–bond CQFP die junction–to–lead thermal resistance (typical) = θ_{JB} = 18 °C/W

3.5.1.2. Thermal management example

The following example is based on a typical desktop configuration using a wire-bond CQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the wire-bond CQFP package with thermal grease.

Figure 5 provides a thermal management example for the CQFP package.

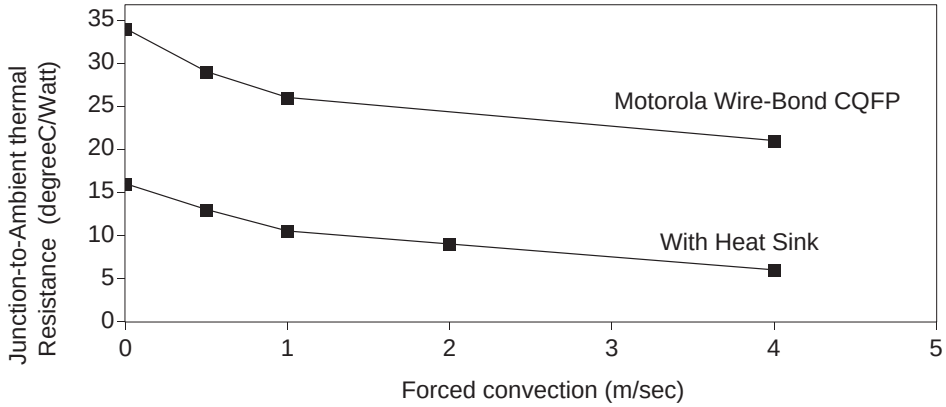


Figure 5 : CQFP thermal management example

The junction temperature can be calculated from the junction to ambient thermal resistance, as follows :

Junction temperature : $T_j = T_a + R_{\theta ja} * P$

or $T_j = T_a + (R_{\theta jc} + R_{cs} + R_{sa}) * P$

Where :

T_a is the ambient temperature in the vicinity of the device

$R_{\theta ja}$ is the junction-to-ambient thermal resistance

$R_{\theta jc}$ is the junction-to-case thermal resistance of the device

R_{cs} is the case-to-heat sink thermal resistance of the interface material

R_{sa} is the heat sink-to-ambient thermal resistance

P is the power dissipated by the device

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the case, from the case to the heat sink, and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

For a power dissipation of 2.5 Watts in an ambient temperature of 40°C at 1 m/sec with the heat sink measured above, the junction temperature of the device would be as follows :

$T_j = T_a + R_{\theta ja} * P$

$T_j = 40°C + (10°C/Watt * 2.5 watts) = 65°C$

which is well within the reliability limits of the device.

Notes :

1. Junction-to-ambient thermal resistance is based on measurements on single-sided printed circuit boards per SEMI (Semiconductor Equipment and Materials International) G38-87 in natural convection.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

3.5.2.CBGA255 package

The data found in this section concerns 603e's packaged in the 255-lead 21 mm multi-layer ceramic (MLC), ceramic BGA package. Data is shown for two cases, the expoded-die case (no heat sink) and using the Thermalloy 2338-pin fin heat sink.

3.5.2.1. Thermal characteristics

The internal thermal resistance for this package is negligible due to the exposed die design. A heat sink is attached directly to the silicon die surface only when external thermal enhancement is necessary.

Additionally, the CBGA package offers an excellent thermal connection to the card and power planes. Heat generated at the chip is dissipated through the package, the heat sink (when used) and the card. The parallel heat flow paths result in the lowest overall thermal resistance as well as offer significantly better power dissipation capability when a heat sink is not used.

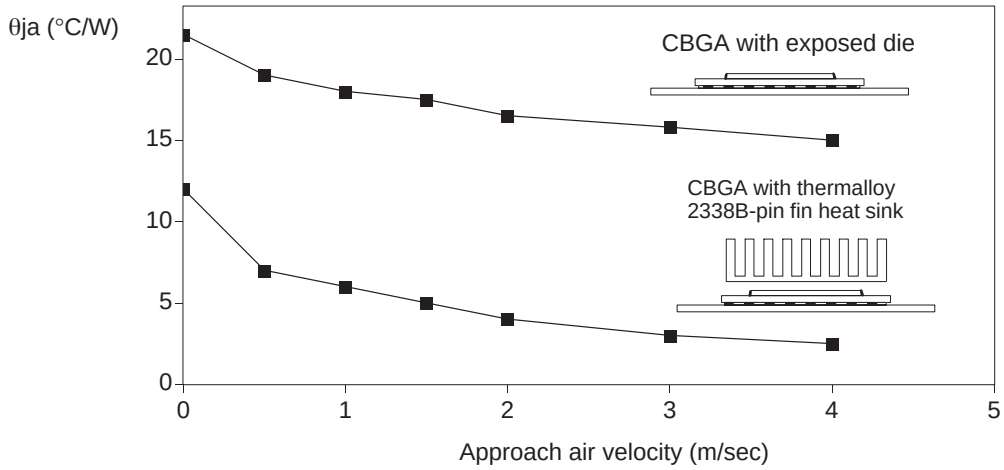
The thermal characteristics for the flip–chip CBGA package are as follows :

Thermal resistance (junction-to-case) = $R_{\theta jc}$ or θ_{jc} = 0.08°C/Watt.

Thermal resistance (junction-to-ball) = $R_{\theta jb}$ or θ_{jb} = 2.8°C/Watt .

3.5.2.2. Thermal management example

The calculations are performed exactly as shown in the previous section for CPFP240. Figure 6 shows typical thermal performance data for the 21 mm CBGA package mounted to a test card.



Assumptions :

1. 2P card with 1 OZ Cu planes
2. 63 mm x 76 mm card
3. Air flow on both sides of card
4. Vertical orientation
5. 2-stage epoxy heat sink attach

Figure 6 : CBGA thermal management example

Temperature calculations are also performed identically to those in the previous section. For a power dissipation of 2.5 Watts in an ambient of 40°C at 1.0 m/sec, the associated overall thermal resistance and junction temperature, found in Table 6 will result.

Table 6 : Thermal resistance and junction temperature

Configuration	θ_{ja} (°C/W)	T_j (°C)
Exposed die (no heat sink)	18.4	86
With 2338 heat sink	5.3	53

Vendors such as Aavid Engineering Inc., Thermalloy, and Wakefield Engineering can supply heat sinks with a wide range of thermal performance.

3.6. Power consideration

The PowerPC603e microprocessor is the first microprocessor specifically designed for low-power operation. The 603e provides both automatic and program-controllable power reduction modes for progressive reduction of power consumption. This chapter describes the hardware support provided by the 603e for power management.

3.6.1. Dynamic Power Management

Dynamic power management automatically powers up and down the individual execution units of the 603e, based upon the contents of the instruction stream. For example, if no floating-point instructions are being executed, the floating-point unit is automatically powered down. Power is not actually removed from the execution unit ; instead, each execution unit has an independent clock input, which is automatically controlled on a clock-by- clock basis. Since CMOS circuits consume negligible power when they are not switching, stopping the clock to an execution unit effectively eliminates its power consumption. The operation of DPM is completely transparent to software or any external hardware. Dynamic power management is enabled by setting bit 11 in HID0 on power-up, of following $\overline{\text{HRESET}}$.

3.6.2. Programmable Power Modes

The 603e provides four programmable power states - full power, doze, nap and sleep. Software selects these modes by setting one (and only one) of the three power saving mode bits. Hardware can enable a power management state through external asynchronous interrupts The hardware interrupt causes the transfer of program flow to interrupt handler code. The appropriate mode is then set by the software. The 603e provides a separate interrupt and interrupt vector for power management - the system management interrupt (SMI). The 603e also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the decrementer interrupt (DI). Note that the 603e cannot switch from on power management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping ; therefore, a hardware handshake is provided to ensure coherency before the 603e enters these power management modes. Table 7 summarizes the four power states.

Table 7 : Power PC 603e Microprocessor Programmable Power Modes

PM Mode	Functioning Units	Activation Method	Full-Power Wake Up Method
Full power	All units active	–	–
Full power (with DPM)	Requested logic by demand	By instruction dispatch	–
Doze	- Bus snooping - Data cache as needed - Decrementer timer	Controlled by SW	External asynchronous exceptions* Decrementer interrupt Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous exceptions Decrementer interrupt Reset
Sleep	None	Controlled by hardware and software	External asynchronous exceptions Reset

* Exceptions are referred to as interrupts in the architecture specification

3.6.3. Power Management Modes

The following sections describe the characteristics of the 603e's power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603e while the power management modes are active.

3.6.3.1. Full-Power Mode with DPM Disabled

Full-power mode with DPM disabled power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared.

- Default state following power-up and $\overline{\text{HRESET}}$.
- All functional units are operating at full processor speed at all times.

3.6.3.2. Full-Power Mode with DPM Enabled

Full-power mode with DPM enabled (HID0[11] = 1) provides on-chip power management without affecting the functionality or performance of the 603e.

- Required functional units are operating at full processor speed.
- Functional units are clocked only when needed.
- No software or hardware intervention required after mode is set.
- Software/hardware and performance transparent.

3.6.3.3. Doze Mode

Doze ode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603e to enable the data cache, copy the data back to memory, disable the cache, and fully return to the doze state.

- Most functional units disabled.
- Bus snooping and time base/decrementer still enabled.
- Dose mode sequence :
  - Set doze bit (HID0[8) = 1).
  - 603e enters doze mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts.
  - Assert hard reset or soft reset.
- Transition to full-power state takes no more than a few processor cycles.
- PLL running and locked to SYSCLK.

3.6.3.4. Nap Mode

The nap mode disables the 603e but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603e to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep mode, a hardware handshake using the quiesce request ($\overline{\text{QREQ}}$) and quiesce acknowledge ($\overline{\text{QACK}}$) signals are requires to maintain data coherency. The 603e will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603e will enter the sleep or nap mode.

- Time base/decrementer still enabled.
- Most functional units disabled (including bus snooping).
- All nonessential input receivers disables.
- Nap mode sequence :
  - Set nap bit (HID0[9] = 1).
  - 603e asserts quiesce request ($\overline{\text{QREQ}}$) signal.
  - System asserts quiesce acknowledge ($\overline{\text{QACK}}$) signal.
  - 603e enters sleep mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{\text{INT}}$, $\overline{\text{SPI}}$, $\overline{\text{MCP}}$ or decrementer interrupts.
  - Assert hard reset or soft reset.
- Transition to full-power takes no more than a few processor cycles.
- PLL running and locked to SYSCLK.

3.6.3.5. Sleep Mode

Sleep mode consumes the least amount of power of the four modes since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Due to the fully static design of the 603e, internal processor state is preserved when no internal clock is present. Because the time base and decrementer are disabled while the 603e is in sleep mode, the 603e's time base contents will have to be updated from an external time base following sleep mode if accurate time-of-day maintenance is required. Before the 603e enters the sleep mode, the 603e will assert the $\overline{\text{QREQ}}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{\text{QACK}}$ and the 603e will enter the sleep mode.

- All functional units disabled (including bus snooping and time base).
- All nonessential input receivers disabled :
  - Internal clock regenerators disabled.
  - PLL still running (see below).

- Sleep mode sequence :
  - Set sleep bit (HID0[10] = 1).
  - 603e asserts quiesce request ($\overline{QREQ}$).
  - System asserts quiesce acknowledge ($\overline{QACK}$).
  - 603e enters sleep mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{INT}$, $\overline{SMI}$, or $\overline{MCP}$ interrupts.
  - Assert hard reset or soft reset.
- PLL may be disabled and SYSCLK may be removed while in sleep mode.
- Return to full-power mode after PLL and SYSCLK disabled in sleep mode :
  - Enable SYSCLK.
  - Reconfigure PLL into desired processor clock mode.
  - System logic waits for PLL startup and relock time (100 µsec).
  - System logic asserts one of the sleep recovery signals (for example, INT or SMI).

3.6.4. Power Management Software Considerations

Since the 603e is a dual issue processor with out -of-order execution capability, care must be taken in how the power management mode is entered. Furthermore, nap and sleep modes require all outstanding bus operations to be completed before the power management mode is entered. Normally during system configuration time, one of the power management modes would be selected by setting the appropriate HID0 mode bit. Later on, the power management mode is invoked by setting the MSR[POW] bit. To provide a clean transition into and out of the power management mode, the **stmsr**[POW] should be preceded by a **sync** instruction and followed by an **isync** instruction.

3.6.5. Power dissipation

Table 8 : Power dissipation

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, 0°C ≤ T_c ≤ 125°C

CPU clock Frequency

	80 MHz	**100 MHz**	**120 MHz**	**133 MHz**	**Units**
Full-On Mode (DPM Enabled)					
Typical	2.1	3.2	3.9	4.2	W
Max	3.0	4.0	4.8	5.3	W
Doze Mode[1]					
Typical	0.8	1.0	1.2	1.3	W
Nap Mode[1]					
Typical	70	70	80	85	mW
Sleep Mode[1]					
Typical	40	40	45	50	mW
Sleep Mode-PLL Disabled[1]					
Typical	5.0	5.0	6.0	6.0	mW
Sleep Mode-PLL and SYSCLK Disabled[1]					
Typical	3.0	3.0	3.0	3.0	mW

Note 1 : The values provided for this mode do not include pad driver power (OVDD) or analog supply power (AVDD). Worst-case AVDD = 15 mW

Note : To calculate the power consumption at low temperature (–55°C), use a 1.25 factor
Maximum power measurements are performed with a worst case instruction mix at VDD=3.465V

3.7. Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo,
- Manufacturer's part number,
- Class B identification if applicable,
- Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4. ELECTRICAL CHARACTERISTICS

4.1. General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 9 : Static electrical characteristics for the electrical variants.
- Table 10 : Dynamic electrical characteristics for the 603e.

These specifications are for 80 MHz and 100 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0_PLL_CFG3 signals. All timings are specified respective to the rise edge of SYSCLK.

4.2. Static characteristics

Table 9 : Electrical characteristics

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_c ≤ 125°C

Characteristics		Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)		V_{IH}	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)		V_{IL}	GND	0.8	V
SYSCLK input high voltage		CV_{IH}	2.4	5.5	V
SYSCLK input low voltage		CV_{IL}	GND	0.4	V
Input leakage current	V_{in} = 3.465 V(1)	I_{in}	-	10	µA
	V_{in} = 5.5 V1	I_{in}	-	245	µA
Hi-Z (off-state) leakage current	V_{in} = 3.465 V(1)	I_{TSI}	-	10	µA
	V_{in} = 5.5 V(1)	I_{TSI}	-	245	µA
Output high voltage	I_{OH} = –9 mA	V_{OH}	2.4	-	V
Output low voltage	I_{OL} = 14 mA	V_{OL}	-	0.4	V
Capacitance, V_{in} = 0 V, f = 1 MHz(2) (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{in}	-	10.0	pF
Capacitance, V_{in} = 0 V, f = 1 MHz(2) (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{in}	-	15.0	pF

Notes : 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).
2. Capacitance is periodically sampled rather than 100 % tested.

4.3. Dynamic characteristics

4.3.1. Clock AC specifications

Table 10 provides the clock AC timing specifications as defined in Figure 7.

Table 10 : Clock AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_c ≤ 125°C

Num	Characteristics	80 MHz		100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
	Processor frequency	80	80	80	100	80	120	80	133.3	Mhz	5
	VCO frequency	160	160	160	200	160	240	160	266.6	Mhz	5
	SYSCLK (bus) frequency	20	66.67	20	66.67	20	66.67	20	66.67	Mhz	
1	SYSCLK cycle time	15	60	15	60	15	60	15	60	ns	
2,3	SYSCLK rise and fall time	–	2.0	–	2.0	–	2.0	–	2.0	ns	1
4	SYSCLK duty cycle (1.4V measured)	40	60	40	60	40	60	40	60	%	3
	SYSCLK jitter	–	±150	–	±150	–	±150	–	±150	ps	2
	603e internal PLL relock time	–	100	–	100	–	100	–	100	us	3,4

Notes:

1. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
2. Cycle-to-cycle jitter, is guaranteed by design.
3. Timing is guaranteed by design and characterization, and is not tested.
4. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG0–PLL_CFG3 signal description in Section 1.8, "System Design Information," for valid PLL_CFG0–PLL_CFG3 settings, and to Section 1.9, "Ordering Information," for available frequencies and part numbers.

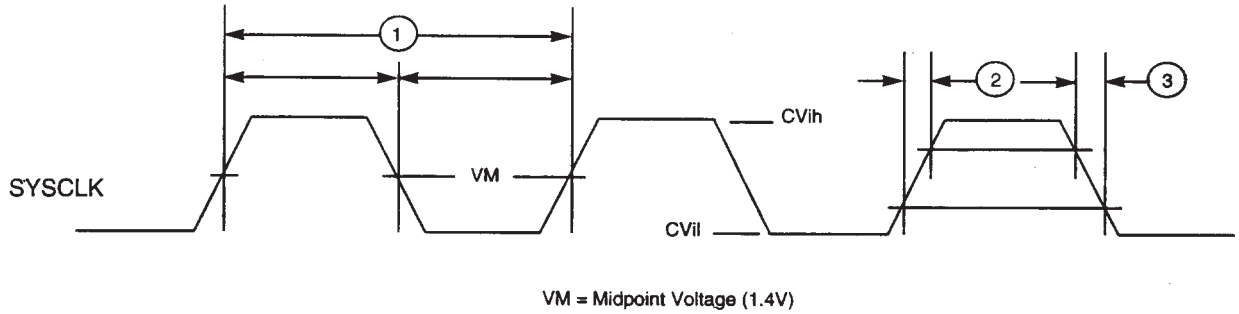


Figure 7 : SYSCLK input timing diagram

4.3.2. Input AC specifications

Table 11 provides the input AC timing specifications for the 603e as defined in Figure 8 and Figure 9.

Table 11 : Input AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_c ≤ 125°C

Num	Characteristics	80 MHz		100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	4.0	-	4.0	-	4.0	-	4.0	-	ns	2
10b	All other inputs valid to SYSCLK (input setup)	5.0	-	5.0	-	5.0	-	5.0	-	ns	3
10c	Mode select inputs valid to HRESET (input setup) (for DRTRY, QACK and TLBISYNC)	8* t_{sys}	-	8* t_{sys}	-	8* t_{sys}	-	8* t_{sys}	-	ns	4,5,6, 7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	-	1.0	-	1.0	-	1.0	-	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	-	1.0	-	1.0	-	1.0	-	ns	3
11c	HRESET to mode select inputs invalid (input hold) (for DRTRY, QACK, and TLBISYNC)	0	-	0	-	0	-	0	-	ns	4, 6, 7

Notes: 1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 2.

2. Address/data/transfer attribute input signals are composed of the following: A0–A31, AP0–AP3, TT0–TT4, TC0-TC1, TBST, TSIZ0–TSIZ2, GBL, DH0–DH31, DL0–DL31, DP0–DP7.

3. All other input signals are composed of the following: TS, ABB, DBB, ARTRY, BG, AACK, DBG, DBWO, TA, DRTRY, TEA, DBDIS,HRESET, SRESET, INT, SMI, MCP, TBEN, QACK, TLBISYNC.

4. The setup and hold time is with respect to the rising edge of HRESET. See Figure 9

5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.

6. These values are guaranteed by design, and are not tested.

7. This specification is for configuration mode only. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.

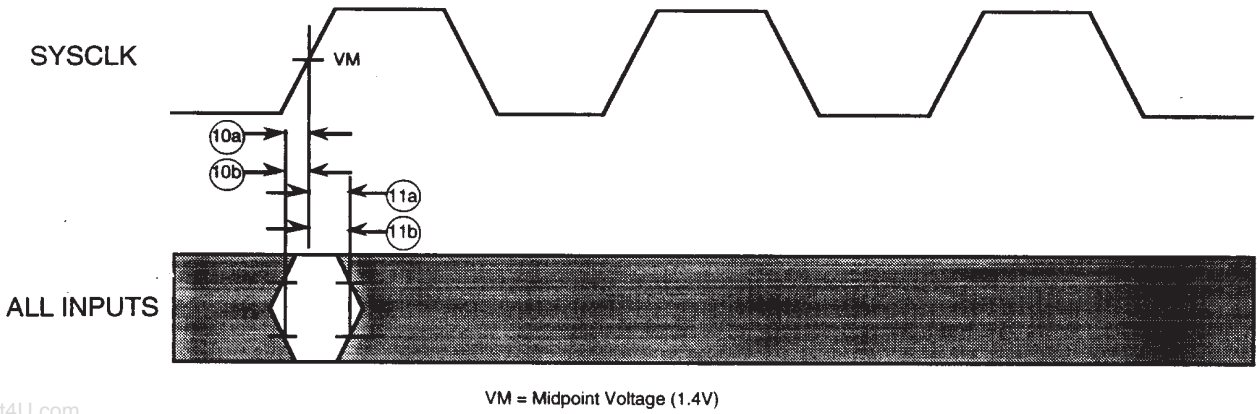


Figure 8 : Input timing diagram

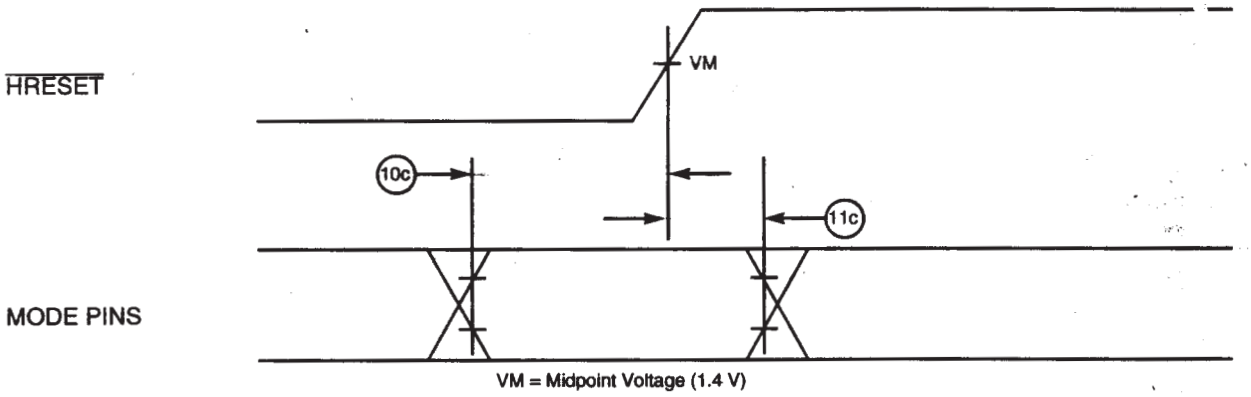


Figure 9 : Mode select input timing diagram

4.3.3. Output AC specifications

Table 12 provides the output AC timing specifications for the 603e (shown in Figure 10).

Table 12 : Output AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, C_L = 50 pF, –55°C ≤ T_c ≤ 125°C

Num	Characteristic	80 MHz		100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	–	1.0	–	1.0	–	1.0	–	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	11.0	–	11.0	–	11.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	10.0	–	10.0	–	10.0	–	10.0	ns	6
14a	SYSCLK to output valid (5.5 V to 0.8 V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	13.0	–	13.0	–	13.0	–	13.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	11.0	–	11.0	–	11.0	ns	6
15	SYSCLK to output invalid (output hold)	0.5	–	0.5	–	0.5	–	0.5	–	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	9.5	–	9.5	–	9.5	–	9.5	ns	

Num	Characteristic	80 MHz		100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1.2	–	1.2	–	1.2	–	1.2	t_{sys}	5, 7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	9.0	–	9.0	–	9.0	–	9.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * t_{sys} + 1.0	–	0.2 * t_{sys} + 1.0	–	0.2 * t_{sys} + 1.0	–	0.2 * t_{sys} + 1.0	–	ns	3, 5, 8
20	Maximum dalay to $\overline{ARTRY}$ precharge	–	1.2	–	1.2	–	1.2	–	1.2	t_{sys}	5, 8
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2.25	–	2.25	–	2.25	–	2.25	t_{sys}	5, 8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin. See.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).
5. t_{sys} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.

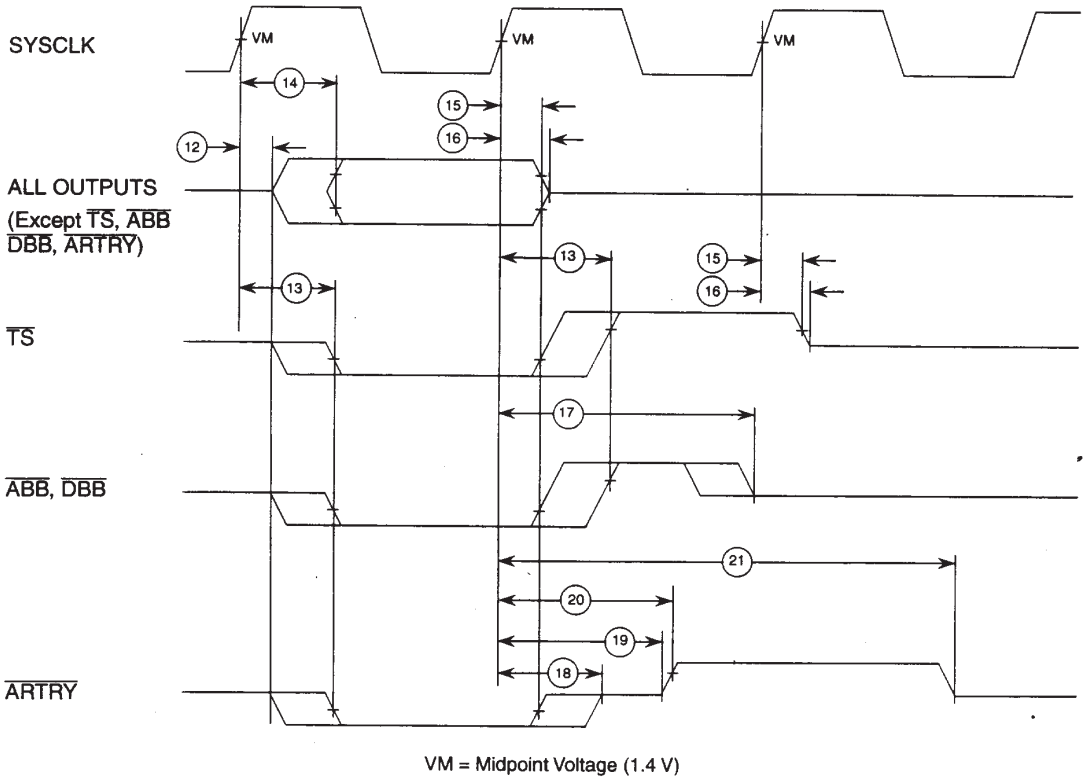


Figure 10 : Output timing diagram

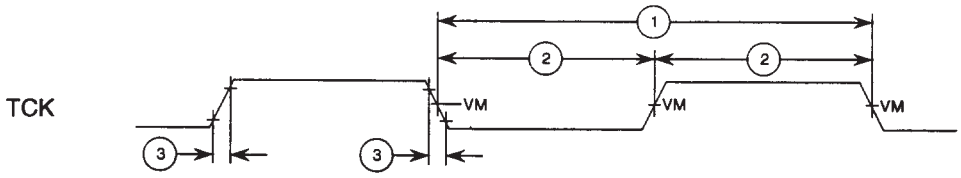
4.4. JTAG AC timing specifications

Table 13 : JTAG AC timing specifications (independent of SYSCLK)

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, C_L = 50 pF, –55°C ≤ T_C ≤ 125°C

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{TRST}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{TRST}$ assert time	40	—	ns	
6	Boundary scan input data setup time	6	—	ns	2
7	Boundary scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes: 1. $\overline{TRST}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.



VM = Midpoint Voltage (1.4 V)

Figure 11 : Clock input timing diagram

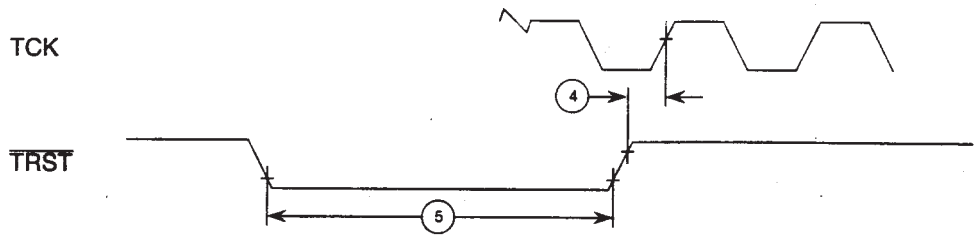


Figure 12 : $\overline{TRST}$ timing diagram

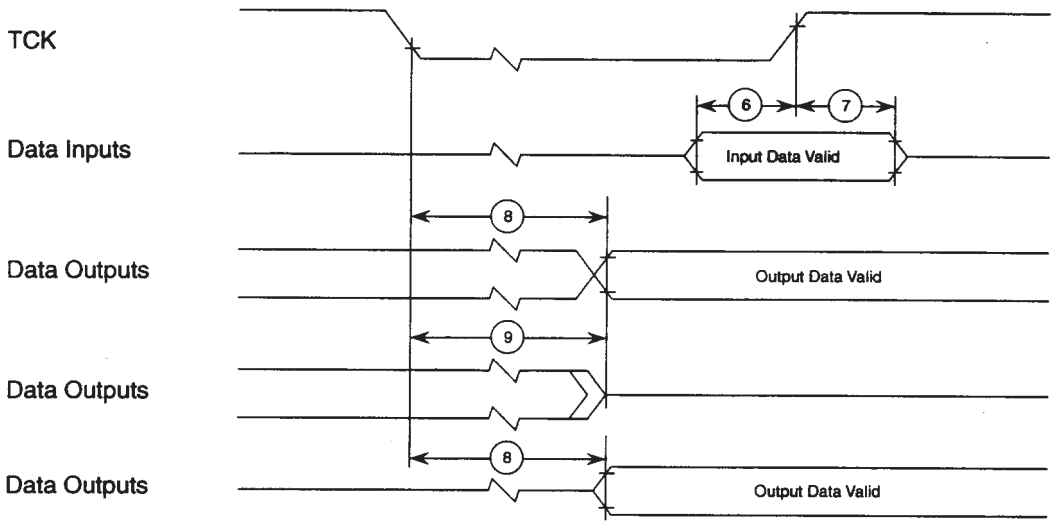


Figure 13 : Boundary-scan timing diagram

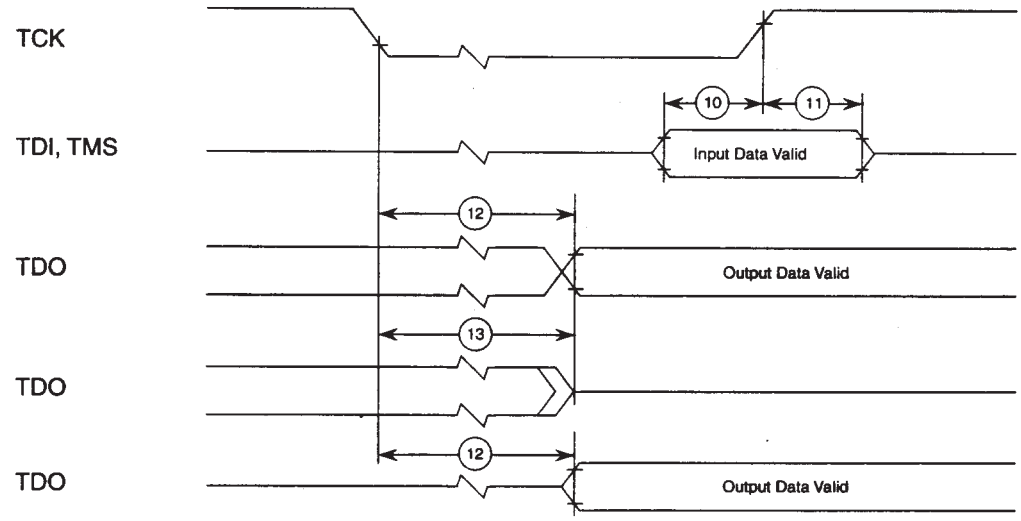


Figure 14 : Test access port timing diagram

5. FUNCTIONAL DESCRIPTION

5.1. PowerPC registers and programming model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege - supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, special-purpose registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of hardware implementation (HID) registers.

Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating-system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603e.

5.1.1. General-Purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, general-purpose registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors and 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

5.1.2. Floating-Point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit floating-point registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single - or double - precision floating-point formats.

5.1.3. Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

5.1.4. Floating-Point Status and Control Register (FPSCR)

The floating-point status and control register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

5.1.5. Machine State Register (MSR)

The machine state register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling completes. The 603e implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

5.1.6. Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit segment registers (SRs). To speed access, the 603e implements the segment registers as two arrays ; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (stsr) instruction loads both arrays.

5.1.7. Special-Purpose Registers (SPRs)

The powerPC operating environment architecture defines numerous special-purpose registers that serve a variety of functions, such as providing controls, indicating status, configuring the processor, and performing special operations. During normal execution, a program can access the registers, shown in Figure 15, depending on the program's access privilege (supervisor or user, determined by the privilege-level (PR) bit in the MSR). Note that register such as the GPRs and FPRs are accessed through operands that are part of the instructions. Access to registers can be explicit (that is, through the use of specific instructions for that purpose such as Move to Special-Purpose Register (mtspr) and Move from Special-Purpose Register (mfspr) instructions) or implicit, as the part of the execution of an instruction. Some registers are accessed both explicitly and implicitly.

Il the 603e, all SPRs are 32 bits wide.

5.1.7.1. User-Level SPRs

The following 603e SPRs are accessible by user-level software :

- Link register (LR) - The link register can be used to provide the branch target address and to hold the return address after branch and link instructions. The LR is 32 bits wide in 32-bit implementations.
- Count register (CTR) - The CRT is decremented and tested automatically as a result of branch-and-count instructions. The CTR is 32 bits wide in 32-bit implementations.
- Integer exception register (XER) - The 32-bit XER contains the summary overflow bit, integer carry bit, overflow bit, and a field specifying the number of bytes to be transferred by a Load String Word Indexed (lswx) or Store String Word Indexed (stswx) instruction.

5.1.7.2. Supervisor-Level SPRs

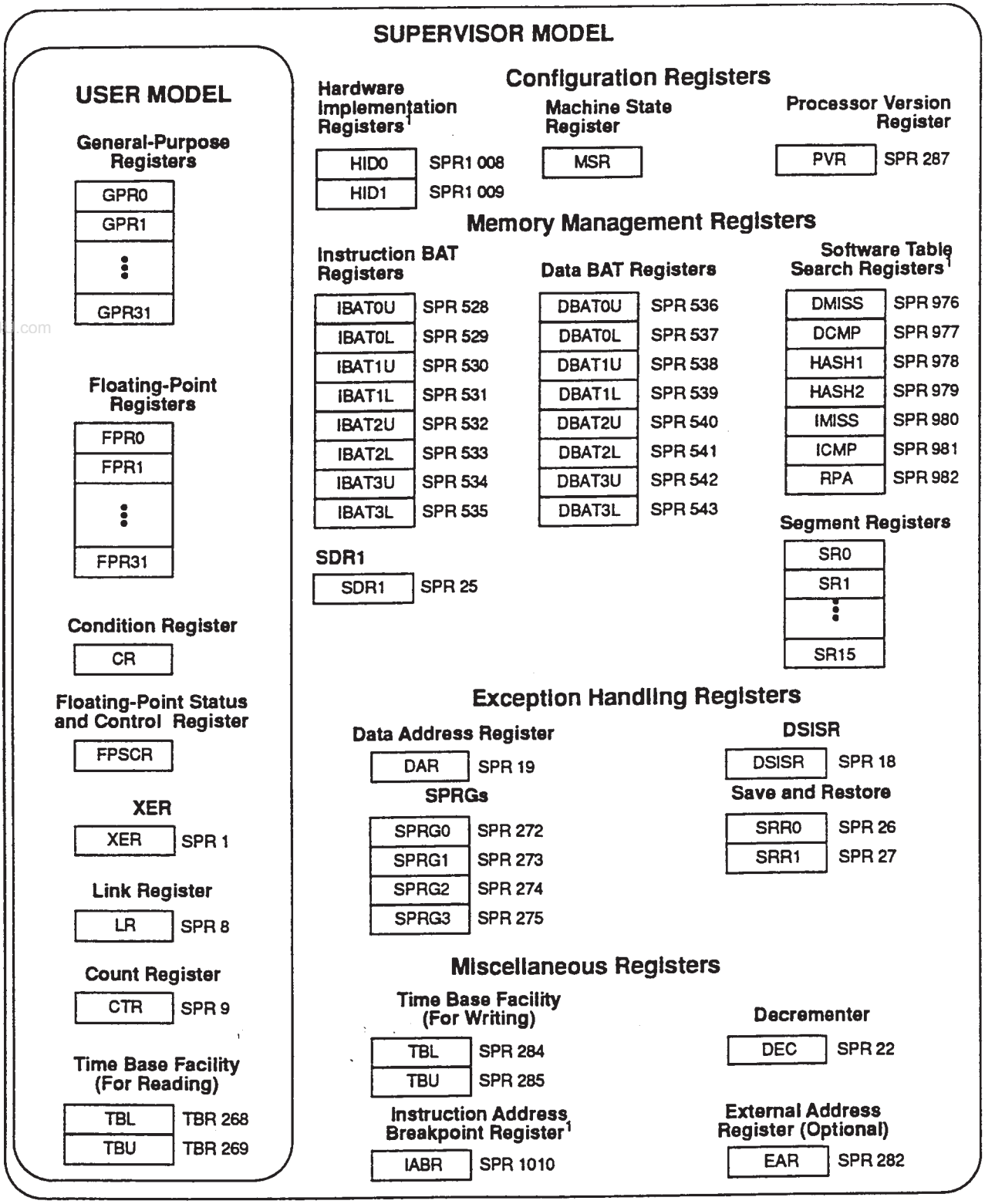
The 603e also contains SPRs that can be accessed only by supervisor-level software. These registers consist of the following :

- The 32-bit DSISR defines the cause of data access and alignment exceptions.
- The data address register (DAR) is a 32-bit register that holds the address of an access after an alignment or DSI exception.
- Decrementer register (DEC) is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.
- The 32-bit SDR1 specifies the page table format used in virtual-to-physical address translation for pages. (Note that physical address is referred to as real address in the architecture specification).
- The machine status save/restore register 0 (SRR0) is a 32-bit register that is used by the 603e for saving the address of the instruction that caused the exception, and the address to return to when a Return from Interrupt (**rfi**) instruction is executed.
- The machine status save/restore register 1 (SRR1) is a 32-bit register used to save machine status on exceptions and to restore machine status when an **rfi** instruction is executed.
- The 32-bit SPRG0-SPRG3 registers are provided for operating system use.
- The external access register (EAR) is a 32-bit register that controls access to the external control facility through the External Control In Word Indexed (**eciwx**) and External Control Out Word Indexed (**ecowx**) instructions.
- The time base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - time base upper (TBU) and time base lower (TBL).
- The processor version register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.
- Block address translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 15 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603e :

- The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.
- The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary page table entry groups (PTEGs).
- The ICMP and DCMP registers contain a duplicate of the first word in the page table entry (PTE) for which the table search is looking.
- The required physical address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.
- The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603e”s checkstops and features, and allows software to read the configuration of the PLL configuration signals.
- The instruction address breakpoint register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 15 shows all the 603e registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.



[1] These registers are 603e–specific registers. They may not be supported by other PowerPC processors.

Figure 15 : PowerPC microprocessor programming model - Register

5.2. Instruction set and addressing modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

5.2.1. PowerPC instruction set and addressing modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

5.2.1.1. PowerPC instruction set

The PowerPC instructions are divided into the following categories :

- **Integer instructions** - These include computational and logical instructions.
  - Integer arithmetic instructions.
  - Integer compare instructions.
  - Integer logical instructions.
  - Integer rotate and shift instructions.

- **Floating-point instructions** -These include floating-point computational instructions, as well as instructions that affect the FPSCR.
  - Floating-point arithmetic instructions.
  - Floating-point multiply/add instructions.
  - Floating-point rounding and conversion instructions.
  - Floating-point compare instructions.
  - Floating-point status and control instructions.
- **Load/store instructions** - These include integer and floating-point load and store instructions.
  - Integer load and store instruction.
  - Integer load and store multiple instructions.
  - Floating-point load and store.
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx.** instructions).
- **Flow control instructions** - These include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow.
  - Branch and trap instructions.
  - Condition register logical instructions.
- **Processor control instructions** - These instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers.
  - Move to/from SPR instructions.
  - Move to/from MSR.
  - Synchronize.
  - Instruction synchronize.
- **Memory control instruction** - These instructions provide control of caches, TLBs, and segment registers.
  - Supervisor-level cache management instructions.
  - User-level cache instructions.
  - Segment register manipulation instructions.
  - Translation lookaside buffer management instructions.

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between memory and a set of 32 floating-point registers (FPRs).

Computational instructions do not modify memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

5.2.1.2. Calculating effective addresses

The effective address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

The PowerPC architecture supports two simple memory addressing modes :

- EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index).
- EA = (RA|0) + rB (register indirect with index).

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry from bit 0 is ignored in 32-bit implementations.

5.2.2. PowerPC 603e microprocessor instruction set

The 603e instruction set is defined as follows :

- The 603e provides hardware support for all 32-bit PowerPC instructions.
- The 603e provides two implementation-specific instructions used for software table search operations following TLB misses :
  - Load Data TLB Entry (**tlbld**).
  - Load Instruction TLB Entry (**tlbli**).
- The 603e implements the following instructions which are defined as optional by the PowerPC architecture :
  - External Control In Word Indexed (**eciwx**).
  - External Control Out Word Indexed (**ecowx**).
  - Floating Select (**fsed**).
  - Floating Reciprocal Estimate Single-Precision (**fres**).
  - Floating Reciprocal Square Root Estimate (**frsqrte**).
  - Store Floating-Point as Integer Word (**stfiwx**).

5.3. Cache implementation

The following subsections describe the PowerPC architecture's treatment of cache in general, and the 603e specific implementation, respectively.

5.3.1. PowerPC cache characteristics

The PowerPC architecture does not define hardware aspects of cache implementations. For example, some PowerPC processors, including the 603e, have separate instruction and data caches (hardware architecture), while others, such as the PowerPC 601™ microprocessor, implement a unified cache.

PowerPC microprocessor control the following memory access modes on a page or block basis :

- Write-back/write-through mode.
- Cache-inhibited mode.
- Memory coherency.

Note that in the 603e, a cache line is defined as eight words. The VEA defines cache management instructions that provide a means by which the application programmer can affect the cache contents.

5.3.2. PowerPC 603e microprocessor cache implementation

The 603e has two 16-Kbyte, four-way set-associative (instruction and data) caches. The caches are physically addressed, and the data cache can operate in either write-back or write-through mode as specified by the PowerPC architecture.

The data cache is configured as 128 sets of 4 lines each. Each line consists of 32 bytes, two state bits, and an address tag. The two state bits implement the three-state MEI (modified/exclusive/invalid) protocol. Each line contains eight 32-bit words. Note that the PowerPC architecture defines the term block as the cacheable unit. For the 603e, the block size is equivalent to a cache line. A block diagram of the data cache organization is shown in Figure 16.

The instruction cache also consists of 128 sets of 4 lines, and each line consists of 32 bytes, an address tag, and a valid bit. The instruction cache may not be written to except through a line fill operation. The instruction cache is not snooped, and cache coherency must be maintained by software. A fast hardware invalidation capability is provided to support cache maintenance. The organization of the instruction cache is very similar to the data cache shown in Figure 16.

Each cache line contains eight contiguous words from memory that are loaded from an 8-word boundary (that is, bits A27-A32 of the effective addresses are zero) ; thus, a cache line never crosses a page boundary. Misaligned accesses across a page boundary can incur a performance penalty.

The 603's cache lines are loaded in four beats of 64 bits each. The burst load is performed as "critical double word first". The cache that is being loaded is blocked to internal accesses until the load completes. The critical double word is simultaneously written to the cache and forwarded to the requesting unit, thus minimizing stalls due to load delays.

To ensure coherency among caches in a multiprocessor (or multiple caching-device) implementation, the 603e implements the MEI protocol. These three states, modified, exclusive, and invalid, indicate the state of the cache block as follows :

- **Modified** - The cache line is modified with respect to system memory ; that is, data for this address is valid only in the cache and not in system memory.
- **Exclusive** - This cache line holds valid data that is identical to the data at this address in system memory. No other cache has this data.
- **Invalid** - This cache line does not hold valid data.

Cache coherency is enforced by on-chip bus snooping logic. Since the 603e's data cache tags are single ported, a simultaneous load or store and snoop access represent a resource contention. The snoop access is given first access to the tags. The load or store then occurs on the clock following snoop.

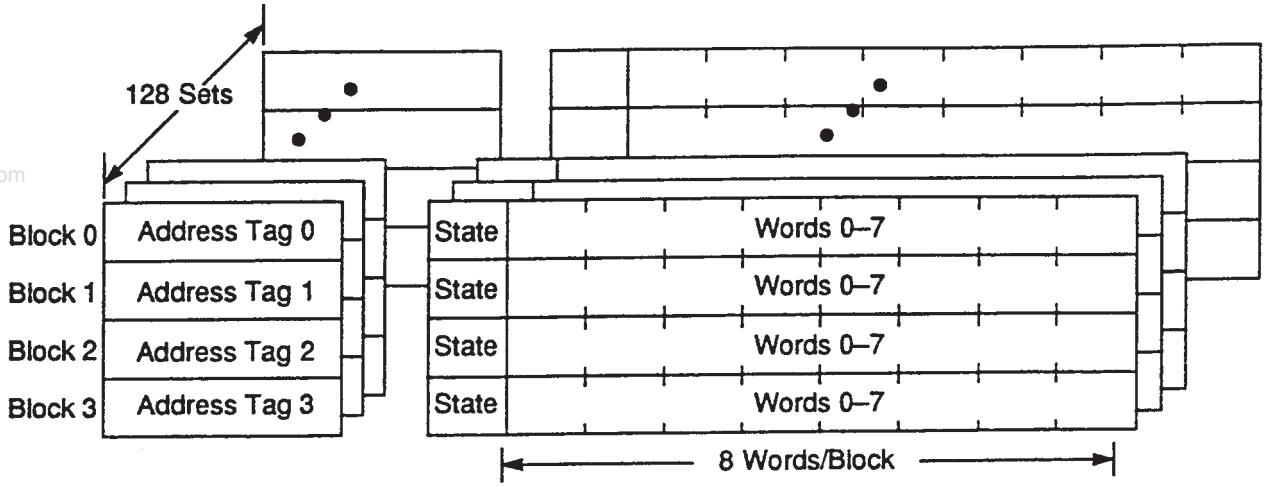


Figure 16 : Data cache organization

5.4. Exception model

The following subsections describe the PowerPC exception model and the 603e implementation, respectively.

5.4.1. PowerPC exception model

The PowerPC exception mechanism allows the processor to change to supervisor state as a result of external singles, errors, or unusual conditions arising in the execution of instructions, and differ from the arithmetic exceptions defined by the IEEE for floating-point operations. When exceptions occur, information about the state of the processor is saved to certain registers and the processor begins execution at an address (exception vector) predetermined for each exception. Processing of exceptions occurs in supervisor mode.

Although multiple exception conditions can map to a single exception vector, a more specific condition may be determined by examining a register associated with the exception - for example, the DSISR and the FPSCR. Additionally, some exception conditions can be explicitly enable or disabled by software.

The PowerPC architecture requires that exceptions be handled in program order ; therefore, although a particular implementation may recognize exception conditions out of order, they are presented strictly in order. When an instruction-caused exception is recognized, any unexecuted instructions that appear earlier in the instruction stream, including any that have not yet entered the execute state, are required to complete before the exception is taken. Any exceptions caused by those instructions are handled first. Likewise, exceptions that are asynchronous and precise are recognized when they occur, but are not handled until the instruction currently in the completion state successfully completes execution or generates an exception, and the completed store queue is emptied.

Unless a catastrophic causes a system reset or machine check exception, only one exception is handled at a time. If, for example, a single instruction encounters multiple exception conditions, those conditions are encountered sequentially. After the exception handler handles an exception, the instruction execution continues until the next exception condition is encountered. However, in many cases there is no attempt to re-execute the instruction. This method of recognizing and handling exception conditions sequentially guarantees that exceptions are recoverable.

Exception handlers should save the information stored in SRR0 and SRR1 early to prevent the program state from being lost due to a system reset and machine check exception or to an instruction-caused exception in the exception handler, and before enabling external interrupts.

The PowerPC architecture support four types of exceptions :

- **Synchronous, precise** - These are causes by instructions. All instruction-caused exceptions are handled precisely ; that is, the machine state at the time the exception occurs is known and can be completely restored. This means that (excluding the trap and system call exceptions) the address of the faulting instruction is provided to the exception handler and that neither the faulting instruction nor subsequent instructions in the code stream will complete execution before the exception is taken. Once the exception is processed, execution resumes at the address of the faulting instruction (or at an alternate address provided by the exception handler). When an exception is taken due to an trap or system call instruction, execution resumes at an address provided by the handler.
- **Synchronous, imprecise** - The PowerPC architecture defines two imprecise floating-point exception modes, recoverable and nonrecoverable. Even though the 603e provides a means to enable he imprecise modes, it implements these modes identically to the precise mode (-hat is, all enabled floating-point enabled exceptions are always precise on the 603e).
- **Asynchronous, maskable** - The external, SMI, and decrementer interrupts are maskable asynchronous exceptions. When these exceptions occur, their handling is postponed until the next instruction, and any exceptions associated with that instruction, completes execution. If there are no instructions in the execution units, the exception is taken immediately upon determination of the correct restart address (for loading SRR0).
- **Asynchronous, non maskable** - There are two non maskable asynchronous exceptions : system reset and the machine check exception. These exceptions may not be recoverable, or may provide a limited degree of recoverability. All exceptions report recoverability through the SMR[RI] bit.

5.4.2. PowerPC 603e microprocessor exception model

A specified by the PowerPC architecture, all 603e exceptions can be described as either precise or imprecise and either synchronous or asynchronous. Asynchronous exceptions (some or which are maskable) are caused by events external to the processor's execution ; synchronous exceptions, which are all handled precisely by the 603e, are caused by instructions. The 603e exception classes are shown in Table 14.

Synchronous/Asynchronous	precise/Imprecise	Exception type
Asynchronous, non maskable	Imprecise	Machine check System reset
Asynchronous, maskable	Precise	External interrupt Decrementer System management interrupt
Synchronous	Precise	Instruction-caused exceptions

Table 15 : PowerPC 603e microprocessor exception classifications

Although exceptions have other characteristics as well, such as whether they are maskable or non maskable, the distinctions shown in Table 15 define categories of exceptions that the 603e handles uniquely. Note that Table 15 includes no synchronous imprecise instructions. While the PowerPC architecture supports imprecise handling of floating-point exceptions, the 603e implements these exception modes as precise exceptions.

The 603e's exceptions, and conditions that cause them, are listed in Table 16. Exceptions that are specific to the 603e are indicated.

Table 16 : Exceptions and conditions

Exception Type	Vector Offset (hex)	Causing Conditions
Reserved	00000	—
System reset	00100	A system reset is caused by the assertion of either $\overline{\text{SRESET}}$ or $\overline{\text{HRESET}}$.
Machine check	00200	A machine check is caused by the assertion of the $\overline{\text{TEA}}$ signal during a data bus transaction, assertion of $\overline{\text{MCP}}$, or an address or data parity error.
DSI	00300	The cause of a DSI exception can be determined by the bit settings in the DSISR, listed as follows: 1 Set if the translation of an attempted access is not found in the primary hash table entry group (HTEG), or in the rehashed secondary HTEG, or in the range of a DBAT register; otherwise cleared. 4 Set if a memory access is not permitted by the page or DBAT protection mechanism; otherwise cleared. 5 Set by an **eciwx** or **ecowx** instruction if the access is to an address that is marked as write-through, or execution of a load/store instruction that accesses a direct-store segment. 6 Set for a store operation and cleared for a load operation. 11 Set if **eciwx** or **ecowx** is used and EAR[E] is cleared.
ISI	00400	An ISI exception is caused when an instruction fetch cannot be performed for any of the following reasons: • The effective (logical) address cannot be translated. That is, there is a page fault for this portion of the translation, so an ISI exception must be taken to load the PTE (and possibly the page) into memory. • The fetch access violates memory protection. If the key bits (Ks and Kp) in the segment register and the PP bits in the PTE are set to prohibit read access, instructions cannot be fetched from this location.
External interrupt	00500	An external interrupt is caused when MSR[EE] = 1 and the $\overline{\text{INT}}$ signal is asserted.
Alignment	00600	An alignment exception is caused when the 603e cannot perform a memory access for any of reasons described below: • The operand of a floating-point load or store instruction is not word-aligned. • The operand of **lmw, stmw, lwarx**, and **stwcx.** instructions are not aligned. • The operand of a single-register load or store operation is not aligned, and the 603e is in little-endian mode. • The instruction is **lmw, stmw, lswi, lswx, stswi, stswx** and the 603e is in little-endian mode. • The operand of **dcbz** is in storage that is write-through-required, or caching inhibited.

Exception Type	Vector Offset (hex)	Causing Conditions
Program	00700	A program exception is caused by one of the following exception conditions, which correspond to bit settings in SRR1 and arise during execution of an instruction: • Floating-point enabled exception—A floating-point enabled exception condition is generated when the following condition is met: (MSR[FE0] | MSR[FE1]) & FPSCR[FEX] is 1. FPSCR[FEX] is set by the execution of a floating-point instruction that causes an enabled exception or by the execution of one of the "move to FPSCR" instructions that results in both an exception condition bit and its corresponding enable bit being set in the FPSCR. • Illegal instruction—An illegal instruction program exception is generated when execution of an instruction is attempted with an illegal opcode or illegal combination of opcode and extended opcode fields (including PowerPC instructions not implemented in the 603e), or when execution of an optional instruction not provided in the 603e is attempted (these do not include those optional instructions that are treated as no-ops). • Privileged instruction—A privileged instruction type program exception is generated when the execution of a privileged instruction is attempted and the MSR register user privilege bit, MSR[PR], is set. In the 603e, this exception is generated for **mtspr** or **mfspr** with an invalid SPR field if SPR[0] = 1 and MSR[PR] = 1. This may not be true for all PowerPC processors. • Trap—A trap type program exception is generated when any of the conditions specified in a trap instruction is met.
Floating-point unavailable	00800	A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and move instructions) when the floating-point available bit is disabled, (MSR[FP] = 0).
Decrementer	00900	The decrementer exception occurs when the most significant bit of the decrementer (DEC) register transitions from 0 to 1. Must also be enabled with the MSR[EE] bit.
Reserved	00A00–00BFF	—
System call	00C00	A system call exception occurs when a System Call (**sc**) instruction is executed.
Trace	00D00	A trace exception is taken when MSR[SE] =1 or when the currently completing instruction is a branch and MSR[BE] =1.
Reserved	00E00	The 603e does not generate an exception to this vector. Other PowerPC processors may use this vector for floating-point assist exceptions.
Reserved	00E10–00FFF	—
Instruction translation miss	01000	An instruction translation miss exception is caused when an effective address for an instruction fetch cannot be translated by the ITLB.
Data load translation miss	01100	A data load translation miss exception is caused when an effective address for a data load operation cannot be translated by the DTLB.
Data store translation miss	01200	A data store translation miss exception is caused when an effective address for a data store operation cannot be translated by the DTLB; or where a DTLB hit occurs, and the change bit in the PTE must be set due to a data store operation.

Exception Type	Vector Offset (hex)	Causing Conditions
Instruction address breakpoint	01300	An instruction address breakpoint exception occurs when the address (bits 0– 29) in the IABR matches the next instruction to complete in the completion unit, and the IABR enable bit (bit 30) is set to 1.
System management interrupt	01400	A system management interrupt is caused when MSR[EE] =1 and the $\overline{SMI}$ input signal is asserted.
Reserved	01500–02FFF	—

5.5. Memory management

The following subsections describe the memory management features of the PowerPC architecture, and the 603e implementation, respectively.

5.5.1. PowerPC memory management

The primary functions of the MMU are to translate logical (effective) addresses to physical addresses for memory accesses, and to provide access protection on blocks and pages of memory.

There are two types of accesses generated by the 603e that require address translation - instruction accesses, and data accesses to memory generated by load and store instructions.

The PowerPC MMU and exception model support demand-paged virtual memory. Virtual memory management permits execution of programs larger than the size of physical memory ; demand-paged implies that individual pages are loaded into physical memory from system memory only when they are first accessed by an executing program.

The hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

The page table contains a number of page table entry groups (PTEGs). A PTEG contains eight page table entries (PTEs) of eight bytes each ; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

Address translations are enabled by setting bits in the MSR-MSR[IR] enables instruction address translations and MSR[DR] enables data address translations.

5.5.2. PowerPC 603e microprocessor memory management

The instruction and data memory management units in the 603e provide 4 Gbyte of logical address space accessible to supervisor and user programs with a 4-Kbyte page size and 256-Mbyte segment size. Block sizes range from 128 Kbyte to 256Mbyte and are software selectable. In addition, the 603e uses an interim 52-bit virtual address and hashed page tables for generating 32-bit physical addresses. The MMUs in the 603e rely on the exception processing mechanism for the implementation of the paged virtual memory environment and for enforcing protection of designated memory areas.

Instruction and data TLBs provide address translation in parallel with the on-chip cache access, incurring no additional time penalty in the event of a TLB hit. A TLB is a cache of the most recently used page table entries. Software is responsible for maintaining the consistency of the TLB with memory. The 603e's TLBs are 64-entry, two-way set-associative caches that contain instruction and data address translations. The 603e provides hardware assist for software table search operations through the ashed page table on TLB misses. Supervisor software can invalidate TLB entries selectively.

The 603e also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbyte to 256 Mbyte. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of page table entry groups (PTEGs). A PTEG contains eight page table entries (PTEs) of eight bytes each ; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

5.6. Instruction timing

The 603e is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603e has four major pipeline stages, described a follows :

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction fetch. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction fetch stage, and determining which of the instructions are eligible to be dispatched in the current cycle. in addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage that the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/writeback pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store units has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.
- The complete/writeback pipeline stage maintains the correct architectural machine state and transfers the contents of the rename registers to the GPRs and FPRs as instructions are retired. If the completion logic detects an instruction causing an exception, all following instructions are cancelled, their execution results in rename registers are discarded, and instructions are fetched from the correct instruction stream.

A superscalar processor is one that issues multiple independent instructions into multiple pipelines allowing instructions to execute in parallel. The 603e has five independent execution units, one each for integer instructions, floating-point instructions, branch instructions, load/store instructions, and system register instructions. The IU and the FPU each have dedicated register files for maintaining operands (GPRs and FPRs, respectively), allowing integer calculations and floating-point calculations to occur simultaneously without interference.

Because the PowerPC architecture can be applied to such a wide variety of implementations, instruction timing among various PowerPC processors varies accordingly.

6. PREPARATION FOR DELIVERY

6.1. Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

6.2. Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

7. HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

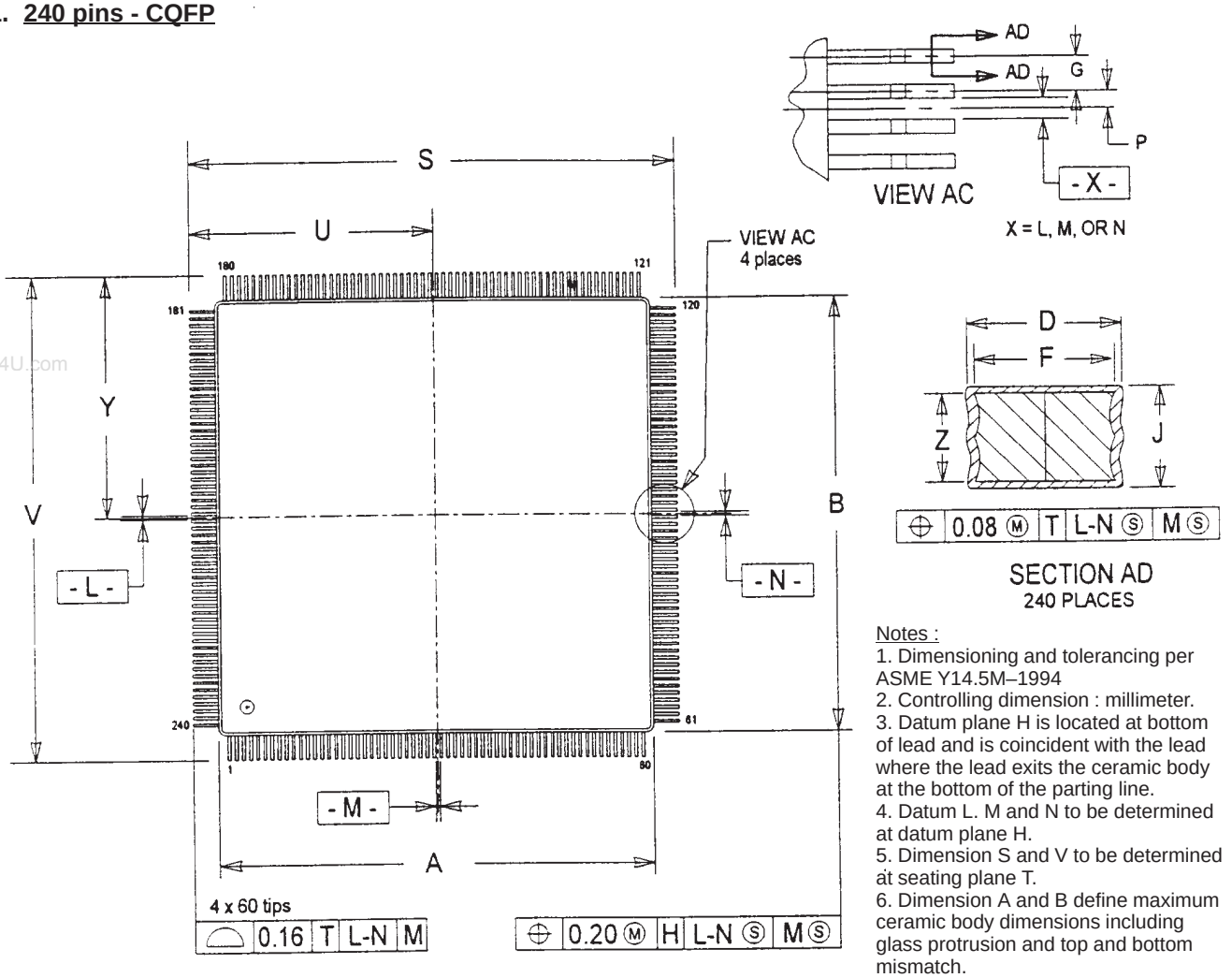
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

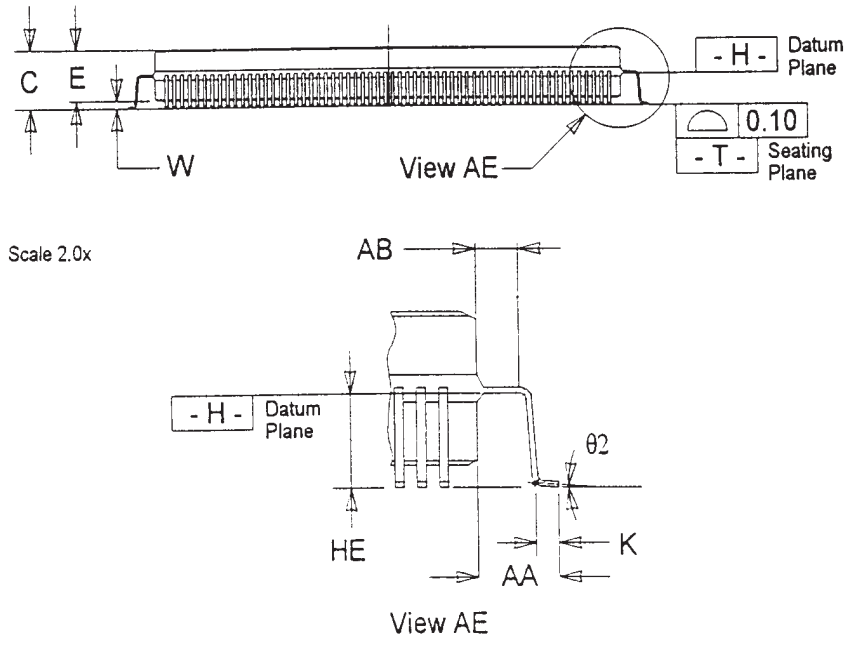
f) Maintain relative humidity above 50 percent if practical.

8. PACKAGE MECHANICAL DATA

8.1. 240 pins - CQFP



Notes :
1. Dimensioning and tolerancing per ASME Y14.5M–1994
2. Controlling dimension : millimeter.
3. Datum plane H is located at bottom of lead and is coincident with the lead where the lead exits the ceramic body at the bottom of the parting line.
4. Datum L. M and N to be determined at datum plane H.
5. Dimension S and V to be determined at seating plane T.
6. Dimension A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch.



MILLIMETERS			
DIM	MIN	TYP	MAX
A	30.86	31.00	31.75
B	30.86	31.00	31.75
C	3.67	3.95	4.15
D	0.185	0.220	0.270
E	3.10	3.50	3.90
F	0.175	0.200	0.225
G		0.50 BSC	
HE	2.025	2.100	2.175
J	0.130	0.147	0.175
K	0.45	0.50	0.55
P		0.25 BSC	
S	34.41	34.58	34.75
U	17.20	17.30	17.40
V	34.41	34.58	34.75
W	0.25	0.50	0.75
Y	17.20	17.30	17.40
Z	0.122	0.127	0.132
AA		1.80 REF	
AB		0.95 REF	
θ2	1°	4°	7°

Figure 17 : Mechanical dimensions of the Wire-bond CQFP package

8.2. BGA package description

The following sections provide the package parameters and mechanical dimensions for the CBGA packages.

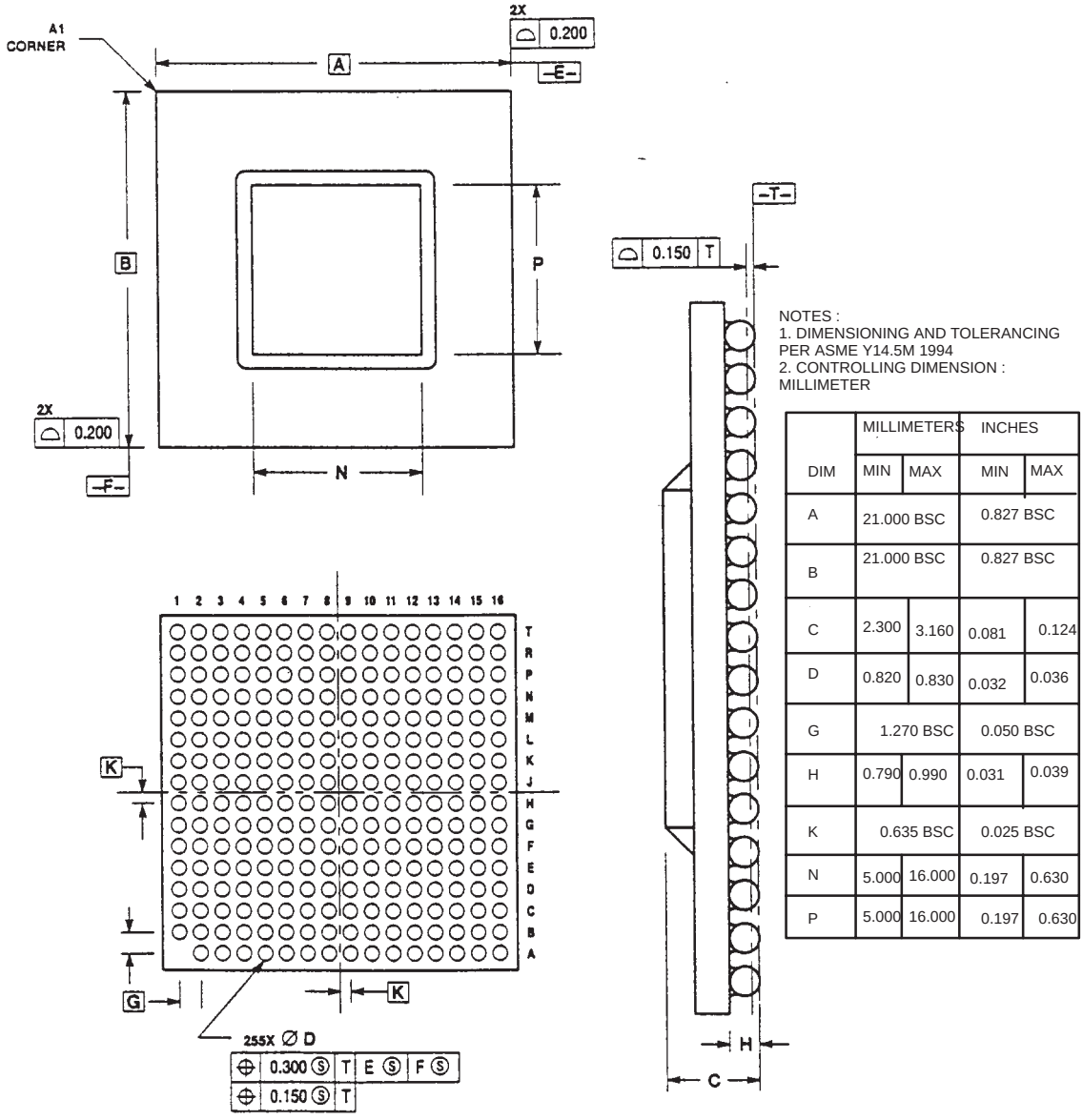
8.2.1.Package parameters

The package parameters are as provided in the following list. The package type is 21 mm, 255-lead ceramic ball grid array (CBGA).

Package outline . . . . . 21 mm
Interconnects 255
Pitch . . . . . 1.27 mm
maximum module height . . . 3.16 mm

8.2.2.Mechanical dimensions of the BGA package

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.300	3.160	0.081	0.124
D	0.820	0.830	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

Figure 18 : Mechanical dimensions and bottom surface nomenclature of the CBGA package

9. CLOCK RELATIONSHIPS CHOICE

The 603e microprocessors offer customers numerous clocking options. An internal phase-lock loop synchronizes the processor (CPU) clock to the bus or system clock (SYSCLK) at various ratios.

Inside each PowerPC microprocessor is a phase-lock loop circuit. A voltage controlled oscillator (VCO) is precisely controlled in frequency and phase by a frequency/phase detector which compares the input bus frequency (SYSCLK frequency) to a submultiple of the VCO.

The ratio of CPU to SYSCLK frequencies is often referred to as the bus mode (for example, 2:1 bus mode).

In the Table (Table 17), the horizontal scale represents the bus frequency (SYSCLK) and the vertical scale represents the PLL–CFG[0–3] signals.

For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

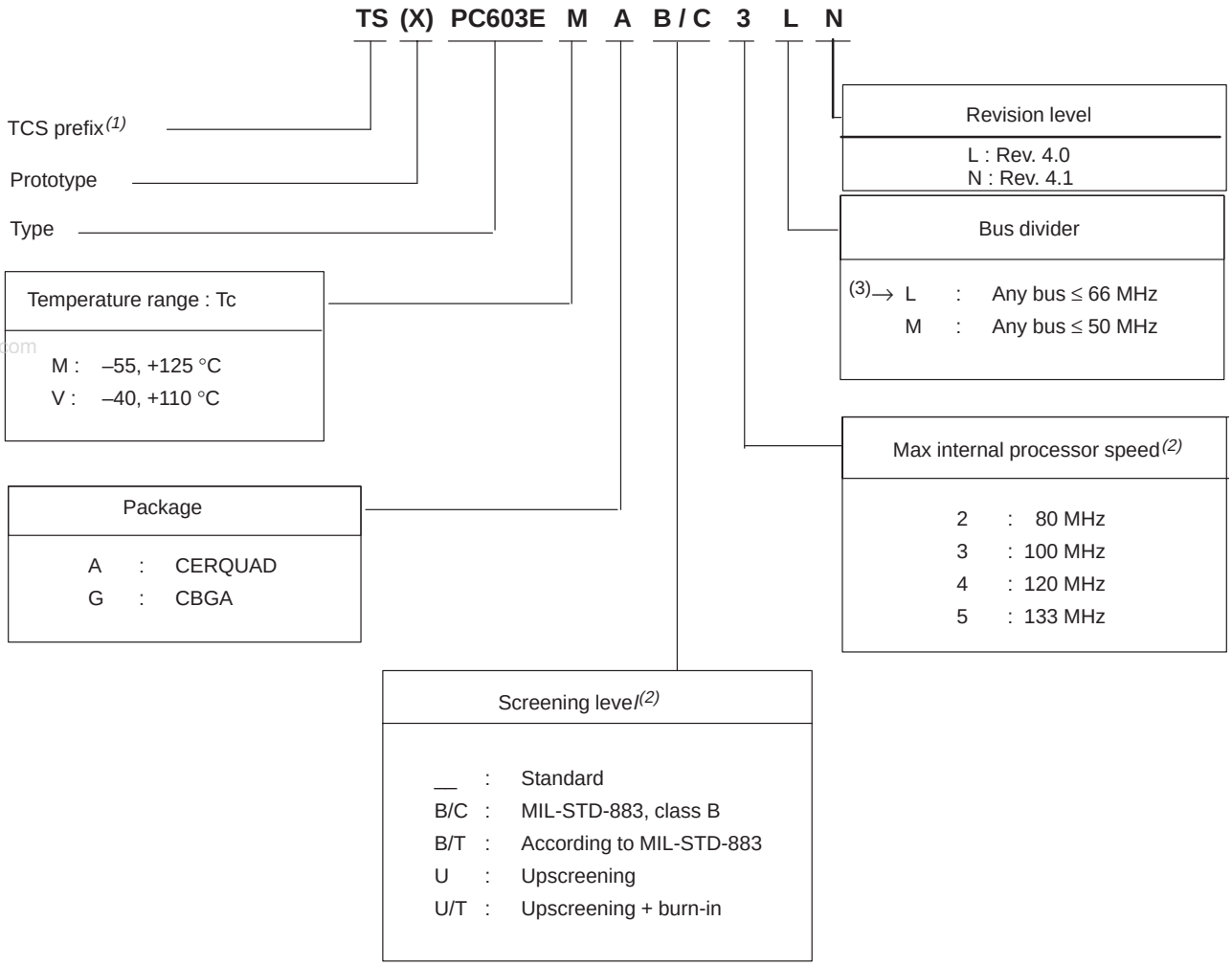
Table 17 : CPU frequencies for common bus frequencies and multipliers

PLL_CFG[0–3]	CPU Frequency in MHZ (VCO Frequency in MHz)								
	Bus–to–Core Multiplier	Core–to VCO Multiplier	Bus 20 MHz	Bus 25 MHz	Bus 33.33 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.67 MHz
0000	1x	2x	–	–	–	–	–	–	–
0001	1x	4x	–	–	–	–	–	–	–
0010	1x	8x	–	–	–	–	–	–	–
1100	1.5x	2x	–	–	–	–	–	90 (180)	100 (200)
0100	2x	2x	–	–	–	80 (160)	100 (200)	120 (240)	133.33 (266)
0101	2x	4x	–	–	–	–	–	–	–
0110	2.5x	2x	–	–	83.33 (166)	100 (200)	125 (250)	–	–
1000	3x	2x	–	–	100 (200)	120 (240)	–	–	–
1110	3.5x	2x	–	87.5 (175)	116.67 (233)	–	–	–	–
1010	4x	2x	80 (160)	100 (200)	133.33 (266)	–	–	–	–
0011	PLL bypass								
1111	Clock off								

Notes :

1. Some PLL configurations may select bus, CPU or VCO frequencies which are not supported
2. In PLL–bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note : the AC timing specifications given in this document do not apply in PLL–bypass mode.
3. In clock–off mode, no clocking occurs inside the 603e regardless of the SYSCLK input.

10. ORDERING INFORMATION



(1) THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

(2) For availability of the different versions, contact your TCS sale office

(3) Preferred option (to be confirmed)

This product is manufactured and commercialized by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - Avenue de Rochepleine PO Box 123 - 38521 SAINT-EGREVE Cedex - FRANCE.

For further information please contact :

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