

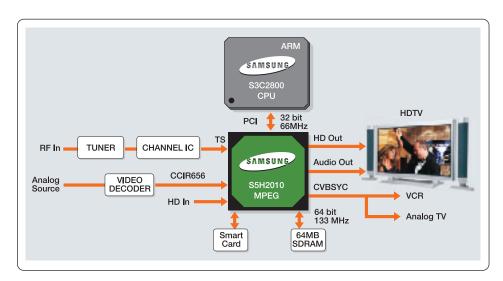
Samsung S5H2010 / S3C2800

Chipset Solution for High-Definition TVs and Set-Top Boxes

With the FCC's recent mandate that nearly all televisions incorporate a digital tuner within the decade, coupled with advanced functionality now available in high-definition TVs and set-top boxes, consumers are now demanding DVR capability and high-definition quality. Dual-output tuning is driving set-top box replacement at the high end.

Samsung's HDTV chipset is the cost-effective, high-performance solution. An MPEG-2 decoder (S5H2010) and digital TV CPU (S3C2800) provide enhanced picture quality and graphical user interface.

Advanced features include a 200MHz ARM9 32-bit RISC processor core, single HD-capable MPEG-2 decoder, transport demultiplexer, 2D graphic engine, display processor engine, NTSC/PAL encode, Smart Card interface, and PCI. The chipset includes a complete development platform, reference design, production-ready middleware, device drivers, application software and technical support.



Samsung Digital TV Platform
System Application

► Samsung's S5H2010 / S3C2800 chipset solution delivers high-performance at an incredible price, making high-definition TVs and set-top boxes an affordable reality most consumers.





Samsung's S5H2010 / S3C2800 chipset includes features that allow engineers to simplify the design process, hasten time-to-market, and lower the bill-of-materials.

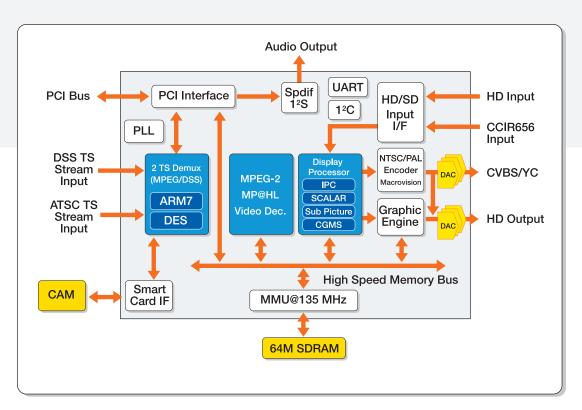
S5H2010 / S3C2800 Chipset Key Features

- High-performance companion CPU with 200MHz, ARM920T, 32-bit RISC processor core
- MPEG-2 MP&HL video decoder
- MPEG-2 TS demux (DSS, supports all 18 ATSC video formats)
- Built-in DES descrambler
- Display processor engine with advanced IPC and scalar for better picture quality
- NTSC video encoder integrated on chip
- NTSC output with Macrovision and closed caption

- Analog/Digital HD out (1080i, 720p, 480p)
- Supports three types of video output formats: analog HD video, digital HD video, and analog SD video
- Core on-chip peripherals: I²C, UART, Smart Card interface
- Peripheral expansion through PCI
- Reference board with various RTOS and popular middleware support

S5H2010 MPEG-2 Decoder

Samsung's S5H2010 MPEG-2 decoder supports resolutions of 720 x 480p and 1280 x 720p at 60 frames per second to provide high-quality video for HDTV.



S5H2010 MPEG-2 Decoder Internal Architecture

S5H2010 MPEG-2 Decoder Specifications

ARM7TDMI RISC CPU

- For programmable TS demux
- Speed: 67.5MHz @ 1.8V + 0.15V
- 16K-byte SRAM

External Memory Interface

64-bit wide SDRAM interface

TS (Transport Stream) Demux Engine

- S/W demux configuration using ARM7 TDMI
- MPEG-2 or DSS TS demux
- ATSC support
- Built-in DES descrambler
- Receives 48 PIDs simultaneously
- CRC (MPEG-2 : 32bit, DSS : 16bit)
- Built-in Clock Recovery Circuit for Program Clock Recovery

MPEG Video Decoder

- ISO/IEC 11172-2 (MPEG-1) format
- SO/IEC 13818-2 MP@HL (MPEG-2) format
- DSS MPEG-1 format
- DSS MPEG-2 SD and HD format

Various Video Input Formats

- TS stream
- Digital HD (RGB/YcbCr) (24 bit)
- Digital SD (8 bit)
- Supports ITU-R 656/ITU-R 656

Display Processor

- 4 display planes (background, video, OSD, and cursor)
- Letter box, pan/scan display pillar-box (side wall) panorama display
- 3D IPC
- PIP

Various Video Output Formats

- Digital HD (1080i, 720p, 480p, RGB/YcbCr)
- Analog HD CGMS, Macrovision
- Analog SD, CGMS, Macrovision (CVBS, S-video)

Graphic Processor

- 4 Graphic windows (on the OSD plane)
- Window and/or pixel blending
- 2D Graphic accelerator

Audio Input/Output Supports

- PCM 2-channel with 2-channel output
- 2-Channel SPDIF input externally and outputs in PCM or SPDIF data format
- Supports I²S and EIJA serial data outpot formats
- Supports formats converting PCM to SPDIF

On-Chip Peripherals

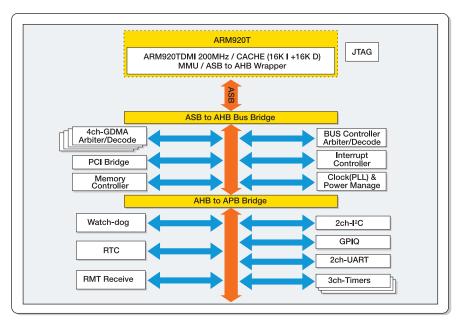
- PCI interface (32-bit, 33MHz)
- UART, Smart Card I/F, Output GPIO

JTAG Interface (including ARM7)

Package: 492-pin BGA

S3C2800 Microprocessor

Samsung's S3C2800 32 bit RISC microprocessor, based on an ARM920T core is developed using 0.18um CMOS standard cells and a memory compiler. It's elegant, fully static low-power design is ideal for HDTV and set-top box applications.



S3C2800 CPU Internal Architecture

S3C2800 CPU Specifications

Architecture

- ARM920T CPU core with maximum clock frequency of 200MHz at 1.8V
- Memory management unit
- Internal AMBA bus architecture (AMBA 2.0, AHBA/APB)

Memory Controller

- Address space: 32-Mbytes per each bank
- Supports programmable 8/16/32-bit data bus width for each memory bank
- 8 memory banks

I/D (Instruction/Data) Cache Memory

 64-way set-associative I-Cache (16KB) and D-Cache (16KB)

Clock & Power Manager

- On-chip PLL supports MCU at maximum of 200MHz at 1.8V
- Power Management support

PCI Bus Interface

- Embedded PCI Host Bridge
- 32-bit data bus at 66MHz

Interrupt Controller

- 34 Interrupt sources
- Software polling interrupt mode

Timer

 3-Channel, 16-bit timer with DMA-based or interrupt-based operation

Watchdog Timer

■ 16-bit

Real Time Clock (RTC)

- RTC with calendar function
- 32.768KHz input clock

General-Purpose Input/Output (GPIO) Ports

44 Multiplexed input/output ports

UART

- 2-channel UART with DMA-based or interrupt based operation
- Supports hardware handshaking during transmit/receive operation

DMA Controller

 4-Channel, general-purpose Direct Memory Access controller without CPU intervention

I²C-BUS Interface

 2-Channel Multi-Master I²C-Bus with interrupt-based operation

Operating Voltage Range

- Core: 1.65V to 1.95V
- I/O: 3.0V to 3.6V

Package

208-pin LQFP

For more information on Samsung's S5H2010 / S3C2800 Chipset, visit: www.samsungsemi.com



➤ Samsung's S5H2010/S3C2800 chipset enables TV and STB manufacturers to quickly enter HDTV market with high-performance, highvalue digital solutions.



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