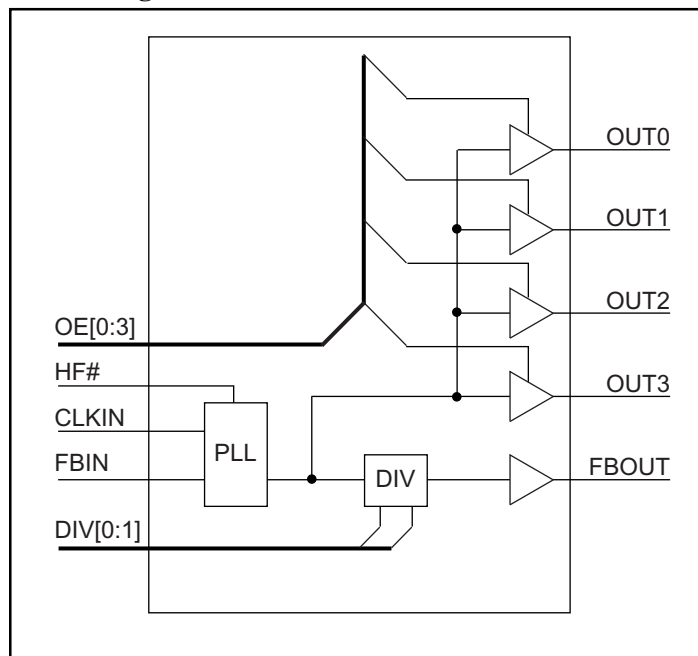
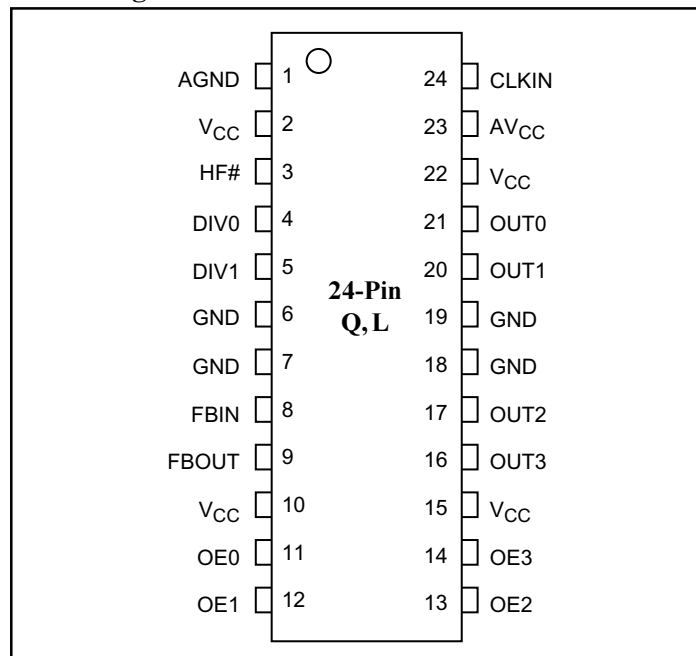


Product Features

- Four synchronous outputs
- Selectable divider/multiplier
- Output Enable control
- Low phase error < 150 ps
- Allows clock input to have spread spectrum modulation for EMI reduction
- Low output skew < 200 ps
- Low cycle jitter < 200 ps
- Industrial temperature (–40°C to 85°C)
- 3.3V V supply
- Packages: 24-pin QSOP (Q) and 24-pin TSSOP (L)

Product Description

PI6C2410 is a low skew, low jitter, PLL clock buffer with divider or multiplier designed for PCI-X application in servers and workstations. There are two selectable input ranges using HF# input: 10-40 MHz and 40-80 MHz. All outputs are synchronized to the input and to the other outputs. Each output can be independently turned off to reduce EMI and power consumption.

Block Diagram

Pin Configuration

Clock Select Table

HF#	DIV1	DIV0	OUT _x	CLKIN	OUT _x
1	1	1	CLKIN	33MHz	33MHz
1	1	0	2xCLKIN		66MHz
1	0	1	3xCLKIN		100MHz
1	0	0	4xCLKIN		133MHz
0	1	1	CLKIN/2	66MHz	33MHz
0	1	0	CLKIN		66MHz
0	0	1	1.5xCLKIN		100MHz
0	0	0	2xCLKIN		133MHz

Pin Description

Pin	Type	Qty	Symbol	Description
21,20,17,16	O	4	OUT[0:3]	Clock outputs. To achieve zero input to output delay, all outputs must have the same loading.
11-14	I	4	OE[0:3]	Active high Output Enable, pulled up. When OE is low, OUT [0:3] outputs are disabled at low state.
9	O	1	FBOUT	Feedback output. To achieve zero input to output delay, FBOUT must have the same loading as OUT[0:3].
8	I	1	FBIN	Feedback input. 7pF must be added to the output driving this pin (FBOUT) in addition to the other load.
24	I	1	CLKIN	Input Clock.
3	I	1	HF#	High Frequency range, pulled up. "1" = Low, "0" = High.
4,5	I	2	DIV[0,1]	Divider/Multiplier Select, pulled up.
2,10,15,22	P	4	V _{CC}	3.3V power
6,7,18,19	P	4	GND	Ground
23	P	1	AV _{CC}	3.3V analog power
1	P	1	AGND	Analog ground

Absolute Maximum Ratings

Supply Voltage (V _{CC} , AV _{CC})	0.5V to +7.0V
Input Voltage	-0.5V to V _{CC} +0.5V
Industrial Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C
Input ESD MIL-883, Method 3015, human body model	2kV

Operating Condition

Symbol	Description	Min.	Max.	Units
V _{CC} , AV _{CC}	I/O Supply, Analog Core Supply	3.0	3.6	V
T _A	Industrial Ambient Temperature	-40	+85	°C

DC Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{il}	Low Input Voltage				0.8	V
V _{ih}	High Input Voltage		2.0			
I _{il}	Low Input Current	V _{IN} = 0V			50	uA
I _{ih}	High Input Current	V _{IN} = V _{CC}			200	
V _{ol}	Low Output Voltage	V _{CC} = 3.0V, I _{ol} = 12mA			0.4	V
V _{oh}	High Output Voltage	V _{CC} = 3.0V, I _{oh} = -12mA	2.4			
I _{dd_33}	Supply Current	C _l = 15pF, F _{OUT} = 33MHz		25	tbd	mA
I _{dd_66}	Supply Current	C _l = 15pF, F _{OUT} = 66MHz		35		
I _{dd_100}	Supply Current	C _l = 15pF, F _{OUT} = 100MHz		45		
I _{dd_133}	Supply Current	C _l = 15pF, F _{OUT} = 133MHz		60		
C _o	Output Capacitance				6	pF
C _i	Input Capacitance				5	
C _l	Load Capacitance				15	
L _{pin}	Pin Inductance				7	nH

Switching Characteristics (T_A = 25°C, V_{CC} = 3.3V ± 0.3V, C_l = 15pF, F_{OUT} = 66.67 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
F _{in}	Input frequency	Low Freq., HF# = "1"	10	33	40	MHz
		High Freq., HF# = "0"	40	66	80	
T _{pd}	Propagation delay	CLKIN to FBIN rising edges @V _{DD} /2	-150		150	ps
T _{sk}	Output skew	@1.4V, rising edges			200	
T _{skpp}	Pkg to pkg skew	@V _{DD} /2, rising edges, same CLKIN			400	
T _{jc}	Cycle jitter				200	
T _{dc}	Duty cycle	@1.4V	45	50	55	%
T _r /T _f	Rise/Fall time	0.8V~2.0V			1.5	ns

Note: T_{jc} = T_p(n+1) - T_p(n) T_{dc} = T_h/T_p
 T_p(n) = Period of the nth cycle T_p = Period cycle time
 T_p(n+1) = Period of nth+1 cycle T_h = High time @1.4V

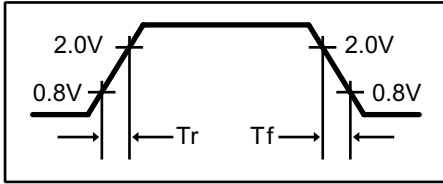


Figure 1. Rise/Fall time

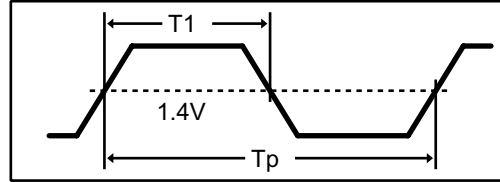


Figure 2. Duty cycle

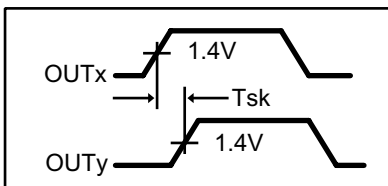


Figure 3. Output skew

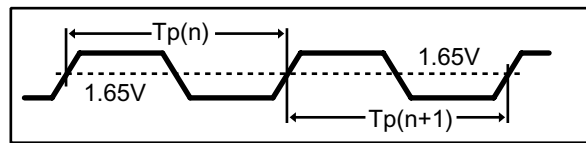


Figure 4. Cycle jitter

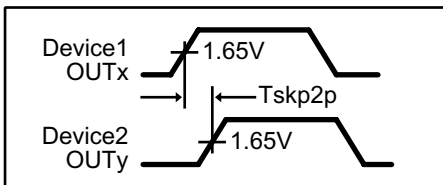


Figure 5. Pkg.-to-Pkg. skew

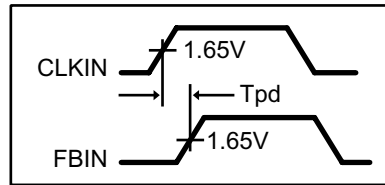


Figure 6. Propagation Delay

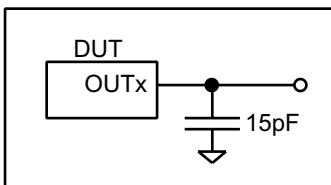


Figure 7. Test load

