T-52-33-03

5CBIC PROGRAMMABLE BUS INTERFACE CONTROLLER

- **Higher Integration Alternative to Transceivers, Latches, Multiplexers and PAL* Functions**
- **Applications Include Dual Port Control, Multiplexed Bus Interface, DRAM Control and Similar Functions**
- **Port-Oriented Bus Management Unit Supports:**
  - **3-Way Asynchronous Data Transfer on Byte-Wide Buses**
  - **Programmable Option of Latched or Real Time Data**
  - **True or Complement Data Path**
- **Macrocell-Based Programmable Logic Unit Provides:**
  - **Variable Input and Output Architecture**
  - **On-Chip Controls for the Bus Management Unit**
  - **Up to Eight Buried Registers**
  - **Programmable Registers can be Configured as Positive Edge-Triggered D-, J-K, R-S or T- Types**
  - **Asynchronous Preset and Clear on All Registers**
  - **Option of Latched Inputs**
- **Low Power: 75 μA Typical Standby**
- **CHMOS EPROM Technology Based:**
  - **Max Bus Port Drive Capability: 16 mA**
  - **Typical Data Transfer Delay Between Ports = 45 ns**
- **Available in 44-Lead Package**
  (See Packaging Spec., Order # 231369)

The Intel 5CBIC is useful in implementing bus interfacing logic functions that have traditionally been done using SSI/MSI TTL components. Core bus functions are provided that can be customized using EPROM bits for specific applications. Control logic can also be implemented through a sum of products architecture that is included in this 44-lead package. Such levels of integration are realized utilizing the benefits of Intel's advanced CHMOSII-E process.

This general purpose architecture is supported by iPLDS II, Intel's Programmable Logic Development System, to develop the design and program the devices. Several methods of entry facilitate the design resulting in shorter completion times.

*PAL is a trademark of Monolithic Memories, Inc.

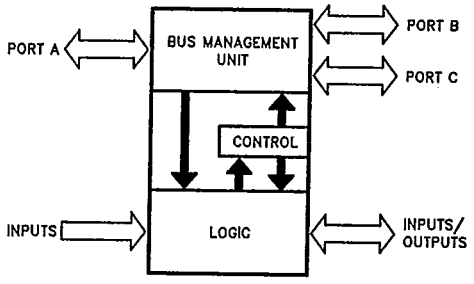


Figure 1. Block Diagram

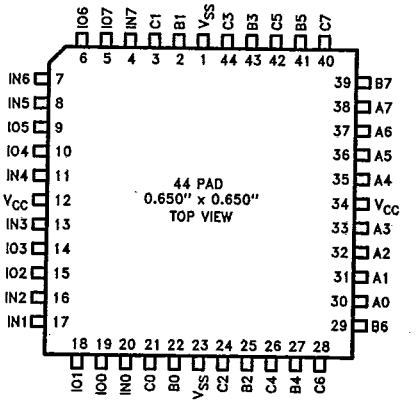


Figure 2. Lead Configuration

August 1988
Order Number: 290126-004

FUNCTIONAL DESCRIPTION

As the name suggests, this programmable bus interface controller offers a high integration solution to design problems involving data transfer on bus lines and the logic needed to control these transfers. This integration directly translates into savings in board space and lower system cost for equivalent functions implemented using conventional SSI/MSI components.

Present in the port-oriented 5CBIC are two functional blocks that enable complex bus functions to be realized: the Bus Management Unit (BMU) and the Programmable Logic Unit (PLU). These two units communicate with each other through the input and the feedback buses. A control section shown in Figure 3 steers signals from the PLU to the two units through the control bus.

ARCHITECTURE DESCRIPTION

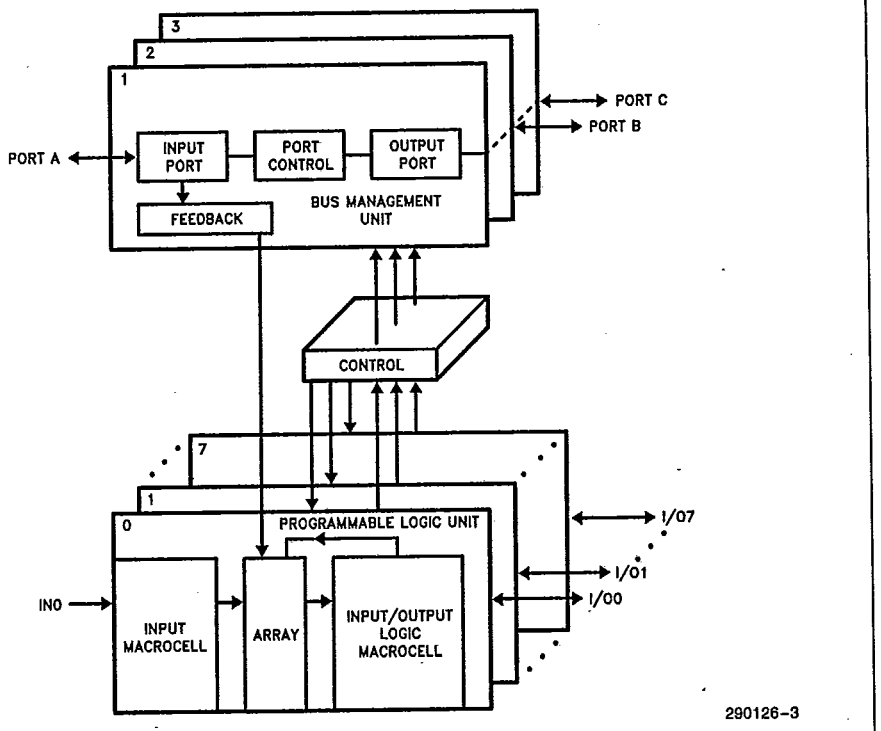
The innovative architecture of the 5CBIC incorporating a port-oriented approach for bus interface control is illustrated in Figure 5. The Bus Management Unit (BMU) and the Programmable Logic Unit (PLU) interface to the feedback and the control busses. The macrocells in the PLU feed the input bus.

Bus Management Unit (BMU)

The Bus Management Unit (BMU) comprises three ports: PA, PB and PC (Figure 4a). Each of these ports is bidirectional and 8 bits wide. Data can be routed from any port to any other port.

Data into any port can be user-selected to be latched by a port Latch Enable signal, (LE). Routing of latched or unlatched data between ports is achieved using a combination of EPROM architecture and dynamic control signals defined by the user. Data out of any port can be programmed to have an inverted sense through EPROM architecture control (INV).

Each bidirectional port can be dynamically configured as an input or an output depending on the control signals OEA, OEB and OEC. Latched data from



In the tridirectional BMU, any port can be steered to any other port. In this diagram, Port A can be directed to Port B or Port C or both. The PLU provides a 600-gate equivalent PAL function.

Figure 3. Functional Blocks in the 5CBIC

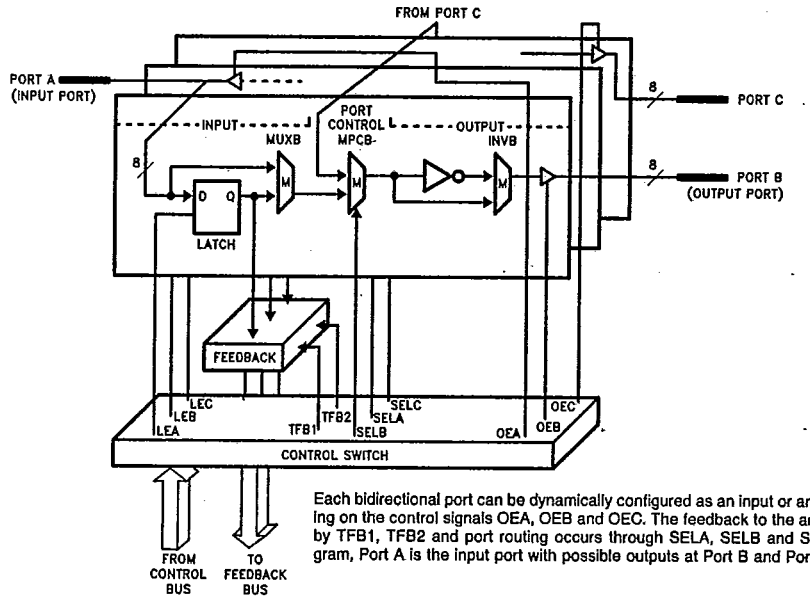
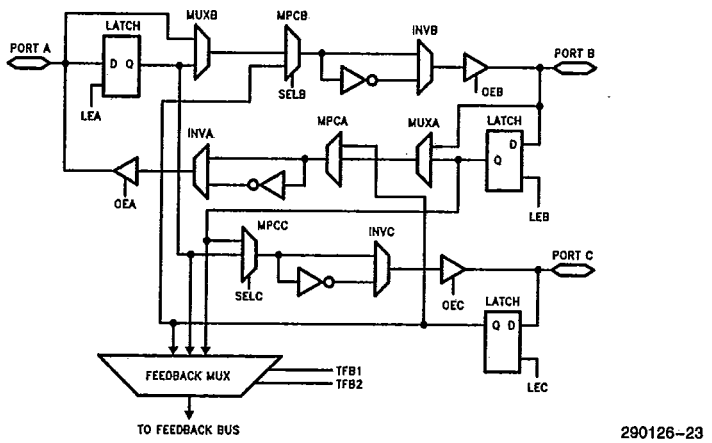


Figure 4a. Bus Management Unit Block Diagram



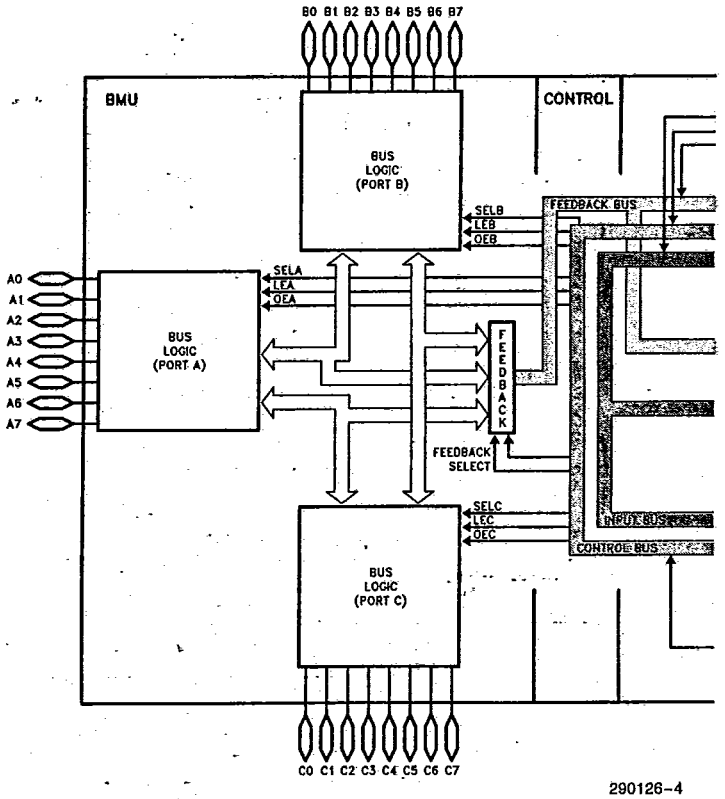
LEGEND:
OEA, OEB, OEC, SELA, SELB, SELC, LEA, LEB, LEC, TFB1 and TFB2 are the control outputs for the BMU derived from the control bus.
MPCA, MPCB and MPCC are dynamic multiplexers controlled by SELA, SELB and SELC for port selection.
MUXA, MUXB, INVA, INVB and INVC are static multiplexers controlled by architecture bits (EPROM bits).
All latches are the "transparent" type.

Figure 4b. BMU Logic Diagram

any incoming port can be fed internally to the array through TFB1 and TFB2. The three ports can be time-multiplexed, if needed. Port routing is controlled by signals SELA, SELB and SELC (Figure 4b).

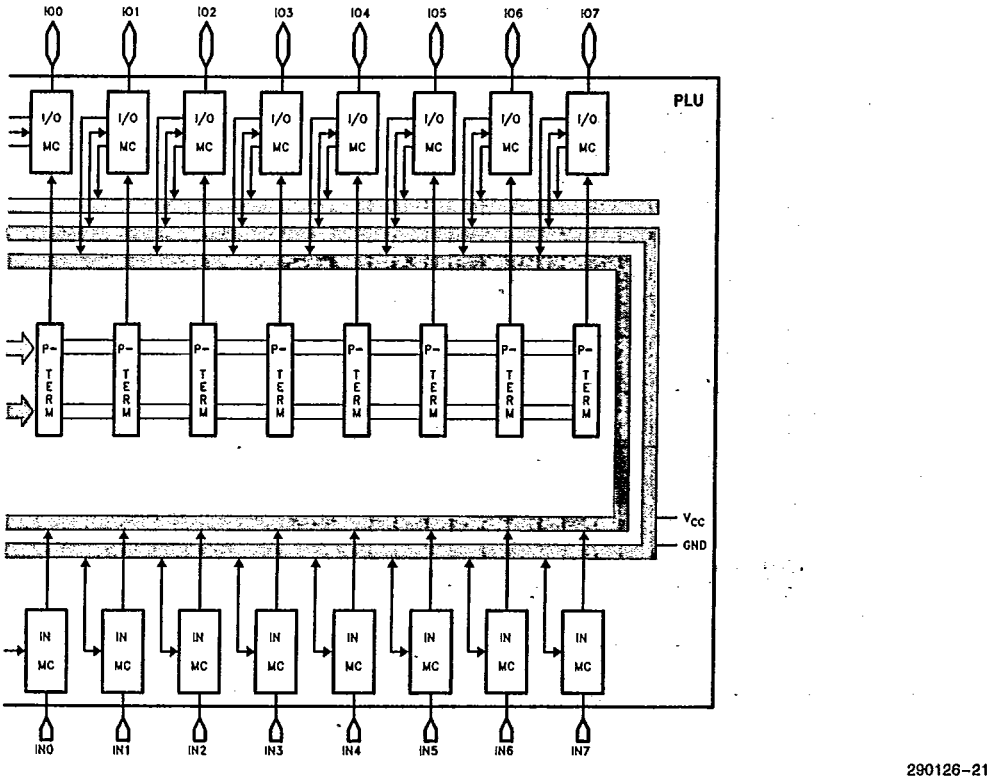
Programmable Logic Unit (PLU)

An on-chip 600-gate-equivalent EPLD supplies the control signals to the bus unit and related applica-



INMC = Input Macro Cell
IOMC = Input/Output Macro Cell
p-term = Product Terms through the logic array

Figure 5. The 5CBIC Architecture


I00
I01
I02
I03
I04
I05
I06
I07
I/O MC
PLU
P-TERM
V_{CC}
GND
IN MC
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
290126-21

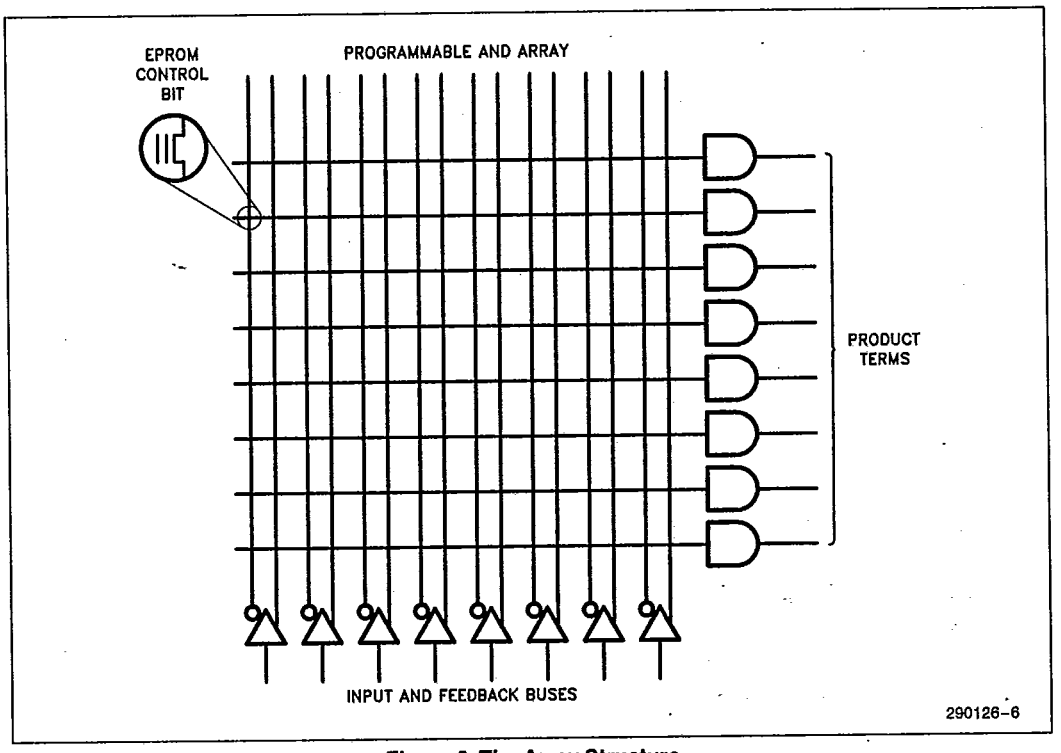


Figure 6. The Array Structure

tion functions in the system. A dedicated input port and a bidirectional I/O port, each 8 bits wide, allows control logic implementation in the 5CBIC. The macrocell based architecture enables the designer to use up to 24 inputs and 8 outputs.

The inputs, array and I/O marcrocells generate a sum-of-products (AND-OR) representation of any given logic. Within the AND array, there is an EPROM connection at every intersection of an incoming signal (true and complement) and a product term to a given macrocell (Figure 6). Before programming an erased device an EPROM connection exists at every intersection. It is during the programming process that these connections are opened to generate the required connections.

The bidirectional I/O port, when configured as an input, is identical to the input port in that inputs may be latched by a signal from the control bus as shown in Figure 7. An additional flow-through option for the data inputs is available in the input macrocell.

The variable output architecture in the PLU allows the designer to select the combinatorial or registered output types on a macrocell basis. This may be implemented by selecting the architecture bit MARB1 and the edge-triggered flip-flop (Figure 7). The Macrocells support D, T, S-R or J-K type registers for optimal design. Truth tables for these are listed in Figure 8 for easy reference. Whereas all eight of the product terms are OR-ed together at the register input for the D- and the T- registers, the J-K and the S-R configurations employ sharing of the product terms among two OR-gates.

The registers receive inputs at its data, clock, set and reset lines. Eight product terms are available for the data input and one each for the set and the clear inputs.

The clock, output enable and the latching signals can be selected by architecture bits MARB2, 6 and 3 respectively to be outputs from the control bus or one product term from the array. Designers thus have more options available for asynchronous clocking and output controls.

The macrocell output can be fed back to the array through the feedback bus or to the control bus. Figure 9 summarizes the bus structure and its relationship to the relevant units in the 5CBIC.

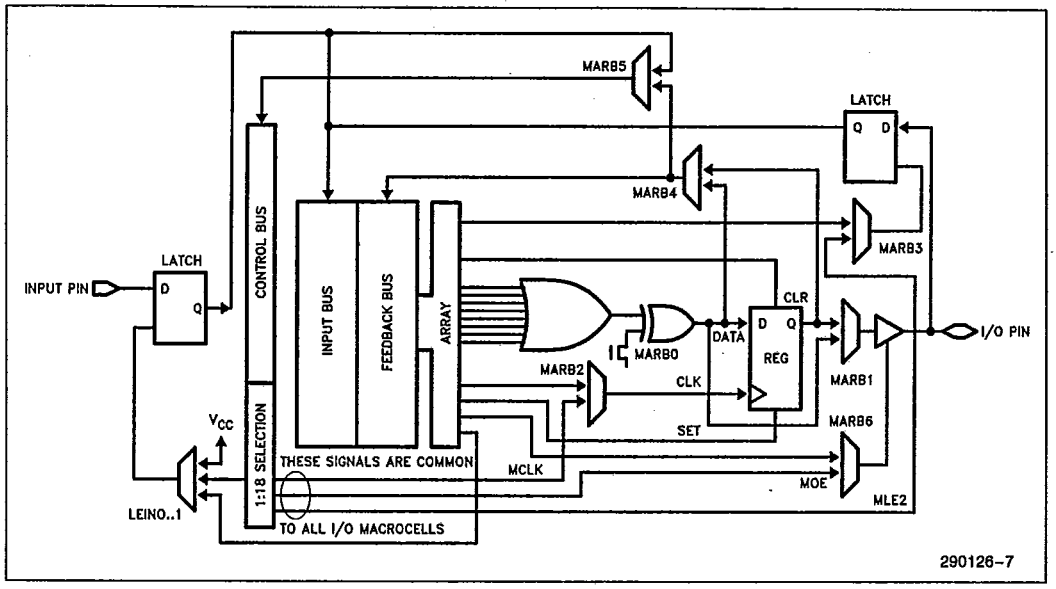


Figure 7. The Programmable Logic Unit

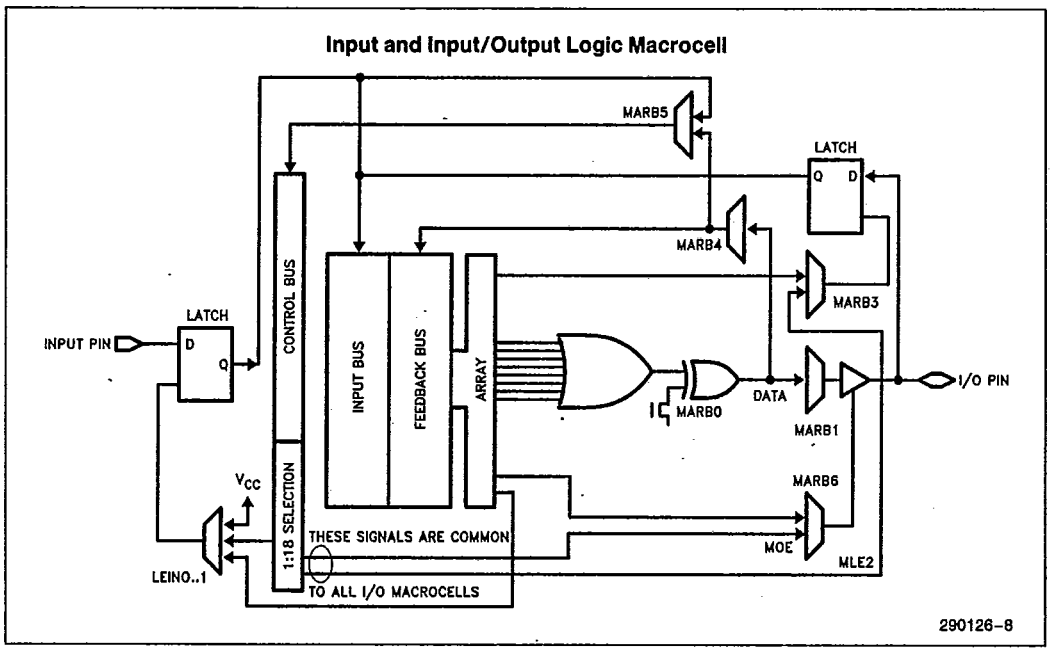
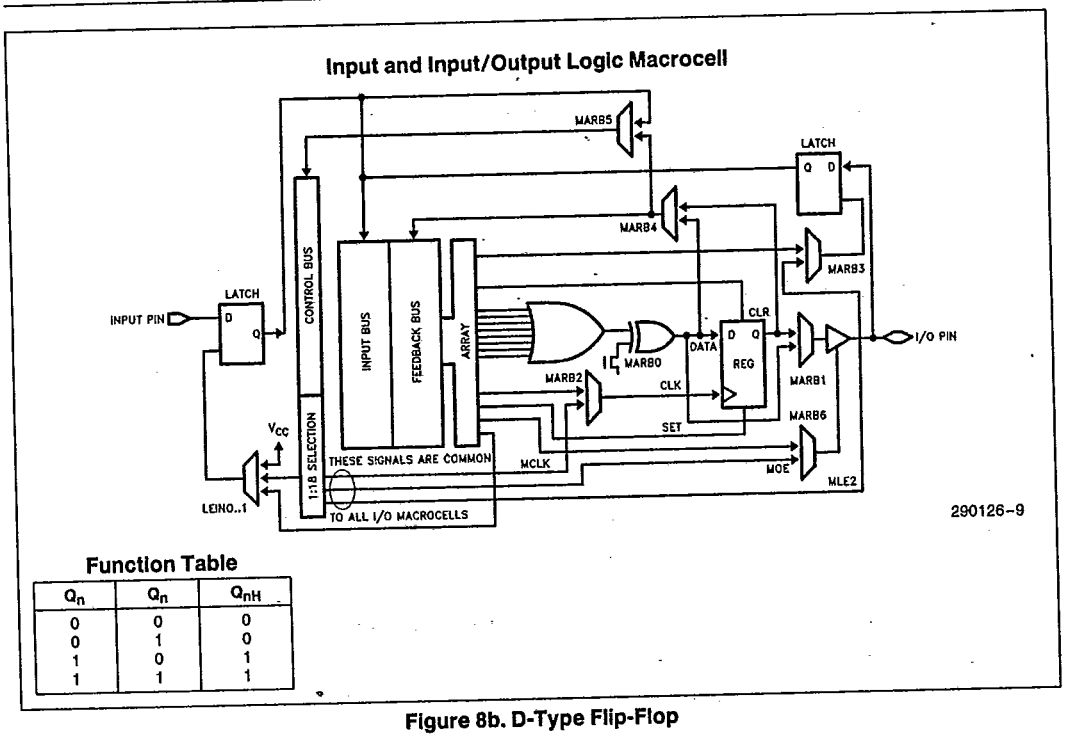


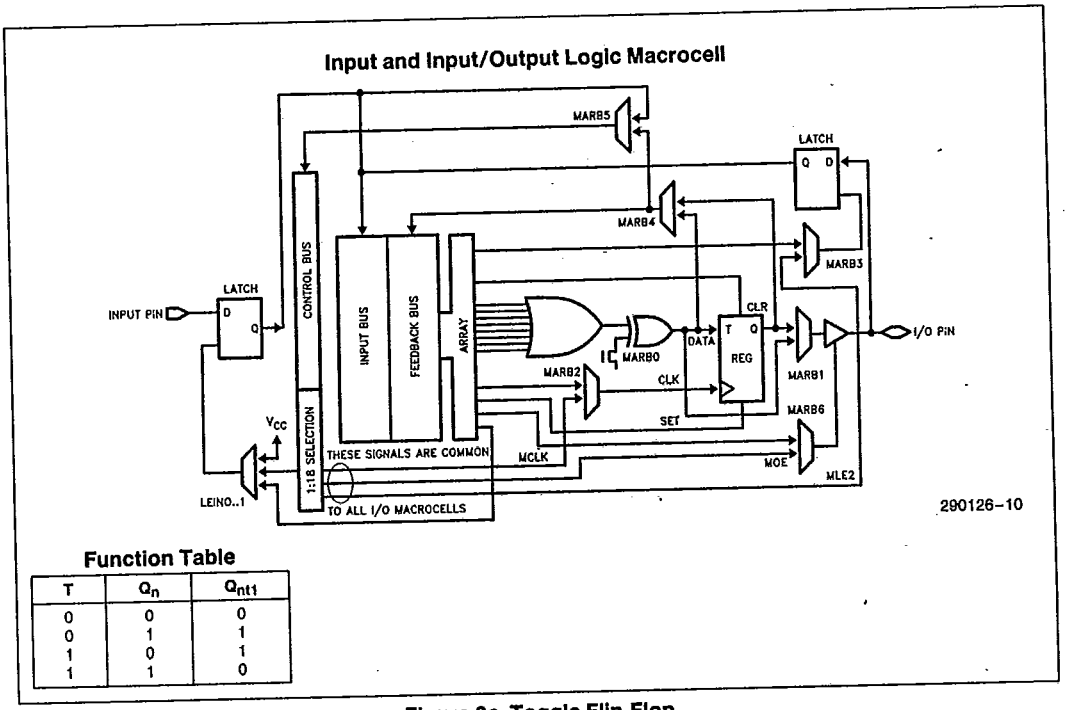
Figure 8a. Combinational



Function Table

Q_n	Q_n	Q_{nH}
0	0	0
0	1	0
1	0	1
1	1	1

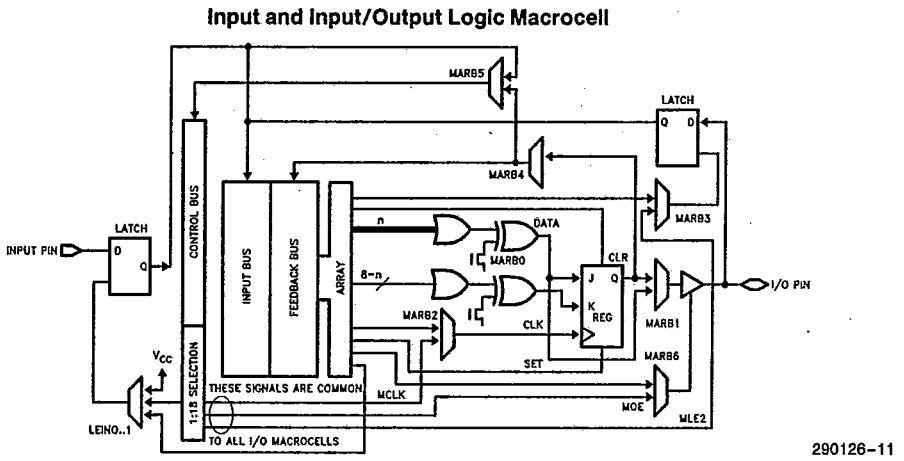
Figure 8b. D-Type Flip-Flop



Function Table

T	Q_n	Q_{nt1}
0	0	0
0	1	1
1	0	1
1	1	0

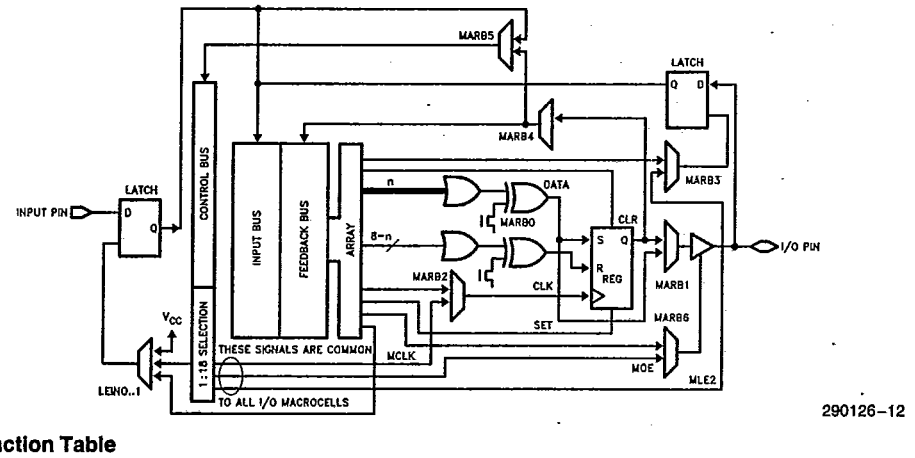
Figure 8c. Toggle Flip-Flop



Function Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 8d. J-K Flip-Flop



Function Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

Figure 8e. S-R Flip-Flop

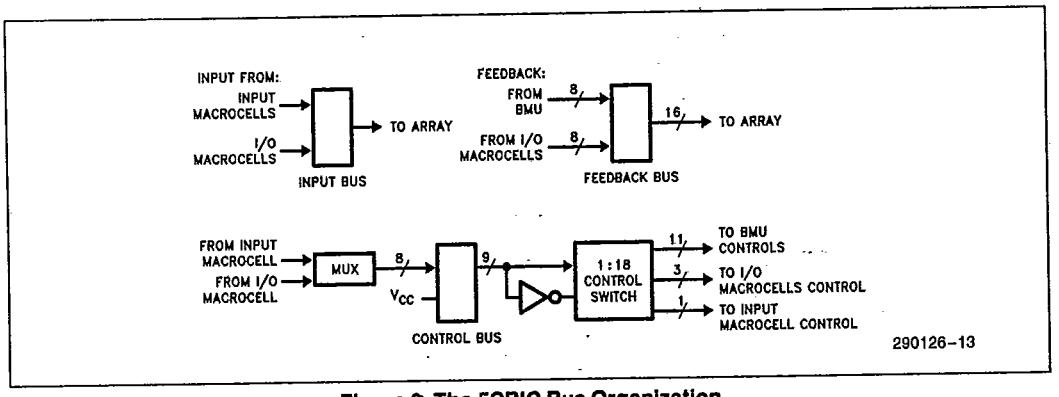


Figure 9. The 5CBIC Bus Organization

Configuring the 5CBIC

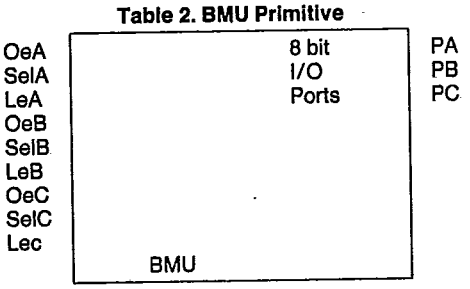
The Device Configuration Manager (DCM) in iPLS II provides a high-level graphic design entry alternative that allows bus configurations to be implemented in minutes. A more detailed explanation is given in the iPLS II manual. An ADF (Advanced Design File) is then automatically generated that defines the logic network using primitives.

The primitive necessary for configuring inter-port communication is the "BMU", while the one required for internal feedback from the BMU to the PLU is the feedback primitive "BFMUX". Tables 1 through 4 define these primitives and their fields/bits.

Table 1. BMU Architecture Bits

Architecture Bit	Selects
MUXA, MUXB	Latched or Flow-Through Port Data
INVA, INVB, INVC	True or Inverted Data Output

Table 2. BMU Primitive



Name: BMU (Bus Management (Unit)

ADF Syntax: PortA, PortB, PortC = BMU (Type, OeA, SelA, LeA, OeB, SelB, LeB, OeC, SelC, LeC)

Description:
- Port A = connection to 8 parallel I/O pins labeled A0–A7
- Port B = connection to 8 parallel I/O pins labeled B0–B7
- Port C = connection to 8 parallel I/O pins labeled C0–C7
- OeA= output enable for Port A
- SelA= select B or C internal connection to Port A (0 = C, 1 = B)
- LeA = input latch enable for Port A
- OeB= output enable for Port B
- SelB= select A or C internal connection to Port B (0 = C, 1 = A)
- LeB = input latch enable for Port B
- OeC= output enable for Port C
- SelC= select A or B internal connection to Port C (0 = A, 1 = B)
- LeC = input latch enable for Port C

Inversion Control				Input Latch		
Port:	**A**	**B**	**C**	**A**	**B**	**C**
Bit:	**5**	**4**	**3**	**2**	**1**	**0**
0	Invert Output	Invert Output	Invert Output	Latched A	Latched B	Latched C
1	No Invert	No Invert	No Invert	Direct A	Direct B	Latched C*

*If LeC is continually high, the C latch is transparent.

Table 3. Bus Feedback Multiplier Primitive

BFMX

TFB1	0	0	1	Fbk
TFB2	0	1	0	[0:7]
	C	B	A	

Name: BFMX (Bus Feedback Multiplexer

ADF Syntax: Fbk[0:7] = BFMX (TFB1, TFB2)

Description: Outputs.

Fbk = 8 parallel lines of feedback to logic array.

Inputs:

TFB1, TFB2 = By appling 0 or 1 as shown on the chart above, select feedback from Port A, B, or C. TFB1 and TFB2 can be set to VCC or GND, or they can be connected to any internal feedback or input node. The ports are defined in the BMU primitive section.

Table 4. PLU Architecture Bits

Architecture Bit	Selects
MARB0	Output Polarity
MARB1	Combinatorial or Registered Outputs
MARB2	Clock Source
MARB3	Latching Signal Source
MARB4	Combinatorial or Registered Feedback to the Logic Array
MARB5	Input Source to the Control Bus
MARB6	tri-state Control Signal

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC}+0.5	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

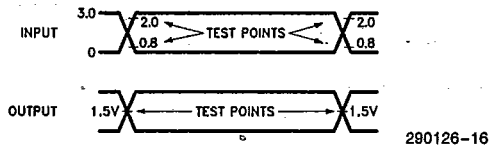
D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Parameter	Description	Min	Max	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		V	TTL: I_{OH} Port A −1 mA, Port B, C −5 mA, I, I/O −1 mA; V_{CC} = Min
V_{OL}	Output Low Voltage		0.45	V	I_{OL} Port A 5 mA, Port B, C 16 mA, I, I/O 5 mA; V_{CC} = Min
V_{IH}	Input High Level	2.0	V_{CC} +0.3	V	
V_{IL}	Input Low Level	−0.3	0.8	V	
I_I	Input Leakage Current		10	µA	$V_{SS} \le V_{IN} < V_{CC}$, V_{CC} = Max
I_{OZ}	Output Leakage Current		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$, V_{CC} = Max
I_{OS}(4)	Output Short Circuit Current	BMU PLU	80 16	mA mA	V_{CC} = Max, V_{OUT} = 0.5
I_{SB}(5)	Operating Current (standby, low power mode)		75	µA	V_{IN} = V_{CC} or Gnd, I_O = 0
I_{CC2}	Operating Current (active, low power mode)		20	mA	V_{IN} = V_{CC} or Gnd, f = 1 MHz, No Load
I_{CC3}	Operating Current (active, turbo mode)		108	mA	V_{IN} = V_{CC} or Gnd, f = 1 MHz, No Load
C_{IN}	Input Pin Capacitance		30	pF	
C_{OUT}	Output Pin Capacitance		40	pF	

NOTES:
4. Output shorted for no more than 1 sec. and only one output shorted at a time.
5. Chip automatically goes into standby mode if logic transitions do not occur at input pins. (Approximately 100 ns after last transition).

NOTES:
C_L includes jig capacitance
Device input rise and fall times < 6 ns

Figure 10. A.C. Testing Load Circuit

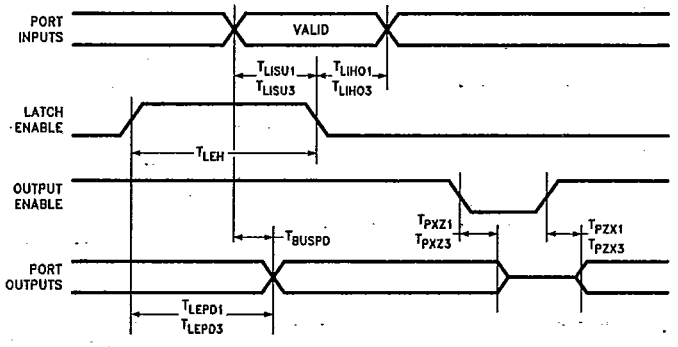


A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point.

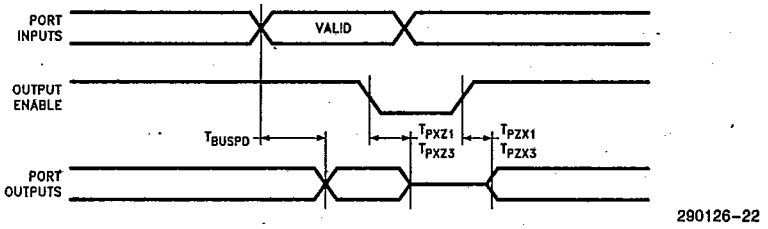
Figure 11. A.C. Testing Input, Output Waveform

Switching Characteristics

Notation:	Timing Suffix	Referenced to Control From:
	1	direct input pin
	2	product term
	3	control bus



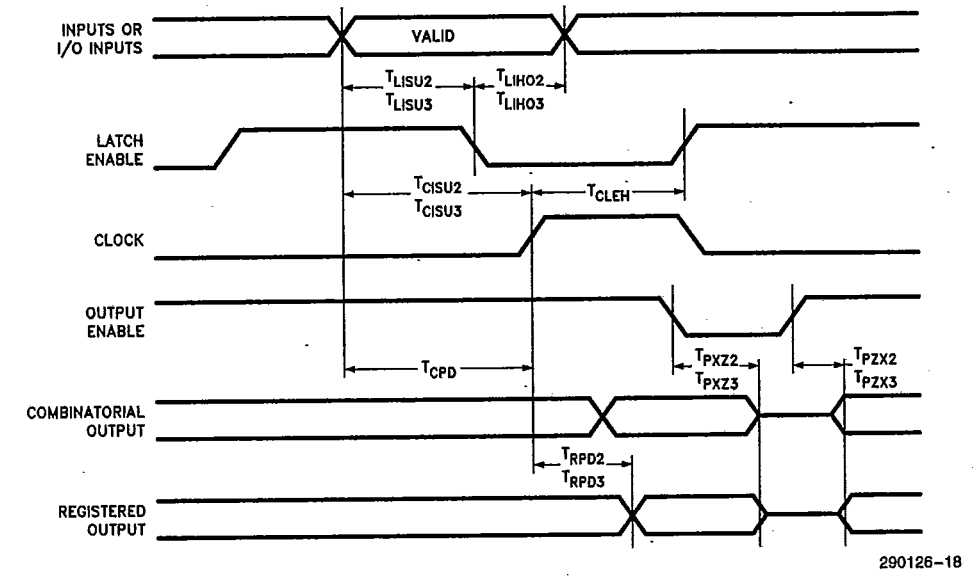
A) Latched Port Inputs



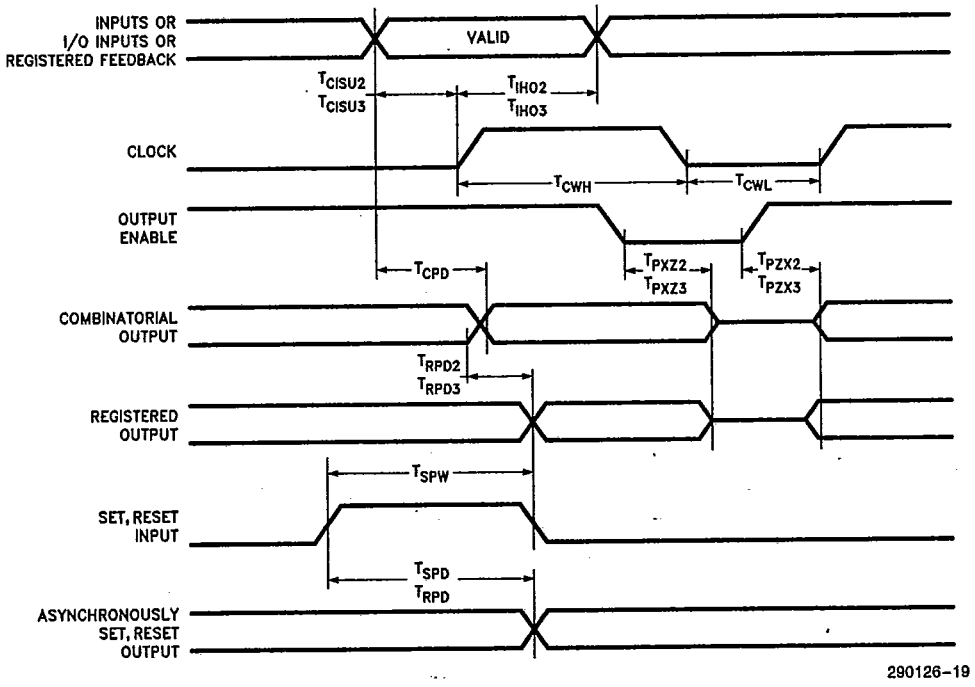
B) Direct Port Inputs

Figure 12. Bus Management Unit

Switching Characteristics (Continued)



A) Latched Inputs



B) Direct Inputs

Figure 13. Programmable Logic Unit

AC CHARACTERISTICS

BUS MANAGEMENT UNIT

Symbol	Parameter	-45			Units
		Min	Typ	Max	Max
T_{LISU1}	Port Input Setup Time to Latch Enable (Fast Option)	0			ns
T_{LISU3}	Port Input Setup Time to Latch Enable (Control Bus)	0			ns
T_{LIHO1}	Port Input Hold Time to Latch Enable (Fast Option)	55			ns
T_{LIHO3}	Port Input Hold Time to Latch Enable (Control Bus)	95			ns
T_{LEH}	Latch Enable High Time	45			ns
T_{BUSPD}	Port to Port Propagation Delay			45	ns
T_{PXZ1}	Valid Output to High Impedance (OE From Fast Option)			45	ns
T_{PXZ3}	Valid Output to High Impedance (OE From Control Bus)			95	ns
T_{PZX1}	High Impedance to Valid Output (OE From Fast Option)			45	ns
T_{PZX3}	High Impedance to Valid Output (OE From Control Bus)			95	ns
T_{LEPD1}	Latch Enable (From Fast Option) To Port Output Delay			65	ns
T_{LEPD3}	Latch Enable (From Control Bus) To Port Output Delay			95	ns

PROGRAMMABLE LOGIC UNIT

Symbol	Parameter	-45			Units
		Min	Typ	Max	
T_{LISU2}	Input Setup Time to Latch Enable (P-Term)	0			ns
T_{LISU3}	Input Setup Time to Latch Enable (Control Bus)	0			ns
T_{LIHO2}	Input Hold Time to Latch Enable (P-Term)	80			ns
T_{LIHO3}	Input Hold Time to Latch Enable (Control Bus)	90			ns
T_{CISU2}	Input Setup Time to Clock (P-Term)	20			ns
T_{CISU3}	Input Setup Time to Clock (Control Bus)	60			ns
T_{CLEH}	Clock to Latch Enable Hold Time	5			ns
T_{CPD}	Combinatorial Output Delay			135	ns

PROGRAMMABLE LOGIC UNIT (Continued)

Symbol	Parameter	−45			Units
		Min	Typ	Max	
T_{RPD2}(6)	Registered Output from Clock (P-Term)			115	ns
T_{RPD3}(7)	Registered Output from Clock (Control Bus)			70	ns
T_{IHO2}	Input Hold Time to Clock (P-Term)	25			ns
T_{IHO3}	Input Hold Time to Clock (Control Bus)	90			ns
T_{CWH}	Minimum Clock Width High	43			ns
T_{CWL}	Minimum Clock Width Low	43			ns
T_{SPD}	Set Output Delay			100	ns
T_{RPD}	Reset Output Delay			100	ns
T_{SPW}	SET/RESET Pulse Width	43			ns
T_{PXZ2}	Valid Output to High-Impedance (OE from P-Term)			85	ns
T_{PXZ3}	Valid Output to High Impedance (OE from Control Bus)			95	ns
T_{PZX2}	High Impedance to Valid Output (OE from P-Term)			95	ns
T_{PZX3}	High Impedance to Valid Output (OE from Control Bus)			95	ns
T_{CP1}	Minimum Clock Period (Register Output to Register Input Through Feedback Path)			110	ns
F1	Maximum Internal Frequency	9.0			MHz
T_{CP2}	Minimum Clock Period Between Logic Transitions (Inputs to Outputs)			135	ns
F2	Maximum External Frequency	7.0			MHz

NOTES:
6. Data out on rising edge of clock.
7. Data out on falling edge of clock.

int$_e$ligent Programming Algorithm™

The 5CBIC supports the int$_e$ligent Programming Algorithm which rapidly programs Intel H-ELPDs (and EPROMs) using an efficient and reliable method. The int$_e$ligent Programming Algorithm is particularly suited to the production programming environment. This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the 5CBIC is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature

over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

TURBO-BIT

The device will consume quiescent current (75 μA, typically) if no transitions are detected in the array for 100 ns or more. This mode, the power-down mode, can be enabled by selecting the Turbo Bit OFF. If this bit is enabled, however, the device consumes active current. The power-down mode will revert to its active state if a transition is detected in the array, at an extra delay of 25 ns in speed paths.

LATCH-UP IMMUNITY

All pins of the 5CBIC have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5CBIC designed with Intel's proprietary CHMOS II-E EPROM process. Thus, pins will not experience latch-up with currents up to 100 mA and voltages ranging from -1V to V_{CC} $+1$V. Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

INTEL PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM (iPLDS II)

iPLDS II provides all the tools needed to design with Intel H-Series EPLDs or compatible devices. In addition to providing development assistance, iPLDS II insulates the user from having to know all the intricate details of EPLD architecture (the machine will optimize a design to benefit from architectual features). It contains comprehensive third generation software that supports several different design entry methods, minimizes logic, does automatic pin assignments and produces the best design fit for the selected EPLD. It is user friendly with guided menus, on-line Help messages and soft key inputs.

In addition, the iPLDS II contains programmer hardware in the form of an iUP-PC Universal Programmer-Personal Computer to enable the user to program EPLDs, read and verify programmed devices and also to graphically edit programming files. The software generates industry standard JEDEC object code output files which can be downloaded to other programmers as well.

The iPLDS II has interfaces to popular schematic capture packages to enable designs to be entered using schematics. One low-cost schematic entry method is provided by SCHEMA II-PLD, which supports EPLD primitives and user-defined macro symbols. SCHEMA II-PLD contains the EPLD Design Manager, which provides a single user interface to both SCHEMA II-PLD and iPLS II software. The other design formats supported are Boolean equation entry and State Machine design entry.

The iPLDS II operates on the IBM† PC.XT, PC/AT, or other compatible machine with the following configuration:

1. At least one floppy disk drive and hard disk drive.
2. MS-DOS†† Operation System Version 3.0 or greater.
3. 512K Memory.
4. Intel iUP-PC Universal Programmer-Personal Computer
5. A GUPI LOGIC Adaptor
6. A color monitor is suggested.

Detailed information on the Intel Programmable Logic Developement System is contained in a separate Intel data sheet.

†IBM Personal Computer is a registered trademark of International Business Machines Corporation.

††MS-DOS is a registered trademark of Microsoft Corporation.