19-0130; Rev 1; 4/94

MAXIM

Low-Cost µP Supervisory Circuits with Battery Backup

General Description

The MAX703 and MAX704 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

1) An active-low reset during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µPs, or other low-power logic circuitry.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

The MAX703 and MAX704 differ only in their supply-voltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.4V.

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

- ♦ **Battery-Backup Power Switching**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V (MAX703)
  4.40V (MAX704)
- ♦ **200ms Reset Pulse Width**
- ♦ **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- ♦ **200µA Quiescent Current**
- ♦ **50nA Quiescent Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **8-Pin DIP and SO Packages**
- ♦ **Guaranteed $\overline{RESET}$ Assertion to V_{CC} = 1V**

Ordering Information

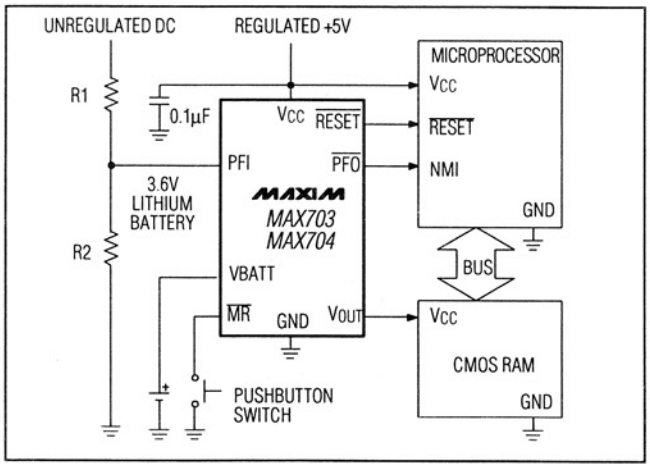
PART	TEMP. RANGE	PIN-PACKAGE
MAX703CPA	0°C to +70°C	8 Plastic DIP
MAX703CSA	0°C to +70°C	8 SO
MAX703C/D	0°C to +70°C	Dice*
MAX703EPA	-40°C to +85°C	8 Plastic DIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

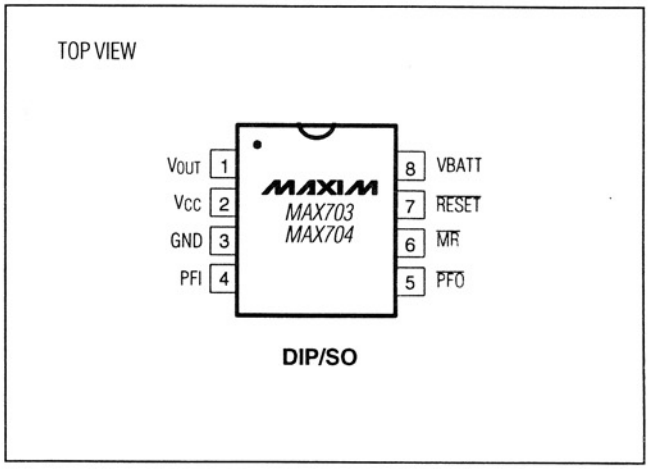
** Dice are tested at T_A = +25°C only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



Low-Cost µP Supervisory Circuits with Battery Backup

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- VBATT ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CB} + 0.3V)

Input Current
- V_{CC} 200mA
- VBATT 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10 sec
- All Other Outputs 20mA

Rate-of-Rise, V_{CC}, VBATT 100V/µs

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C__ ..... 0°C to +70°C
- MAX70_E__ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: V_{CB} is the greater of V_{CC} and VBATT. The input voltage limits on PFI and $\overline{MR}$ may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOLS	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, VBATT (Note 2)				0		5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX70_C			200	350	µA
		MAX70_E/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, VBATT = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A= T_{MIN} to T_{MAX}			5.0	
VBATT Standby Current (Note 3)		5.5V> V_{CC} > VBATT + 0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A=T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC}-0.05	V_{CC}-0.025		V
		I_{OUT} = 50mA		V_{CC}-0.5	V_{CC}-0.25		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT}-0.2V		VBATT-0.1	VBATT-0.02		V
Battery-Switch Threshold (V_{CC} - VBATT)		V_{CC} < V_{RST}	Power-Up		20		mV
			Power-Down		-20		
Battery-Switchover Hysteresis					40		mV
$\overline{RESET}$ Threshold	V_{RST}	MAX703		4.50	4.65	4.75	V
		MAX704		4.25	4.40	4.50	
$\overline{RESET}$ Threshold Hysteresis					40		mV
$\overline{RESET}$ Pulse Width	t_{RST}			140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA		V_{CC}-1.5			V
	V_{OL}	I_{SINK} = 3.2mA				0.4	
		MAX70_C, V_{CC} = 1V, V_{CC} falling, VBATT = 0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M, V_{CC} = 1.2V, V_{CC} falling, VBATT = 0V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOLS	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Input Threshold Low	V_{IL}				0.8	V
High	V_{IH}		2.0			
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ to $\overline{RESET}$ Delay	t_{MD}				250	ns
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	100	250	600	µA
PFI Input Threshold		V_{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current			-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA	V_{CC}-1.5			V
	V_{OL}	I_{SINK} = 3.2mA			0.4	

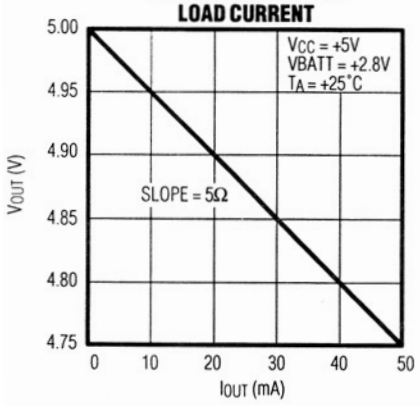
Note 2: Either V_{CC} or VBATT can go to 0V if the other is greater than 2.0V.

Note 3: "-" = battery-charging current, "+" = battery-discharging current.

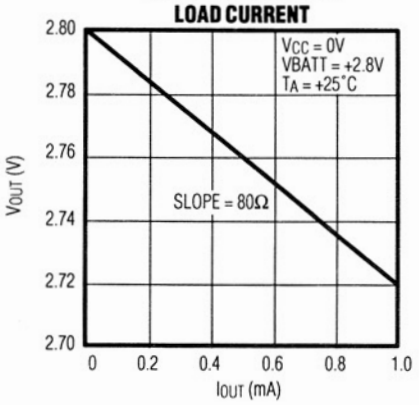
Typical Operating Characteristics

(V_{CC} = +5V, VBATT = +2.8V, T_A = +25°C, unless otherwise noted.)

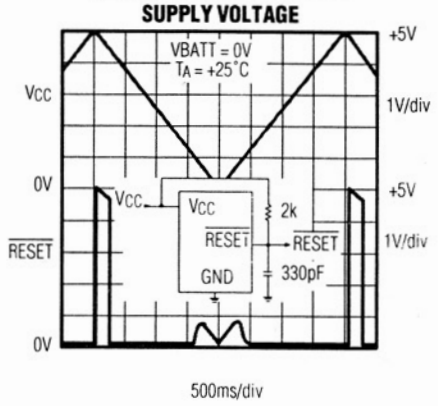
OUTPUT VOLTAGE vs. LOAD CURRENT



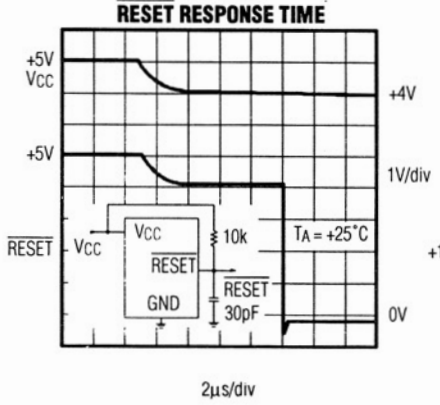
OUTPUT VOLTAGE vs. LOAD CURRENT



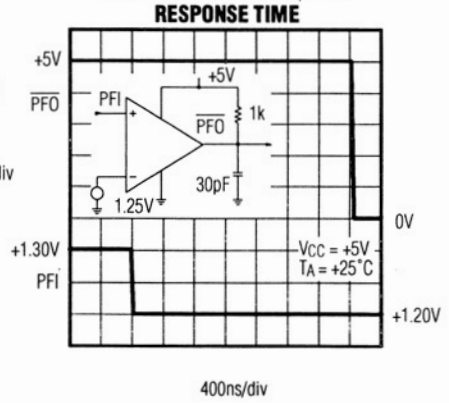
MAX703 $\overline{RESET}$ OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



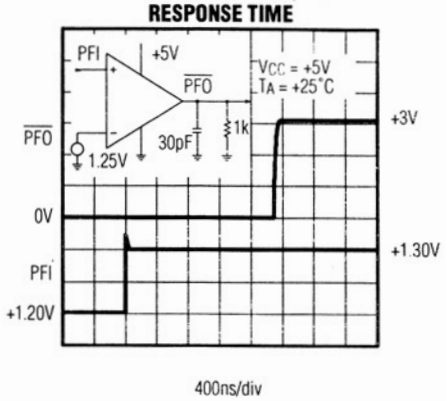
MAX703 $\overline{RESET}$ RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



Low-Cost µP Supervisory Circuits with Battery Backup

Pin Description

PIN	NAME	FUNCTION
1	VOUT	Supply Output for CMOS RAM. When VCC is above the reset threshold, VOUT connects to VCC through a P-channel MOSFET switch. When VCC is below the reset threshold, the higher of VCC or VBATT is connected to VOUT.
2	VCC	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND or VCC when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ remains high.
6	$\overline{MR}$	Manual-Reset Input generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250µA pull-up current. Leave floating when not used.
7	$\overline{RESET}$	Reset Output remains low while VCC is below the reset threshold (4.65V for the MAX703, 4.40V for the MAX704). It remains low for 200ms after VCC rises above the reset threshold (Figure 2) or MR goes from low to high.
8	VBATT	Backup-Battery Input. When VCC falls below the reset threshold, VBATT is switched to VOUT if VBATT is 20mV greater than VCC. When VCC rises 20mV above VBATT, VCC is switched to VOUT. The 40mV hysteresis prevents repeated switching if VCC falls slowly.

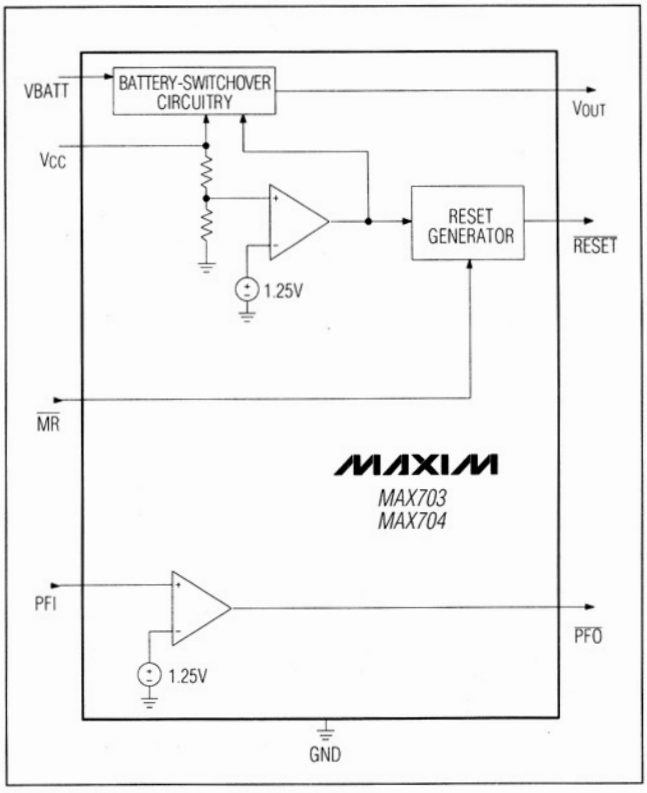


Figure 1. Block Diagram

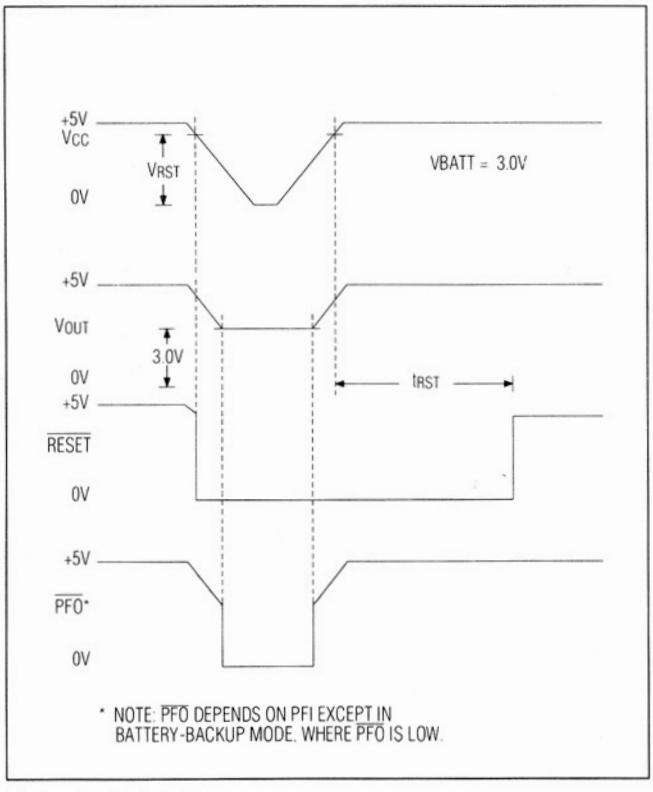


Figure 2. Timing Diagram

Detailed Description

RESET Output

A µP's reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX703/MAX704 assert reset when VCC is low, preventing code-execution errors during power-up, power-down, or brownout conditions.

When VBATT is 2V or more, RESET is always valid, irrespective of VCC. On power-up, as VCC rises, RESET remains low. When VCC exceeds the reset threshold, an internal timer holds RESET low for a time equal to the reset pulse width (typically 200ms); after this interval, RESET goes high (Figure 2). If a power-fail or brownout condition occurs (i.e. VCC drops below the reset threshold), RESET is asserted. As long as VCC remains below the reset threshold, the internal timer is continually restarted, causing the RESET output to remain low. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the end of the last interruption.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than 1.25V, PFO goes low. The power-fail comparator can be used as an undervoltage detector to signal a failing power supply. In the *Typical Operating Circuit*, an external voltage divider at PFI is used to monitor the unregulated DC voltage from which the regulated +5V supply is derived.

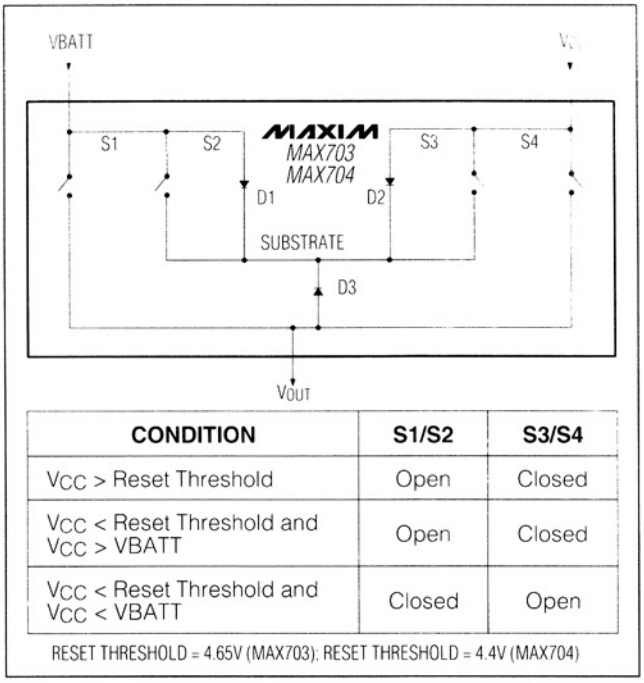
The voltage divider can be chosen so the voltage at PFI falls below 1.25V just before the +5V regulator drops out. PFO is then used as an interrupt to prepare the µP for power-down.

To conserve power, the power-fail comparator is turned off and PFO is forced low when the MAX703/MAX704 enter battery-backup mode.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at VBATT, the MAX703/MAX704 automatically switch RAM to backup power when VCC fails.

As long as VCC exceeds the reset threshold, VCC connects to VOUT through a 5Ω P-channel MOSFET power switch. Once VCC falls below the reset threshold, RESET goes low and VCC or VBATT (whichever is higher) switches to VOUT. Note that VBATT switches to VOUT (through an 80Ω switch) only if VCC is below the reset-threshold voltage **and** VBATT is greater than VCC. When VCC exceeds the reset threshold, it is connected to the MAX703/MAX704 substrate, regardless of the voltage



CONDITION	S1/S2	S3/S4
VCC > Reset Threshold	Open	Closed
VCC < Reset Threshold and VCC > VBATT	Open	Closed
VCC < Reset Threshold and VCC < VBATT	Closed	Open

RESET THRESHOLD = 4.65V (MAX703); RESET THRESHOLD = 4.4V (MAX704)

Figure 3. Backup-Battery Switchover Block Diagram

applied to VBATT (Figure 3). During this time, diode D1 (between VBATT and the substrate) conducts current from VBATT to VCC if VBATT ≥ (VCC + 0.6V).

When the battery-backup mode is activated, VBATT connects to VOUT. In this mode, the substrate connects to VBATT and internal circuitry is powered from the battery (Figure 3). Table 1 shows the status of the MAX703/MAX704 inputs and outputs in battery-backup mode.

When VCC is below, but within, 1V of VBATT, the internal switchover comparator draws about 30µA. Once VCC drops to more than 1V below VBATT, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
VCC	Disconnected from VOUT.
VOUT	Connected to VBATT through an internal 80Ω P-channel MOSFET switch.
VBATT	Connected to VOUT. Supply current is < 1µA when VCC < (VBATT - 1V).
RESET	Logic low
PFI	Power-fail comparator is disabled.
PFO	Logic low
MR	Disabled

Low-Cost µP Supervisory Circuits with Battery Backup

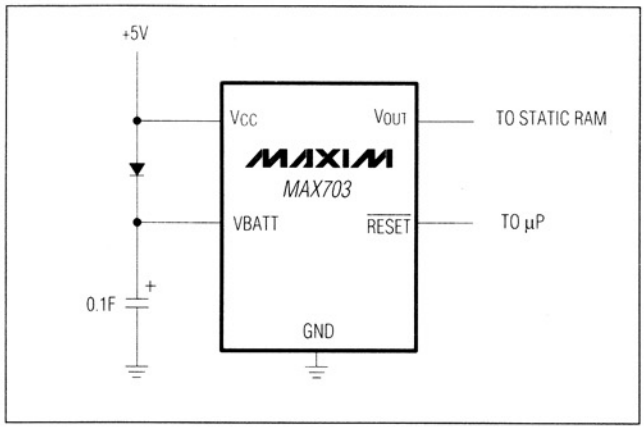


Figure 4. Using a SuperCap as a Backup Power Source with a MAX703 and a +5V ±5% Supply

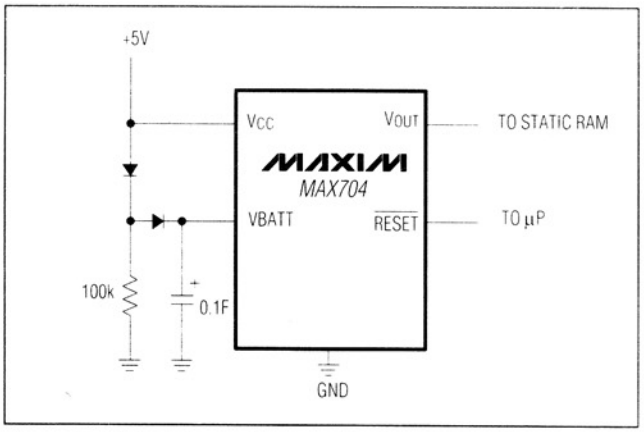


Figure 5. Using a SuperCap as a Backup Power Source with the MAX704 and a +5V ± 10% Supply

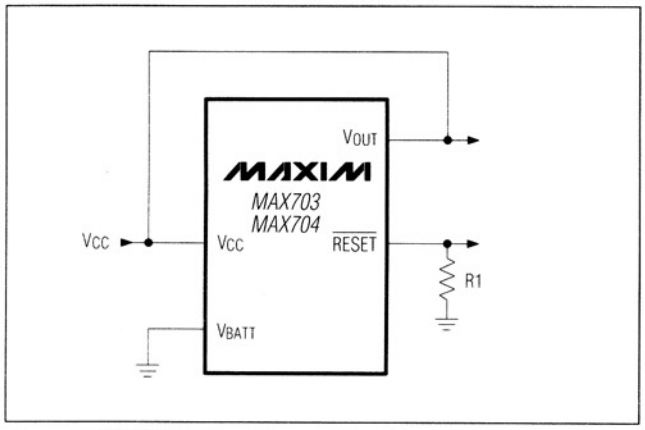


Figure 6. $\overline{RESET}$ Valid to Ground Circuit

Manual Reset

The manual-reset input ($\overline{MR}$) allows $\overline{RESET}$ to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. Because it is TTL/CMOS compatible, $\overline{MR}$ can be driven by an external logic line.

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.1 Farad). When using SuperCaps, if Vcc exceeds the MAX703/MAX704 reset thresholds (4.65V and 4.40V, respectively), VBATT may not exceed VCC by more than 0.6V. Thus, with a 5% tolerance on VCC, VBATT should not exceed VCC (min) + 0.6V = 5.35V. Similarly, with a 10% tolerance on VCC, VBATT should not exceed 5.1V.

Figure 4's SuperCap circuit uses the MAX703 with a ±5% tolerance voltage supply. In this circuit, the SuperCap rapidly charges to within a diode drop of VCC. However, the diode leakage current will trickle-charge the SuperCap voltage to VCC. If VBATT = 5.25V and the power is suddenly removed and then reapplied with VCC = 4.75V, VBATT - VCC does not exceed the allowable 0.6V difference voltage.

Figure 5's circuit uses the MAX704 with a ±10% tolerance voltage supply. Note that if VCC = 5.5V and VBATT ≤ 5.1V, the power can be suddenly removed and reapplied with VCC = 4.5V, and (VBATT - VCC) will not exceed the allowable 0.6V voltage difference.

Batteries and Power Supplies as Backup Power Sources

Lithium batteries work well as backup batteries because they have very low self-discharge rates and high-energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal for use with the MAX703/MAX704. Batteries with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be directly connected to the MAX703/MAX704 VBATT input with no additional circuitry (see *Typical Operating Circuit*).

However, batteries with open-circuit voltages greater than the reset threshold plus 0.3V CANNOT be used as backup batteries, since they source current into the substrate through diode D1 (Figure 3) when VCC is close to the reset threshold.

Table 2. Allowable Backup-Battery Voltages

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX703	4.80
MAX704	4.55

™ Supercap is a registered trademark of Baknor Industries.

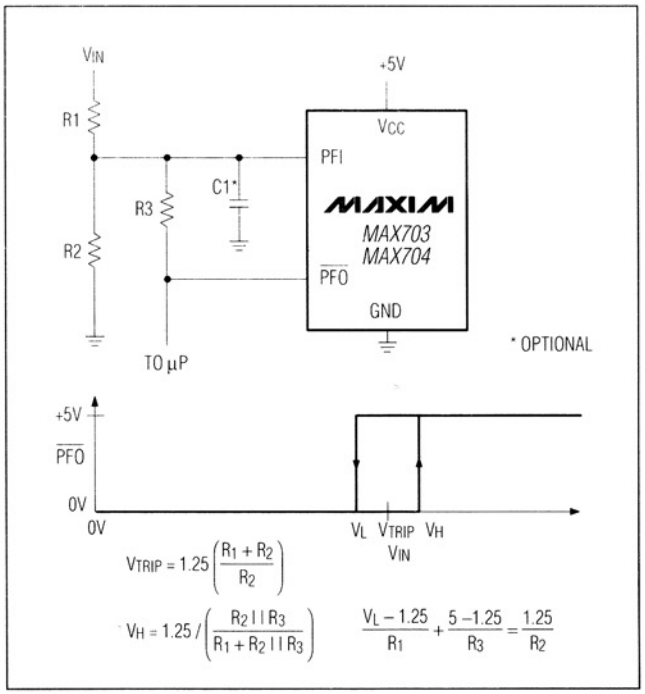


Figure 7. Adding Hysteresis to the Power-Fail Comparator

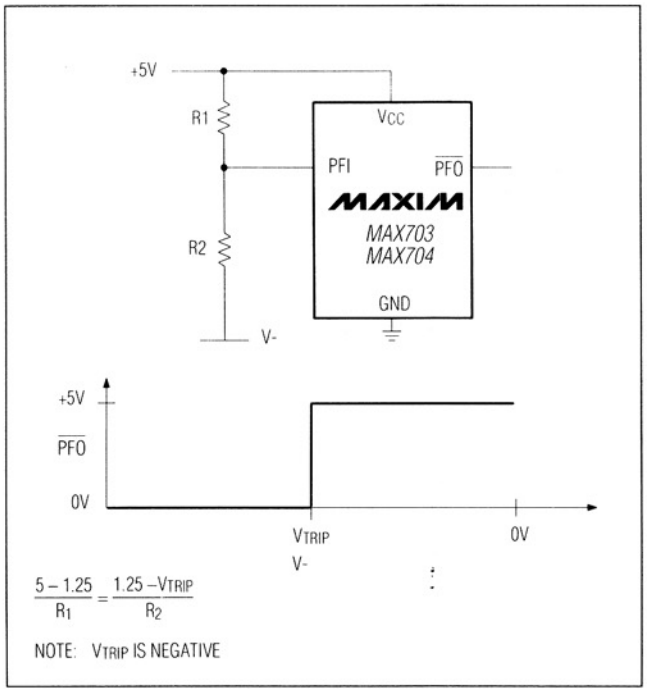


Figure 8. Monitoring a Negative Voltage

Using the MAX703/MAX704 Without a Backup Power Source

If a backup power source is not used, ground VBATT and connect VCC to VOUT. A direct connection to VCC eliminates any voltage drop across the internal switch, which would otherwise appear at VOUT. Alternatively, use the MAX705-MAX708, which do not have battery-backup capabilities.

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When VCC falls below 1V, the MAX703/MAX704 $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the $\overline{RESET}$ pin as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding $\overline{RESET}$ low. Resistor value R1 is not critical. It should be about 100kΩ, which is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

Replacing the Backup Battery

The backup battery can be removed while VCC remains valid without triggering a reset. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered. This is an improvement on switchover ICs that initiate a reset when VCC and VBATT are at or near the same voltage level (regardless of the reset-threshold voltage). If the voltage on the unconnected VBATT pin floats up toward VCC, this condition alone cannot initiate a reset when using the MAX703/MAX704.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 8's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

Low-Cost µP Supervisory Circuits with Battery Backup

Using the Power-Fail Comparator to Assert Reset

In addition to asserting reset at the VCC reset threshold voltage, reset can also be asserted at the PFI input threshold voltage. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a reset pulse when the monitored supply drops below a user-specified threshold or when VCC falls below the reset threshold. For additional noise rejection, place a capacitor between PFI and GND.

Table 3. Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/ 1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

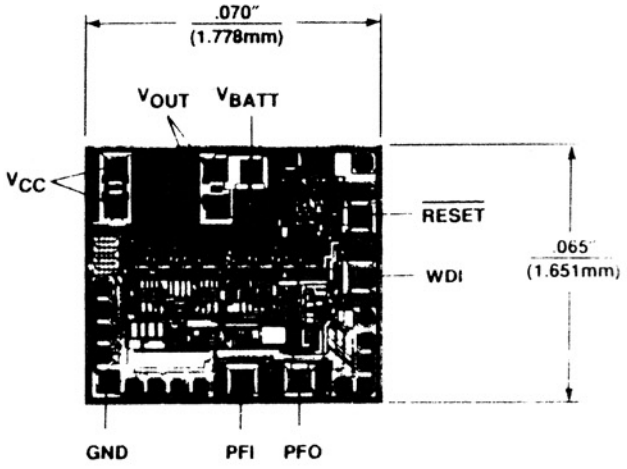
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX704CPA	0°C to +70°C	8 Plastic DIP
MAX704CSA	0°C to +70°C	8 SO
MAX704C/D	0°C to +70°C	Dice*
MAX704EPA	-40°C to +85°C	8 Plastic DIP
MAX704ESA	-40°C to +85°C	8 SO
MAX704MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



SUBSTRATE MUST BE LEFT UNCONNECTED
TRANSISTOR COUNT: 573