2.5 Gbits/s transimpedance amplifier CGY2100

FEATURES

- Suitable for 2.5 Gbits/s optical fibre links
- 30 dB gain (36 dB differential)
- Low noise (8 pA/√Hz)
- High bandwidth (up to 2.8 GHz)
- Bandwidth adjustment input
- Differential outputs
- Single voltage supply operation possible
- Available in a LQFP48 plastic package
- Also available in die form.

APPLICATIONS

- Digital fibre optic receiver for optical telecommunications (e.g. OC-48, STM-16 systems)
- High sensitivity and high gain amplifier.

GENERAL DESCRIPTION

The CGY2100 is a GaAs Monolithic Microwave Integrated Circuits (MMIC) transimpedance amplifier. Typical applications include low noise preamplification in lightwave receiver modules at 2.5 Gbits/s data bit rates. The device is suitable for use as a high sensitivity and high gain preamplifier for frequencies up to 2.8 GHz, and data bit rates up to 3.5 Gbits/s.

The CGY2100 features differential outputs, as well as a bandwidth adjustment input. The device uses a 5 V positive supply voltage and a low current consumption negative supply voltage. Single positive supply voltage operation is also possible.

The device is fabricated using the Philips Microwave Limeil ER05AD Enhancement-Depletion mode standard process. This circuit is available both as a plastic packaged chip (CGY2100HL) and also in die form (CGY2100UH).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2100HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
CGY2100UH		GaAs Semiconductor die. External dimensions = 2.17 × 1.42 mm (tolerance = ±0.01 mm); die thickness = 0.2 mm. Backside material: GaAs.	

BLOCK DIAGRAM

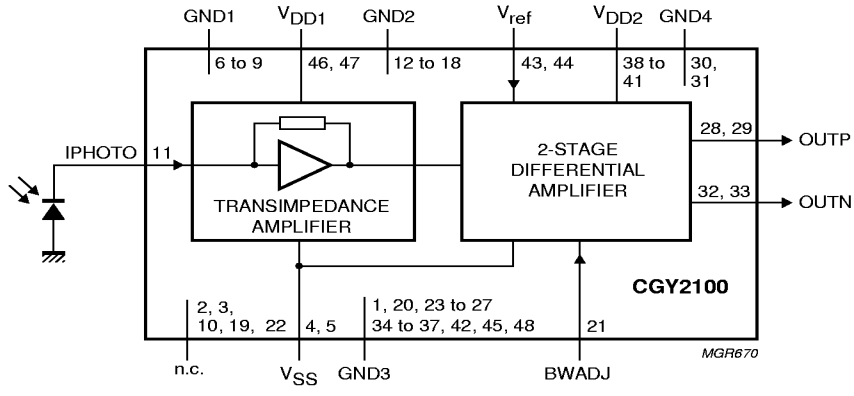


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND3	1	ground 3 (connected to die pad)
n.c.	2	not connected
n.c.	3	not connected
V_{SS}	4	negative supply voltage or connected to ground for single supply operation
V_{SS}	5	negative supply voltage or connected to ground for single supply operation
GND1	6	ground 1 for the first transimpedance stage
GND1	7	ground 1 for the first transimpedance stage
GND1	8	ground 1 for the first transimpedance stage
GND1	9	ground 1 for the first transimpedance stage
n.c.	10	not connected
IPHOTO	11	photo current input
GND2	12	ground 2 for the first transimpedance stage
GND2	13	ground 2 for the first transimpedance stage
GND2	14	ground 2 for the first transimpedance stage
GND2	15	ground 2 for the first transimpedance stage
GND2	16	ground 2 for the first transimpedance stage
GND2	17	ground 2 for the first transimpedance stage
GND2	18	ground 2 for the first transimpedance stage
n.c.	19	not connected
GND3	20	ground 3 (connected to die pad)
BWADJ	21	bandwidth adjustment input
n.c.	22	not connected
GND3	23	ground 3 (connected to die pad)
GND3	24	ground 3 (connected to die pad)
GND3	25	ground 3 (connected to die pad)
GND3	26	ground 3 (connected to die pad)
GND3	27	ground 3 (connected to die pad)
OUTP	28	complementary non-inverting output
OUTP	29	complementary non-inverting output
GND4	30	ground 4 for the output stage
GND4	31	ground 4 for the output stage
OUTN	32	complementary inverting output
OUTN	33	complementary inverting output
GND3	34	ground 3 (connected to die pad)
GND3	35	ground 3 (connected to die pad)
GND3	36	ground 3 (connected to die pad)
GND3	37	ground 3 (connected to die pad)
V_{DD2B}	38	positive supply voltage for the 1st stage of the differential amplifier
V_{DD2B}	39	positive supply voltage for the 1st stage of the differential amplifier
V_{DD2A}	40	positive supply voltage for the 2nd stage of the differential amplifier

SYMBOL	PIN	DESCRIPTION
V_{DD2A}	41	positive supply voltage for the 2nd stage of the differential amplifier
GND3	42	ground 3 (connected to die pad)
V_{ref}	43	reference voltage input for the differential amplifier stage (must be externally decoupled)
V_{ref}	44	reference voltage input for the differential amplifier stage (must be externally decoupled)
GND3	45	ground 3 (connected to die pad)
V_{DD1}	46	positive supply voltage for the transimpedance stage
V_{DD1}	47	positive supply voltage for the transimpedance stage
GND3	48	ground 3 (connected to die pad)

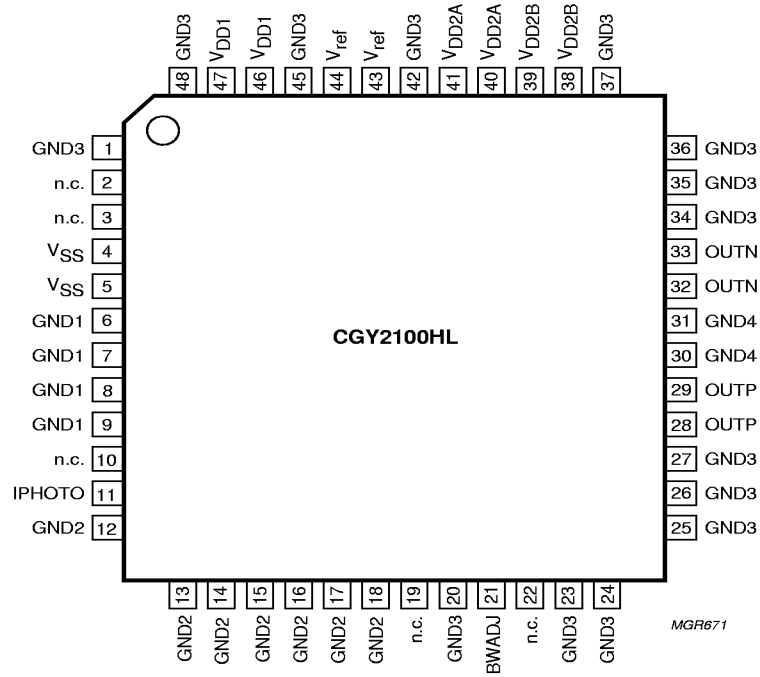


Fig.2 Pin configuration (CGY2100HL).

BONDING PAD LOCATIONS

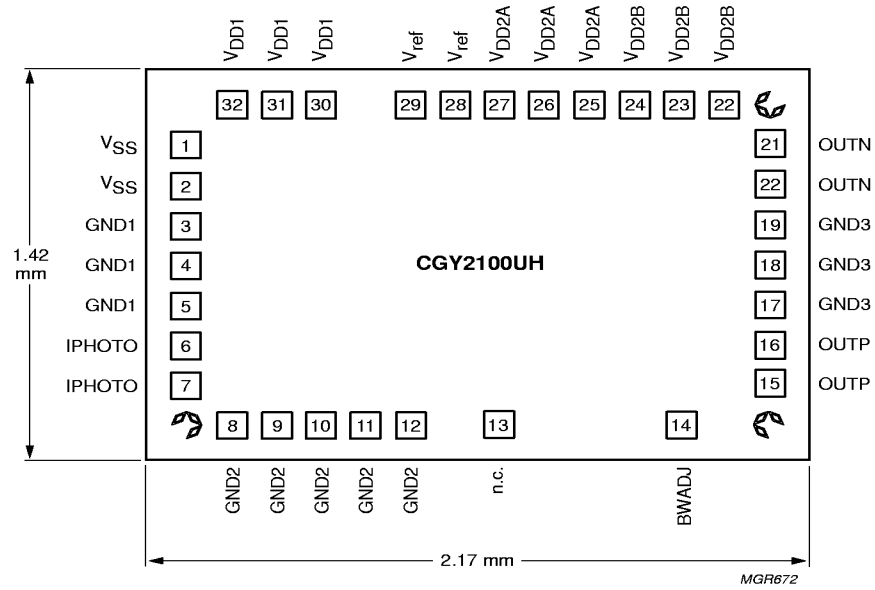


Fig.3 Bonding pad locations (CGY2100UH).

PAD POSITION (CGY2100UH)

SYMBOL	PADS[1]	DESCRIPTION
V_{SS}	1 and 2	negative supply voltage or connected to ground for single supply operation
GND1	3, 4 and 5	ground 1 for the first transimpedance stage
IPHOTO	6 and 7	photo current input
GND2	8 to 12	ground 2 for the first transimpedance stage
n.c.	13	not connected
BWADJ	14	bandwidth adjustment input; see note 2
OUTP	15 and 16	complementary non-inverting output
GND3	17, 18 and 19	ground for the output stage
OUTN	20 and 21	complementary inverting output
V_{DD2B}	22, 23 and 24	positive power supply for the first stage
V_{DD2A}	25, 26 and 27	positive power supply for the second stage
V_{ref}	28 and 29	offset-control input
V_{DD1}	30, 31 and 32	positive power supply for the first transimpedance stage

Notes

1. For each symbol indicated in this table, at least one pad from the corresponding pad list must be wired.
2. BWADJ input: if this input is not needed in the application, the pad may be left unconnected.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage (V_{DD1} and V_{DD2})	–	6.5	V
V_{SS}	negative supply voltage	−6	0	V
$I_{IPHOTO(p-p)}$	input photo current (peak-to-peak value)	–	2.5	mA
T_{amb}	ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−55	+150	°C
T_{ch}	maximum operating channel temperature	–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	30	K/W

DC CHARACTERISTICS

T_{amb} = 25 °C; V_{DD1} = V_{DD2} = 5.0 V; V_{SS} = −4.5 V (dual supply mode); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (V_{DD1} and V_{DD2})		4.5	5.0	5.5	V
V_{SS}	negative supply voltage		−5.5	−4.5	−1.5	V
I_{DD}	positive supply current		59	76	85	mA
		V_{SS} connected to ground; single supply mode	56	73	82	mA
I_{SS}	negative supply current		8	11	15	mA
		V_{SS} connected to ground; single supply mode	2.5	3.5	5	mA
P_{DC}	DC power consumption		331	430	493	mW
		V_{SS} connected to ground; single supply mode	280	365	410	mW
$I_{fwd(max)}$	maximum forward PHOTO current before input overload	note 1	–	2.5	–	mA
$I_{rev(max)}$	maximum reverse PHOTO current before input overload;	note 1	–	0.5	–	mA
$\Delta V_{IPHOTO}/T$	V_{IPHOTO} change over temperature	T_{amb} = −20 to +70 °C	–	0.05	–	V

Note

1. As illustrated in Figs 1 and 11, the forward PHOTO current is assumed to flow from the inside towards the outside of the IC, whereas reverse PHOTO current is assumed to flow from the outside towards the inside of the IC.

INTERNAL DC CHARACTERISTICS

Once the CGY2100 is biased by V_{DD1}, V_{DD2} and V_{SS} (T_{amb} = 25 °C; V_{DD1} = V_{DD2} = 5.0 V; V_{SS} = –4.5 V); the following voltages are automatically set to the internal values specified below. The value of V_{BWADJ} may be externally controlled to perform the bandwidth adjustments.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BWADJ}	internal default bandwidth adjustment voltage	not connected	4.5	4.7	5.0	V
$V_{ref(int)}$	internal reference voltage	DC-decoupled; see Fig.12	1.8	2.1	2.2	V
V_{IPHOTO}	DC input voltage (pin 11)	DC-decoupled	0.4	0.5	0.6	V
V_{OUTP}	DC output voltage (pins 28 and 29)	DC-decoupled; see Fig.12	3.3	3.5	3.8	V
V_{OUTN}	DC output voltage (pins 32 and 33)	DC-decoupled; see Fig.12	3.3	3.5	3.8	V

AC CHARACTERISTICS (DUAL SUPPLY MODE)

T_{amb} = 25 °C; V_{DD1} = V_{DD2} = 5.0 V; V_{SS} = –4.5 V; V_{BWADJ} = 0 V; 50 Ω system; input power = –40 dBm; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|S_{21}\|_{LF}$	low frequency gain	single-ended; f = 3 MHz	28	33	36	dB
$\|Z_{tr}\|_{LF(se)}$	low frequency transimpedance gain	single-ended; f = 3 MHz	62	67	70	dBΩ
$\|Z_{tr}\|_{LF(diff)}$	low frequency transimpedance gain	differential output; f = 3 MHz	68	73	76	dBΩ
f_{co}	cut-off frequency	$\|Z_{tr}\| = \|Z_{tr}\|_{LF} - 4$ dB; notes 1 and 2	2.2	2.8	3.5	GHz
$f_{co(min)}$	minimum cut-off frequency obtained by bandwidth adjustment function	V_{BWADJ} = 5 V; $\|Z_{tr}\| = \|Z_{tr}\|_{LF} - 4$ dB; notes 1 and 2	1.4	1.7	–	GHz
$\|Z_i\|_{(LF)(IPHOTO)}$	low frequency input impedance (pin IPHOTO)	f = 3 MHz	–	53	–	Ω
$VSWR_{in}$	voltage standing wave ratio input	f = 3 MHz; note 1	–	–	–20	dB
		f = 500 MHz; note 1	–	–	–15	dB
		f = 1 to 3 GHz; note 1	–	–	–10	dB
$\|Z_o\|_{LF}$	low frequency output impedance	f = 3 MHz	–	17	–	Ω
$\|Z_{tr(OUTN)}\| - \|Z_{tr(OUTP)}\|$	transimpedance output difference	f = 1.5 GHz; note 1	–	–	1	dBΩ
N_{eq}	equivalent input noise	f = 10 MHz	–	12	–	pA/√Hz
		f = 500 MHz to 1.5 GHz	–	8	10	pA/√Hz
		f = 350 MHz to 2 GHz	–	9	11	pA/√Hz

Notes

1. The transimpedance gain $|Z_{tr}|$, the input Voltage Standing Wave Ratio ($VSWR_{in}$) and the output transimpedance difference $|Z_{tr(OUTN)}| - |Z_{tr(OUTP)}|$ have a precise specification through frequency, which are illustrated in Figs 4, 5 and 6.
2. Using an output equalising filter such as described in Chapter “Test and application information”, the gain as a function of frequency response curve can be flattened and the cut-off frequency enhanced.

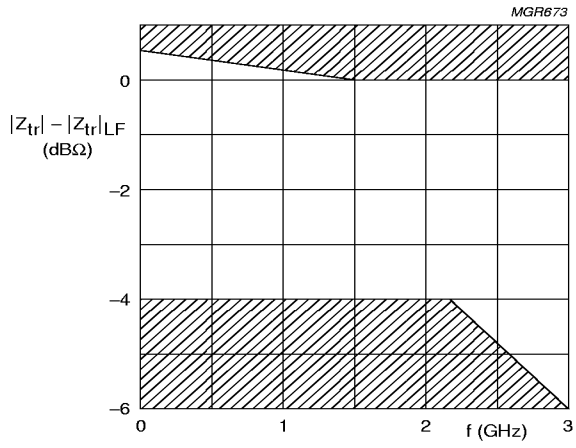
AC CHARACTERISTICS (SINGLE SUPPLY MODE)

T_{amb} = 25 °C; $V_{DD1} = V_{DD2}$ = 5.0 V; V_{SS} connected to ground; V_{BWADJ} = 0 V; 50 Ω system; input power = −40 dBm; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|S_{21}\|_{LF}$	low-frequency gain	single-ended; f = 3 MHz	26	31	34	dB
$\|Z_{tr}\|_{LF(se)}$	low-frequency transimpedance gain	single-ended; f = 3 MHz	60	65	68	dBΩ
$\|Z_{tr}\|_{LF(diff)}$	low-frequency transimpedance gain	differential output; f = 3 MHz	66	71	74	dBΩ
f_{co}	cut-off frequency	$\|Z_{tr}\| = \|Z_{tr}\|_{LF} - 4$ dB; note 1	2	2.5	–	GHz
$f_{co(min)}$	minimum cut-off frequency obtained by bandwidth adjustment function	V_{BWADJ} = 5 V; $\|Z_{tr}\| = \|Z_{tr}\|_{LF} - 4$ dB; note 1	1.3	1.5	–	GHz
$\|Z_i\|_{(LF)(IPHOTO)}$	low frequency IPHOTO input impedance	f = 3 MHz	–	53	–	Ω
$VSWR_{in}$	input standing wave ratio voltage	f = 3 MHz to 2.5 GHz	–	−14	–	dB
		f = 3 GHz	–	−10	–	dB
$\|Z_o\|_{LF}$	low frequency output impedance	f = 3 MHz	–	17	–	Ω
$\|Z_{tr(OUTN)}\| - \|Z_{tr(OUTP)}\|$	transimpedance output difference	f = 1.5 GHz	–	–	1	dBΩ
N_{eq}	equivalent input noise	f = 10 MHz	–	12	–	pA/√Hz
		f = 500 MHz to 1.5 GHz	–	8	10	pA/√Hz
		f = 350 MHz to 2 GHz	–	9	11	pA/√Hz

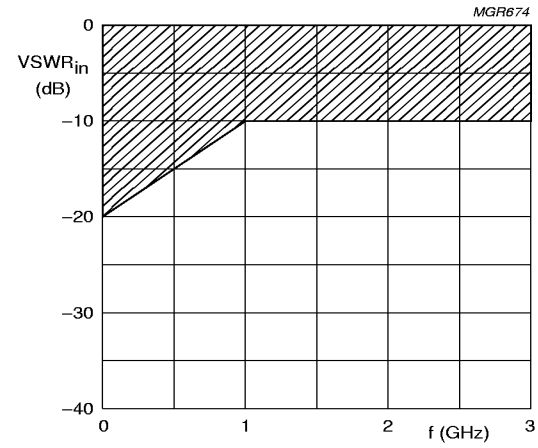
Note

1. Using an output equalising filter such as described in Chapter “Test and application information”, the gain as a function of frequency response curve can be flattened and the cut-off frequency enhanced.



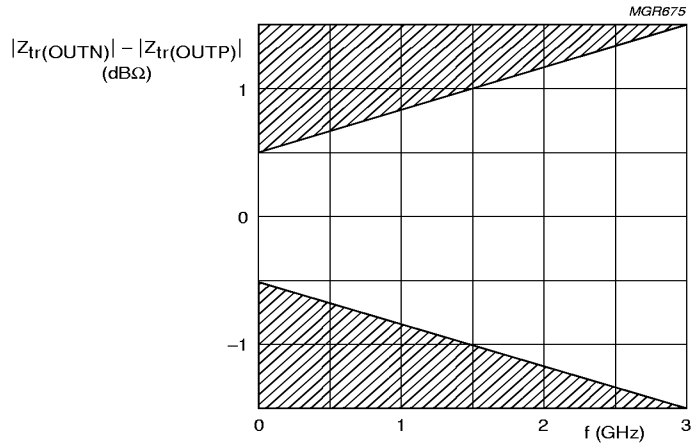
The hatched area indicates the limit of the test specification.

Fig.4 Specification for transimpedance as a function of frequency.



The hatched area indicates the limit of the test specification.

Fig.5 Specification for input standing wave ratio as a function of frequency.



The hatched area indicates the limit of the test specification.

Fig.6 Specification for transimpedance difference as a function of frequency.

TYPICAL PACKAGED PERFORMANCE (CGY2100HL)

The following measurements are made using the CGY2100HL production test set-up. The bandwidth was set to its maximum value (V_{BWADJ} = 0 V). If required, a flatter transimpedance gain may be obtained (as shown in Figs 14 and 15) using the output equalising filters shown in Figs 11 and 12.

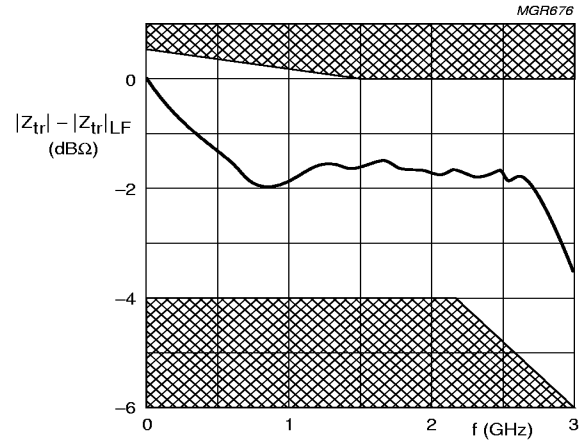


Fig.7 Transimpedance gain.

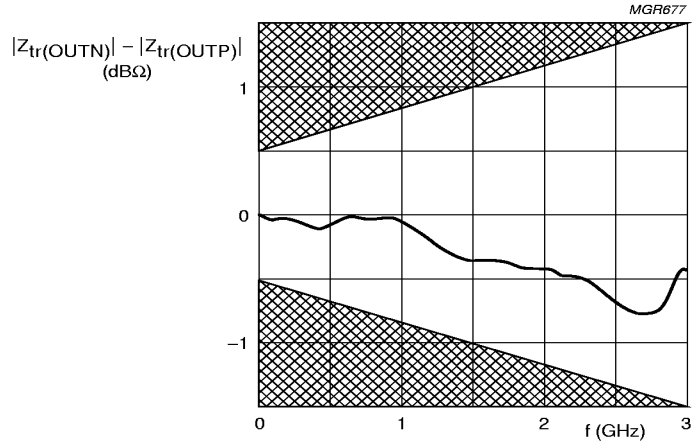


Fig.8 Output symmetry.

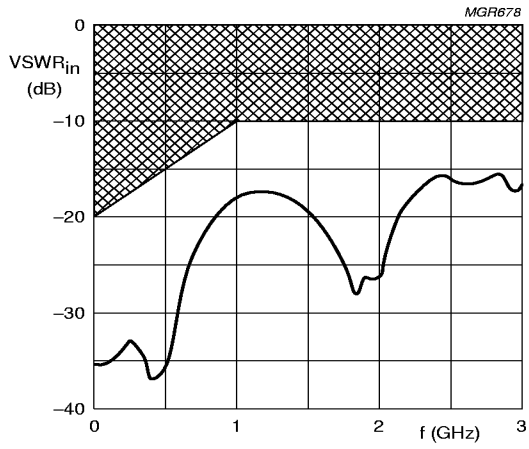


Fig.9 Input match.

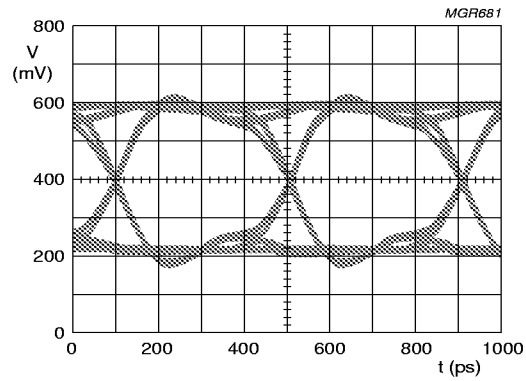


Fig.10 2.5 Gbits/s eye-diagram.

TEST AND APPLICATION INFORMATION

Typical application scheme (dual voltage supply)

The schematic diagram for a typical application is illustrated in Fig.11. The IC is DC-coupled to a photodiode and operated from the nominal V_{DD} = 5 V and V_{SS} = −4.5 V power supplies; a few decoupling capacitors and a dumping resistor are needed. The photodiode biasing voltage used in this application is negative. An electrical configuration using a positive photodiode biasing voltage may also be used, but then the maximum I_{PHOTO} value (overload) is smaller (see Chapter “DC characteristics”).

When the power supplies are turned on, the input is automatically self-biased to V_{IPHOTO}, which is approximately 0.5 V in nominal conditions (see Chapter “DC characteristics”). The voltage drop across the photodiode is then $\Delta V = |V_{bias} - V_{IPHOTO}|$.

An optional equalising filter made from a high-pass RC filter may be used at each output in order to flatten the gain curve; 18 Ω and 10 pF are typical values, which were optimized in order to flatten the gain above 1 GHz (with a 3 dB cut-off of the low frequency gain). These values can be optimized depending on the photodiode capacitance, the bandwidth and the application board layout. Tuning the resistance value allows the low frequency gain to be modified, whereas tuning the capacitance value (for a given resistance value) allows the gain flatness in the intermediate (around 1 GHz) frequency range to be tuned.

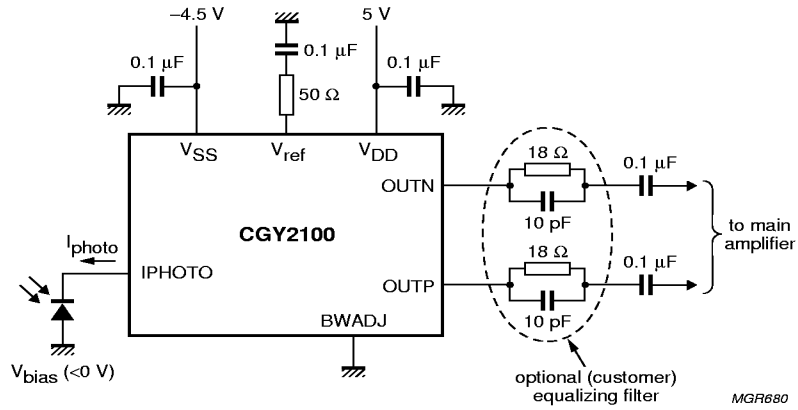


Fig.11 Schematic diagram for a dual supply application where the bandwidth is set to its maximum value (V_{BWADJ} = 0 V).

Typical application scheme (single voltage supply)

The schematic diagram for a typical application with a single voltage supply is illustrated in Fig.12. The V_{SS} pin (or pad) should be directly connected to ground; the 0.1 mF decoupling capacitor is no longer required.

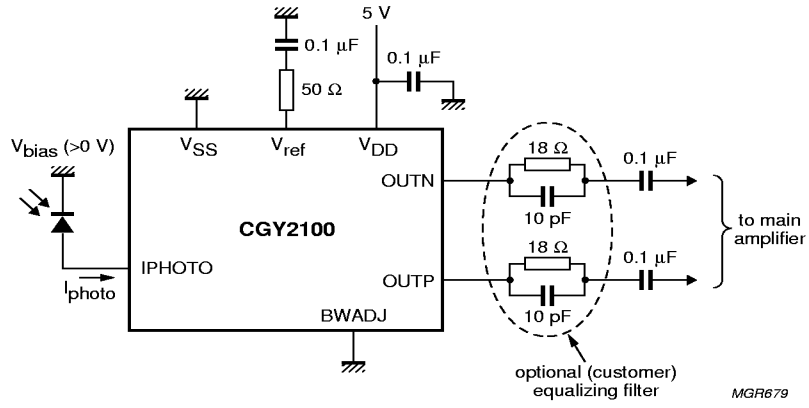


Fig.12 Schematic diagram for a single supply application where the bandwidth is set to its maximum value (V_{BWADJ} = 0 V).

Demonstration board (CGY2100HL)

A demonstration board (which does not include the photodiode) has been developed where Surface Mounted Assembly (SMA) connectors are used for the outputs and for IPHOTO input, while standard pins are used for the power supplies and adjustment inputs.

This demonstration board has been designed for easy use with S-parameter test set-ups. For this reason, the IPHOTO input of the demonstration board is AC-coupled. The PCB layout of the demonstration board is given in Fig.13.

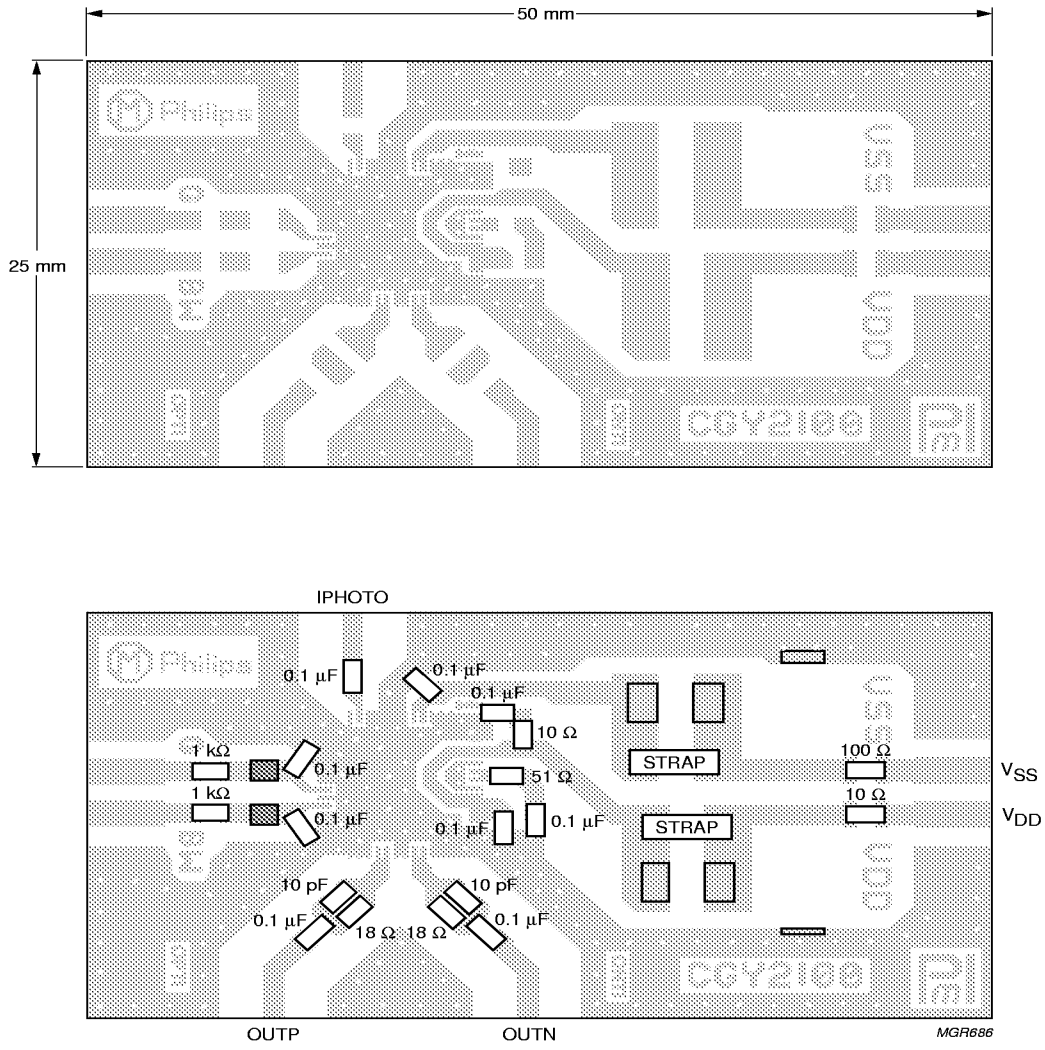


Fig.13 PCB layout of the CGY2100HL demonstration board (2.5×5 mm^2).

Typical results from the application board (CGY2100HL)

Figures 14 and 15 show the measured transimpedance gain and noise as a function of frequency. These measurements were performed under nominal conditions using the demonstration board shown in Fig.13, which includes output filtering. The bandwidth was set to its maximum value (V_{BWADJ} = 0 V).

Figures 16 and 17 show the measured eye diagrams for dual power supply and single positive supply voltage use. These measurements were performed under nominal conditions using the demonstration board shown in Fig.13, which includes output filtering. The bandwidth was set to its minimum value (V_{BWADJ} not connected).

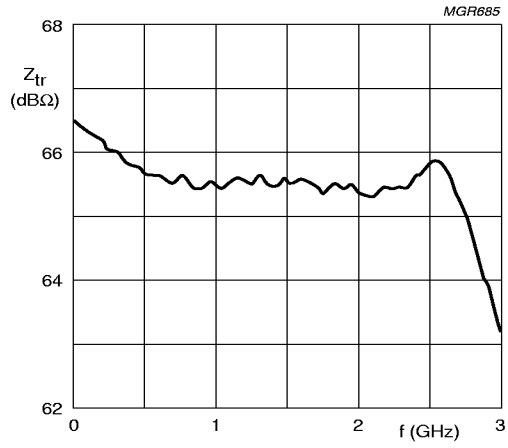


Fig.14 Transimpedance as a function of frequency.

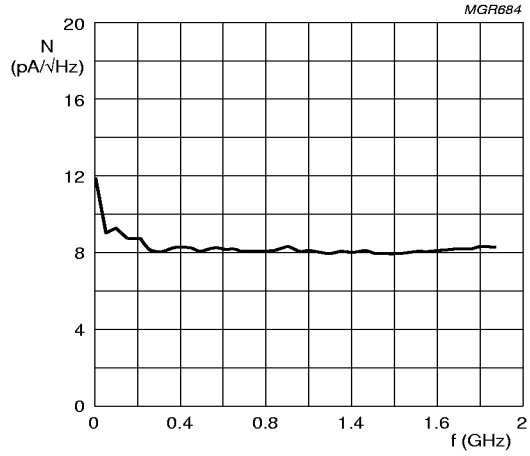


Fig.15 Noise response as a function of frequency.

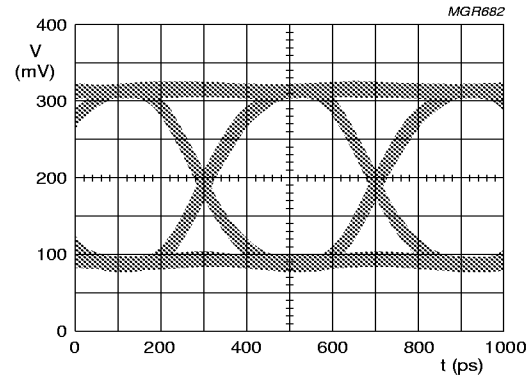


Fig.16 2.5 Gbits/s eye-diagram ($VSWR_{in}$ = −33 dB; single supply).

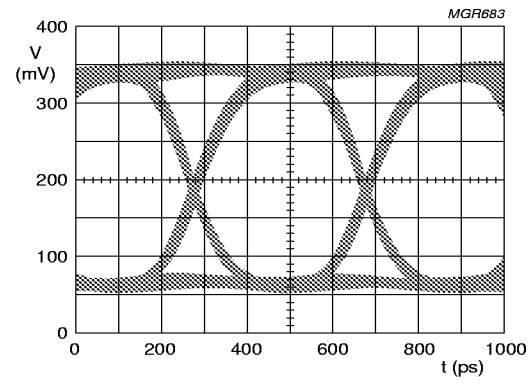
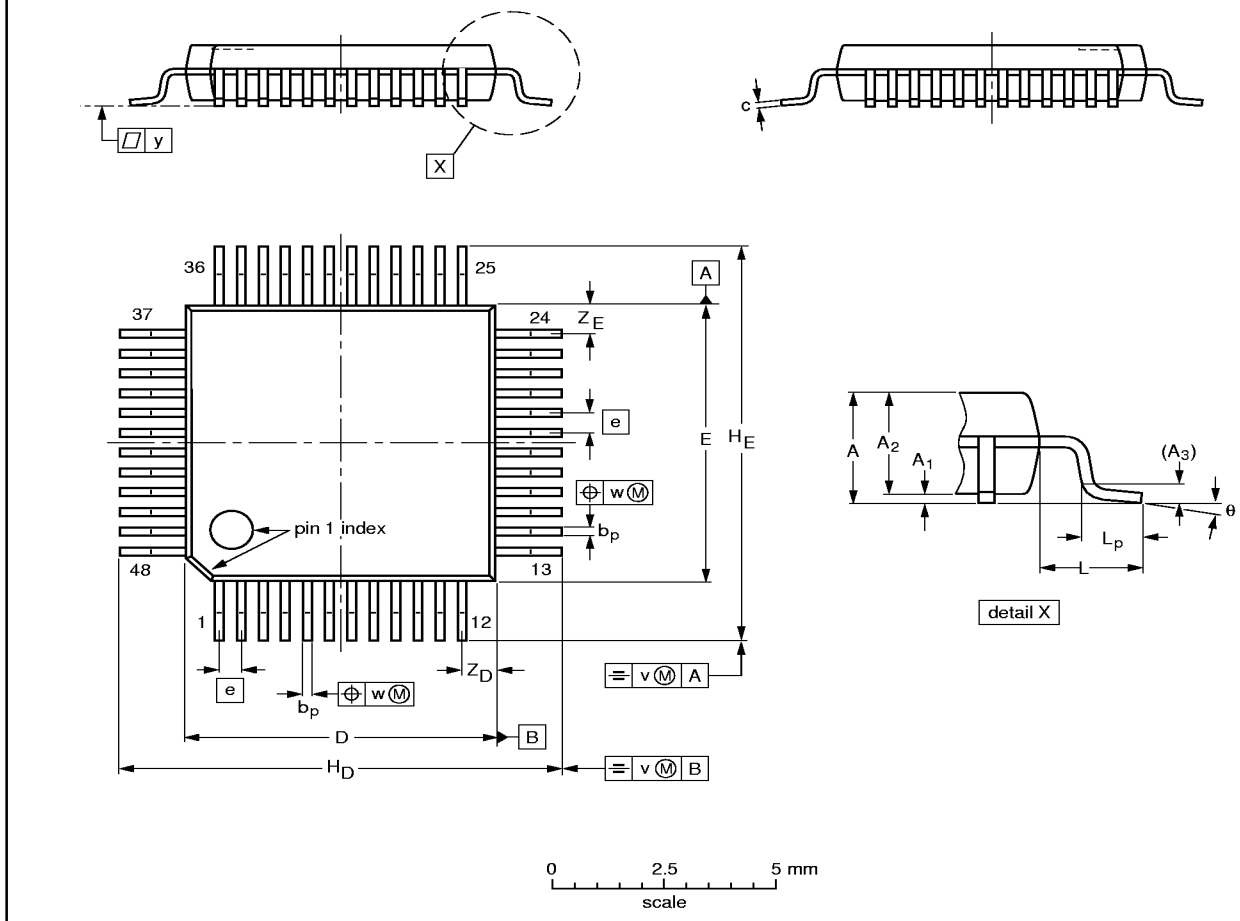


Fig.17 2.5 Gbits/s eye-diagram ($VSWR_{in}$ = −33 dB; dual supply).

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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