Getting Started Guide

Version 2.0

Xilinx® Virtex®-6 DSP Development Kit

AVNET® electronics marketing

Revision History

DATE	VERSION	REVISION
4/1/2010	1.0	Initial Release
10/20/2010	2.0	Update for ISE 12.3

AVNET DESIGN KIT TECHNICAL SUPPORT FILES AND DOWNLOADS WEB ACCESS INSTRUCTIONS

Thank you for purchasing an Avnet design kit. The technical support documents associated with this kit, including the User Guide, Bill of Materials, Schematics, Source Code and Application Notes, are available online. You, the Customer, can access these documents at any time by visiting Avnet's Design Resource Center ("DRC") at: www.em.avnet.com/drc/support

On your first visit to the DRC, You will be required to site register before you can download the documents. To get started, select the name of the manufacturer associated with your design kit from the drop down menu. A complete listing of avail¬able design kits will appear. Select the kit you purchased. Scroll to the bottom of the design kit page to access the support files. Before you download a file, you will be prompted to login. If you are an existing user, please login. If you are a new user, click on the "Need to sign-up?" text. Please complete the short registration form. Upon completion, be sure to retain your login and password information for future visits to Avnet's DRC. Logging in once, gives you unlimited access to all technical support files and downloads. You will also have the chance to request e-mail notifications whenever there are updates to your design kit.

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TABLE OF CONTENTS

ABOUT THIS GUIDE

This guide provides detailed information for getting started with the Xilinx Virtex®-6 FPGA DSP Kit. If the ISE® Design Suite: System Edition has already been installed and the steps in the Hardware Setup Guide has already been completed, proceed to the "Next Steps" section of this document to learn more about additional tutorials available for this kit. Otherwise, follow the steps outlined below to install and enable the required software for this kit.

Additional Documentation

The following documents are available for download at http://www.xilinx.com/products/virtex6.

- **Virtex-6 Family Overview:** This overview outlines the features and product selection of the Virtex-6 family.
- **Virtex-6 FPGA Data Sheet: DC and Switching Characteristics:** This data sheet contains the DC and switching characteristic specifications for the Virtex-6 family.
- **Virtex-6 FPGA Packaging and Pinout Specifications:** This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- **Virtex-6 FPGA Configuration User Guide:** This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
- **Virtex-6 FPGA SelectIO Resources User Guide:** This guide describes the SelectIO™ resources available in all Virtex-6 devices.
- **Virtex-6 FPGA Clocking Resources User Guide:** This guide describes the clocking resources available in all Virtex-6 devices, including the DCMs and PLLs.
- **Virtex-6 FPGA Block RAM Resources User Guide:** This guide describes the Virtex-6 device block RAM capabilities.
- **Virtex-6 FPGA GTP Transceivers User Guide:** This guide describes the GTP transceivers available in the Virtex-6 LXT FPGAs.
- **Virtex-6 FPGA DSP48E1 Slice User Guide:** This guide describes the architecture of the DSP48A1 slice in Virtex-6 FPGAs and provides configuration examples.
- **Virtex-6 FPGA PCB Designers Guide:** This guide provides information on the PCB design for Virtex-6 devices, with a focus on strategies for making design decisions at the PCB interface level.
- **System Generator Users Guide:** This guide provides information using System Generator with Simulink to create DSP designs to be targeted to Xilinx FPGAs.

Additional Support Resources

To search the database of silicon and software questions and answers or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

INTRODUCTION

The Virtex®-6 FPGA DSP Kit conveniently delivers the key components of the Xilinx DSP Design Platform required for developing DSP hardware in a wide range of applications in wireless communications, aerospace and defense, medical and instrumentation markets. For algorithm developers, a familiar DSP design flow is provided based on Simulink® and MATLAB® from Mathworks that allows for the creation of FPGA hardware without the need to learn RTL. Traditional RTL design methodologies are also supported through reference designs that use ISE® Design Suite: Logic Edition and LogicCORE DSP IP.

The Virtex-6 FPGA DSP Kit includes the FMC150 daughter card which is a dual channel A/D and dual channel D/A FMC daughter card. This card provides two 14-bit A/D channels and two 16-bit D/A channels which can be clocked by an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. In addition there is one trigger input for customized sampling control. The FMC150 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1).

This Getting Started Guide will walk you through the steps to setup the ML605 Virtex-6 Development Board and the FMC150 daughter card and run the out-of-box DSP demonstration which is designed to illustrate the hardware flexibility of FPGAs to deliver DSP processing bandwidth through parallelized hardware implementations on a single device. If you have not already installed the Xilinx ISE® software, you will be directed through the steps to install the software, get updates and generate a license. If you are planning to use or evaluate the Simulink-based design flow and do not already have Mathworks products installed you will be guided to the Mathworks web site. Finally this guide will provide hardware design tutorials for both Simulink and RTL design flows.

Virtex-6 DSP Development Kit Contents

What's Inside the Box

- ML605 Board with the XC6VLX240T-1FFG1156 FPGA along with:
  - Power Supply
  - One USB Type-A to Mini-B 5-pin cables
  - Ethernet cable
  - VGA to DVI Adapter
  - Compact Flash Card – 2 GB
- 4DSP FMC150 DAC/ADC Daughter Card with the following:
  - TI DAC3283, Dual-Channel 800 MSPS, 16-bit DAC
  - TI ADS62P49 Dual-Channel, 250 MSPS, 14-bit ADC
  - TI CDCE72010 Clock Distribution Device
- Xilinx ISE Design Suite 12.3 DVD which includes:
  - ISE Foundation with ISE Simulator
  - PlanAhead Design and Analysis Tool
  - Embedded Development Kit (EDK)
  - Xilinx Platform Studio (XPS)
  - Software Development Kit (SDK)
  - ChipScope™ Pro
  - System Generator for DSP®
- ISE Design Suite System Edition license voucher: (device-locked) for Virtex-6 LX240T FPGA
- Documentation
  - ML605 Hardware Setup Guide
  - Getting Started with the Virtex-6 FPGA DSP Kit
  - Virtex-6 FPGA DSP Kit Hardware Setup Guide
- Reference Designs
  - Getting Started Reference Design
  - System Generator Design Tutorial
  - RTL Design Tutorial

What's available online

- License for ISE Design Suite: System Edition
  - http://www.xilinx.com/getproduct
  - http://www.xilinx.com/tools/faq.htm
- Technical Support
  - http://xilinx.com/support
- Development Kit home page with Documentation and Reference Designs
  - http://www.xilinx.com/v6dspkit

If you already have ISE Design Suite installed on your computer then you can proceed directly to the the next section "GETTING STARTED WITH VIRTEX-6 DSP DEVELOPMENT". If you need to install ISE Design Suite then go to the section of this document titled "INSTALLATION AND LICENSING OF ISE DESIGN SUITE".

GETTING STARTED WITH VIRTEX-6 FPGA DSP DEVELOPMENT

This Virtex-6 FPGA DSP Kit comes with a DSP demonstration available as part of the web downloaded documentation package. You can run this demo after installing ISE Design Suite and Simulink to get an overview of the features of the ML605 board using the Simulink-based digital up converter (DUC) / digital down converter (DDC) reference design.

The DSP Reference Design Demonstration

The provided DSP demo uses a pre-built Virtex-6 FPGA design (shown in the figure below) with the following features:

- Integrated interfaces provided for the DAC, ADC and external clocking
- Parameterizable DSP IP to reduce development time and exploit device hardware resources such as the DSP48E1 slice
- Support for isolation of the digital and analog components of the design to assist with debug
- Includes ChipScope Pro to view results without external test equipment

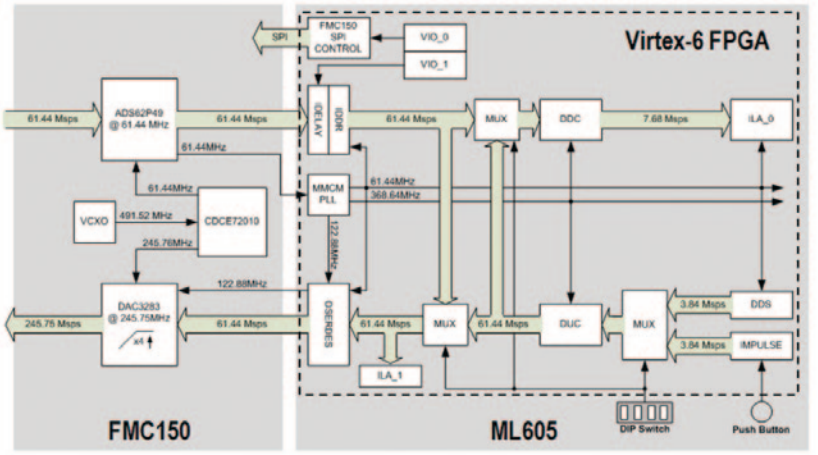

Figure 1: Virtex-6 Reference Design Block Diagram

DSP Demo Hardware Requirements

All hardware required to run the DSP demonstrations and tutorials are provided with the Virtex-6 FPGA DSP Kit.

DSP Demo Setup Instructions

1. Connect the FMC150 to the LPC FMC connector J63 on the ML605.

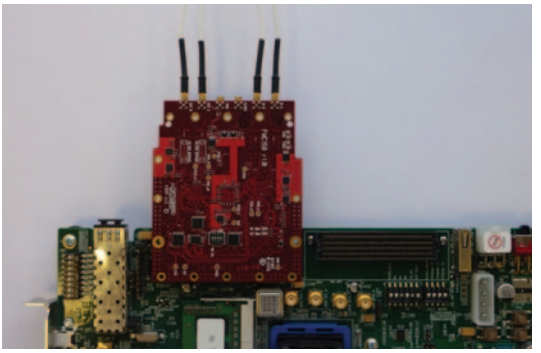

Figure 2

2. Connect DAC Output C to ADC Input A through an MMCX-to-MMCX cable on the FMC150 card. Make sure you use enough force to make a solid connection. You should hear a click.
3. Connect DAC Output D to ADC Input B through an MMCX-to-MMCX cable on the FMC150 card. Make sure you use enough force to make a solid connection. You should hear a click.
4. Setup the DIP switches SW1 on the ML605 to select a DEMO mode (all OFF).

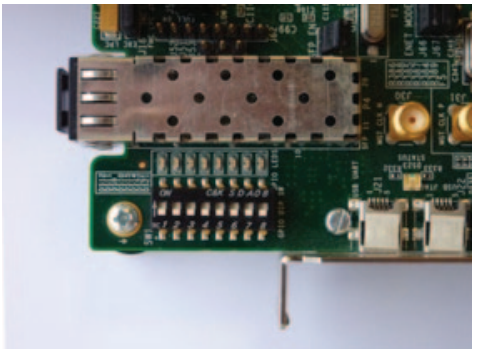

Figure 3

5. Power up the board, connect USB cable.

6. Connect the Ethernet cable directly to your PC and to the Ethernet port on the ML605 board.

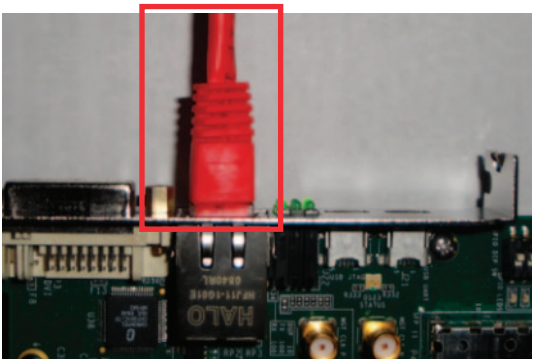

Figure 4

7. Connect the USB Type-A to mini-B 5-pin cable from your PC to J22 on the ML605 board.

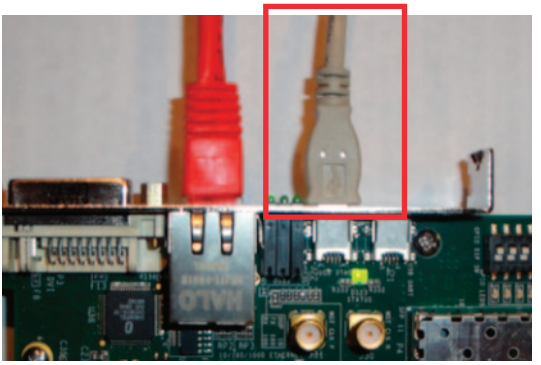

Figure 5

8. Connect the ML605 board power supply and turn on the Power Switch ON.

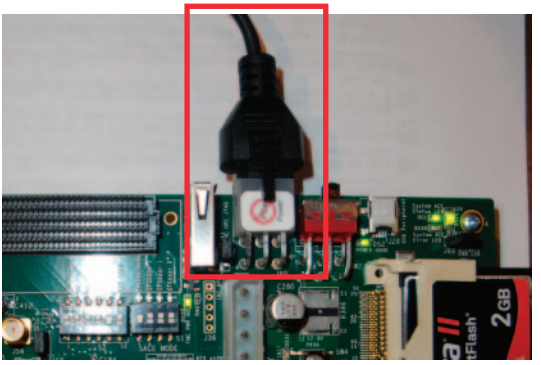

Figure 6

Download the DSP Kit Reference Design

9. Go to the Avnet Virtex-6 FPGA DSP Kit web page: http://www.em.avnet.com/v6dspkit
10. At the bottom of the this web page click on the link that says “Support Files and Downloads.
11. To download the Getting Started Design files click on the link “Virtex6 DSP Kit - Getting Started Reference Design”.This will download the file “virtex6dsp_getting_started_reference_design_12_3_0.zip” to your computer.
12. Unzip this file using the Extract to Hear” option to the C: drive of your computer to install the getting started design files. The top-level folder name should be “virtex6dsp_getting_started_reference_design”. If this is not how it was extracted then change the name to that. There are hard paths in the design files that require this exact file structure.

Getting Started with the Virtex-6 DSP Kit Demo

In this demo we will be downloading the RTL version of the DUC / DDC design to the ML605 board. This design has been modified to include Xilinx ChipScope probes to capture the output data from the hardware and send it back to the ChipScope analyzer software to be displayed. Chipscope can display the data as a signed integer which allows us to view the DUC / DDC output in analog format.

1. Launch Xilinx Project Navigator from the start menu command “Xilinx ISE Design Suite -> ISE Design Tools -> Project Navigator”. Note that this will be version dependent.

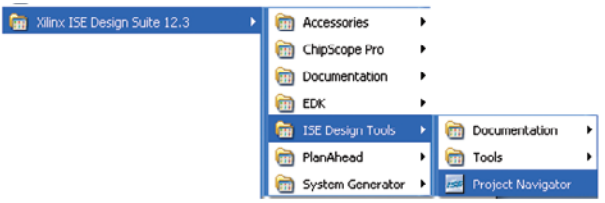

Figure 7

2. From Project Navigator use the pull-down menu command “File -> Open Project” to load the project file “duc_ddc_umts_virtex6_12_3.xise” in the folder

   C:\virtex6dsp_getting_started_design_12_3_0\RTL\Reference_Design\implementation\VHDL\ISE

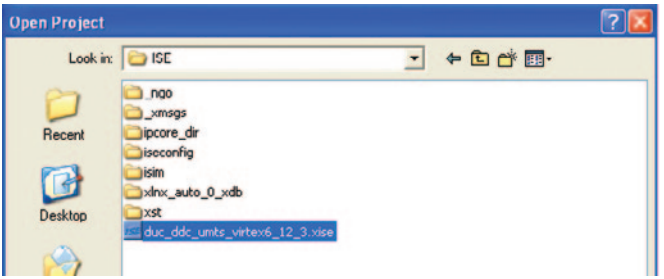

Figure 8

3. From the “Design” window make sure that the “Implementation” option is selected. From the “Hierarchy” window select the top-level RTL source file “ml605_fmc150.vhd” then from the Project Navigator “Processes” window select “Analyze Design using Chipscope” and execute the pop-up command “Run”.This will take about 5 minutes.

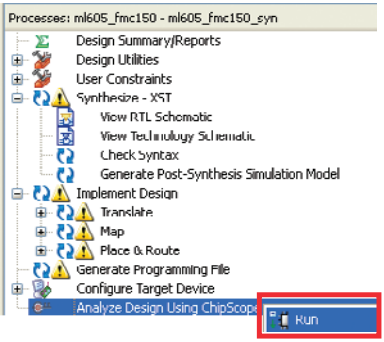

Figure 9

4. Initialize the JTAG chain by clicking on the toolbar command “Open Cable / Search JTAG Chain” from ChipScope.

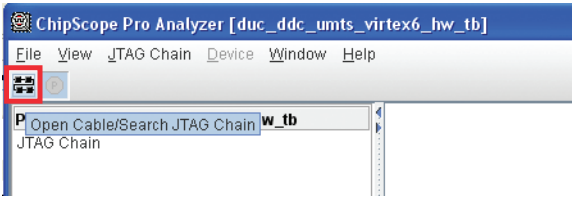

Figure 10

5. From the ChipScope Project window select “DEV1: MyDevice1 (XC6LX240T) and execute the pop-up command “Configure”. Click **OK** on the window that opens. This will configure the FPGA with our design.

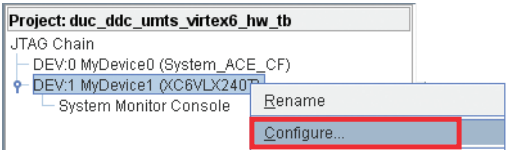

Figure 11

6. Double click “Trigger setup” in the “DDC Output” unit and change the Trigger Apply Settings and Arm Trigger Mode into “Repetitive”.

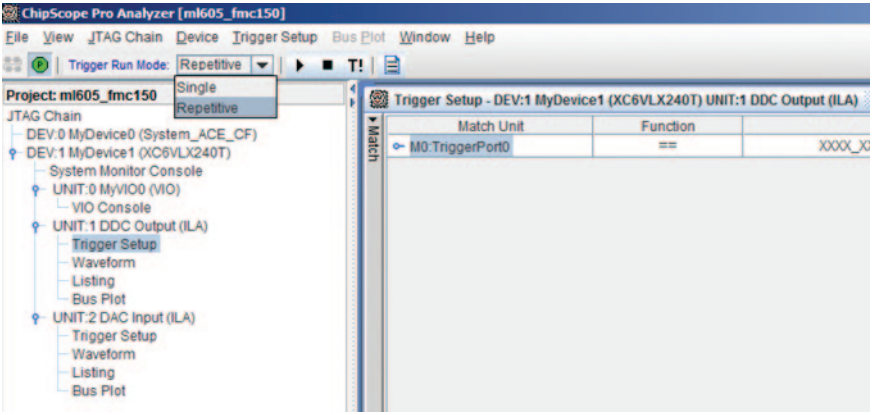

Figure 12

7. Double click “Bus Plot” in the “DDC Output” unit, select both busses in the “Bus Selection” pane as shown below, and click the run button. The I/Q output of the DDC is captured and displayed. ChipScope ILA has been implemented to monitor the signals from the ADCs as well as signals at the DUC outputs driving the DACs. If you wish to capture signals at the DUC outputs, select the “DAC Input” unit in the previous step and repeat the procedure.

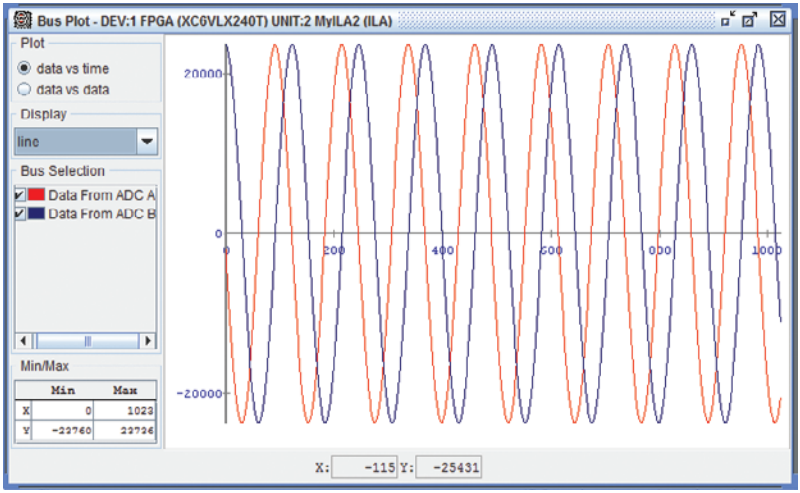

Figure 13

Congratulations!

You have now run the Virtex-6 FPGA DSP Kit reference design through the FMC150 daughter card and observed the results in ChipScope. Since you have been provided a fully functional DSP design you can now begin developing your DSP application on Xilinx Virtex-6 FPGAs

Tutorials

Virtex-6 FPGA DSP Kit RTL Tutorial

- Guide of a series of design techniques useful for implementing DSP algorithms onto Xilinx FPGAs using RTL design methodologies
- How to use ISim to analyze the design and compare the response to golden vectors from MATLAB
- How to use ChipScope to verify the hardware using an impulse input
- Drive the D/A and A/D on the FMC150 in loopback mode

Virtex-6 FPGA DSP Kit System Generator Tutorial

- Guide of a series of design techniques useful for implementing DSP algorithms onto Xilinx FPGAs using Simulink and Xilinx System Generator for DSP
- This will show you how to use hardware co-simulation to accelerate simulations and validate the DSP hardware in a controlled simulation environment
- How to use DSP IP compilers such as the FIR Compiler to rapidly create efficient DSP hardware for the Virtex-6 device

Getting Help and Support

For questions regarding products within a Product Entitlement Account, send an e-mail message to the regional customer services representative.

- Canada, USA and South America — isscs_cases@xilinx.com
- Europe, Middle East, and Africa — eucases@xilinx.com
- Asia Pacific including Japan — apaccase@xilinx.com

For technical support, including the installation and use of a product license file, contact Xilinx Online Technical Support at www.support.xilinx.com. This site also provides the following support resources:

- Software, IP and documentation updates
- Access to technical support web tools
- Searchable answer database with over 4,000 solutions
- User forums
- Training — Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Virtex-6 DSP Kit reference designs or kit hardware http://www.em.avnet.com/v6dspkit

INSTALLING AND LICENSING MATLAB AND SIMULINK

If MATLAB / Simulink will be used in the design flow and it is not already installed, go to the following website to request evaluation software http://www.mathworks.com/xilinx_dspkits

The MATLAB installer has an option to automatically download the installation key and authorize software through the internet. If your company uses a proxy server click on the “connections” option to the MATLAB installer and provide the necessary proxy information.

INSTALLATION AND LICENSING OF ISE DESIGN SUITE

This Avnet Virtex-6 FPGA DSP kit comes with entitlement to a full seat of the ISE Design Suite: System Edition that is device locked to a Virtex-6 XC6VLX240T-1FFG1156 device. This software can be installed from the DVD or the Web installer can be downloaded from the following http://www.xilinx.com/support/download/index.htm.

ISE 12.3 Software Installation

Note: If you are planning on using the System Generator flow you must install MATLAB on your computer before installing ISE Software.

1. Run the ISE Design Suite Installer:
   a. Option 1: Insert the ISE Design Suite DVD included in this kit into the computer
      – If the Installer does not start automatically, run the "xsetup" executable from the DVD
   b. Option 2: Run the Web Installer that can be downloaded from http://www.xilinx.com/support/download/index.htm

   A screen will appear with a welcome dialog, two license agreement dialogs and an opportunity to select the location for the software installation.

   Note: It is recommended that you accept the two license agreements and accept the default install.

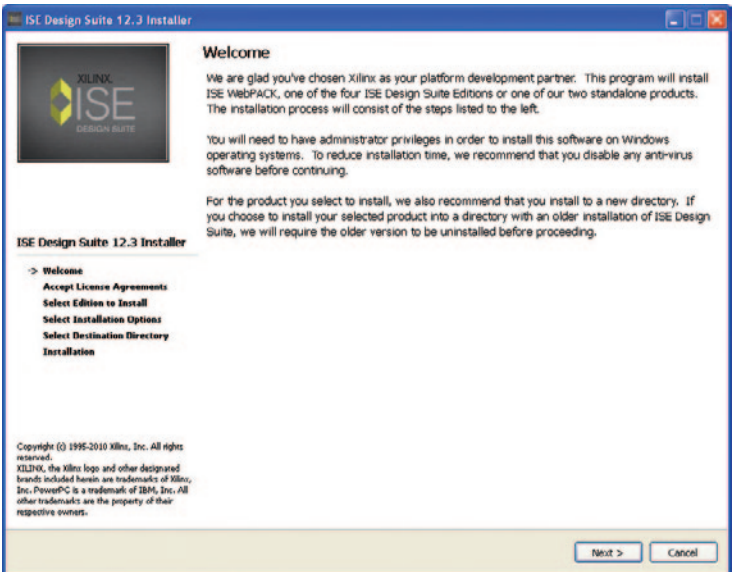

Figure 14: ISE Install Welcome Screen

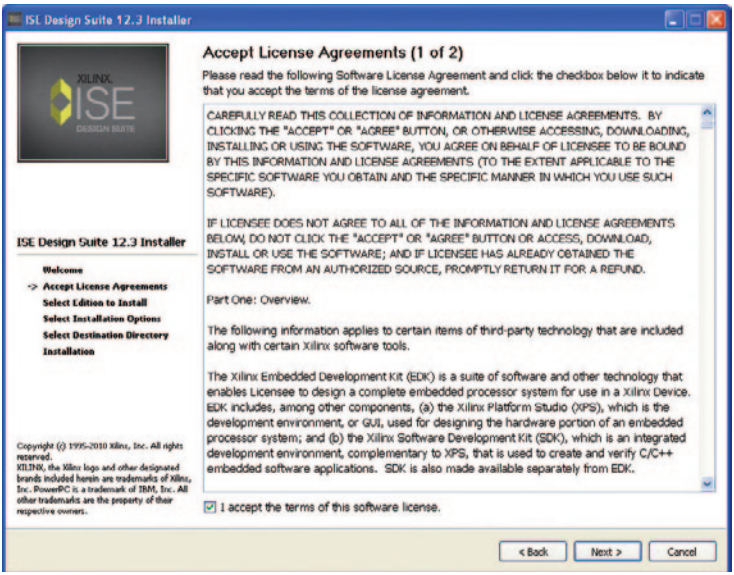

Figure 15: ISE End-user License Agreement

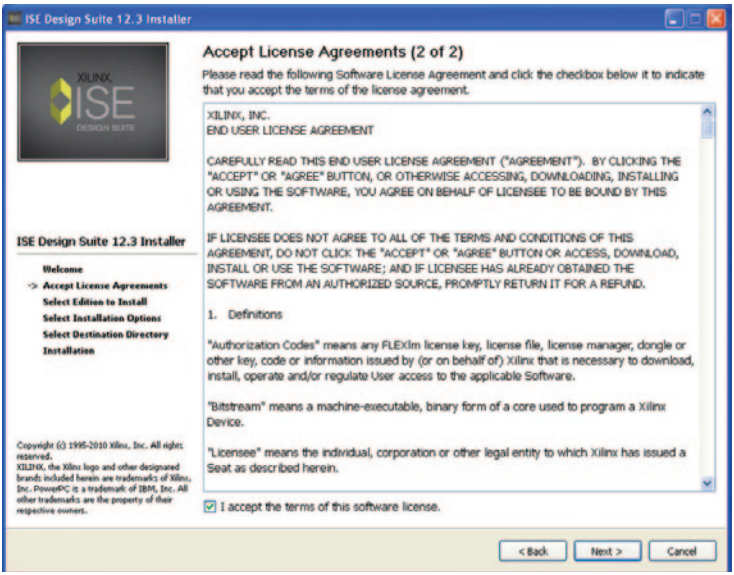

Figure 16: ISE Third- Party Usage License Agreement

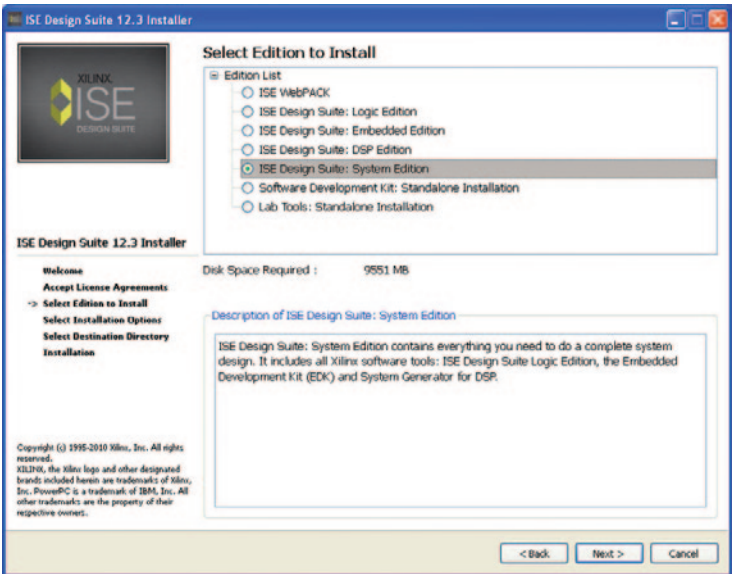

Figure 17: Select Edition to Install

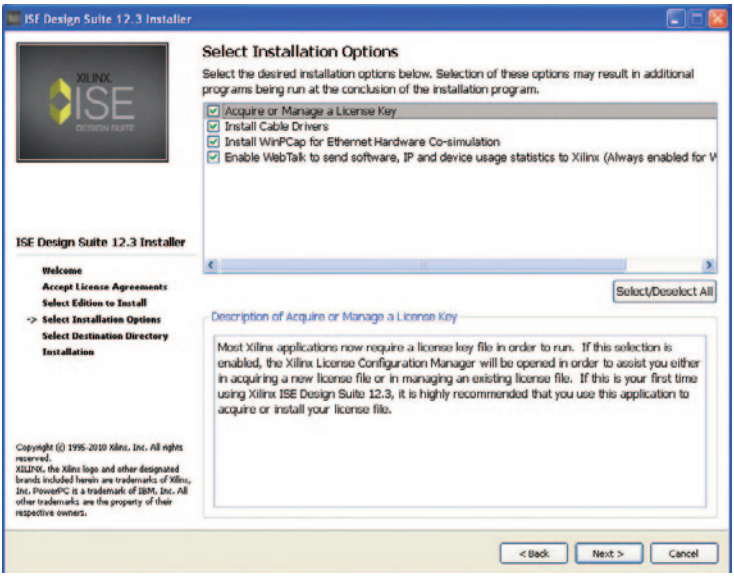

Figure 18: Select Installation Options

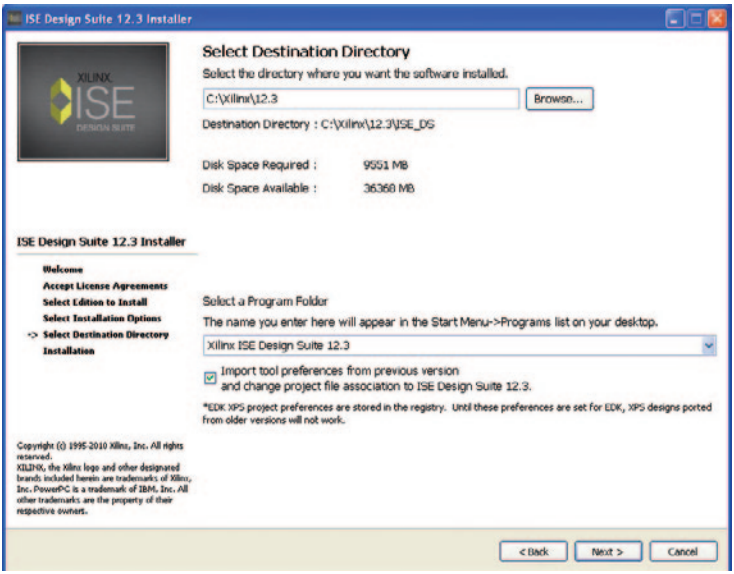

Figure 19: Select Destination Directory and Program Folder

2. Follow the rest of the steps presented by the installer, accepting the defaults to complete the installation. It will stop at 98% complete and prompt you to select a MATLAB version. See Step 3 for instructions.

   Note: The DVD installation might take about one hour. The Web installation might take about three to ten hours based on Internet download speeds.

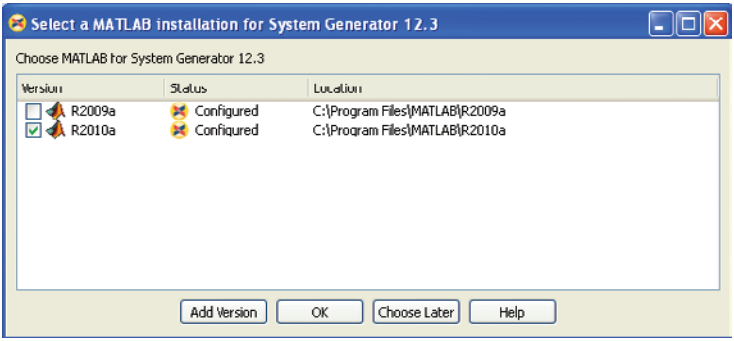

Figure 20: Select MATLAB for Installation for System Generator

3. Near the end of the install you will see the dialog shown below. If you are planning on using System Generator you will need to have MATLAB installed on your computer. Select the version of MATLAB you have installed and click on **OK**. If you are planning on using the RTL design flow you can cancel this form to complete the installation processes.
4. Reboot your machine.

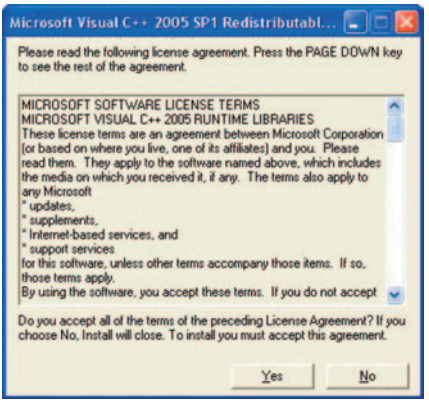

Figure 21: Microsoft Visual C++ Library Install

Downloading and Installing Tool Licenses

1. Visit the Xilinx software registration and entitlement site at http://www.xilinx.com/getproduct
2. The Web browser will launch, showing the Xilinx product download and licensing site.

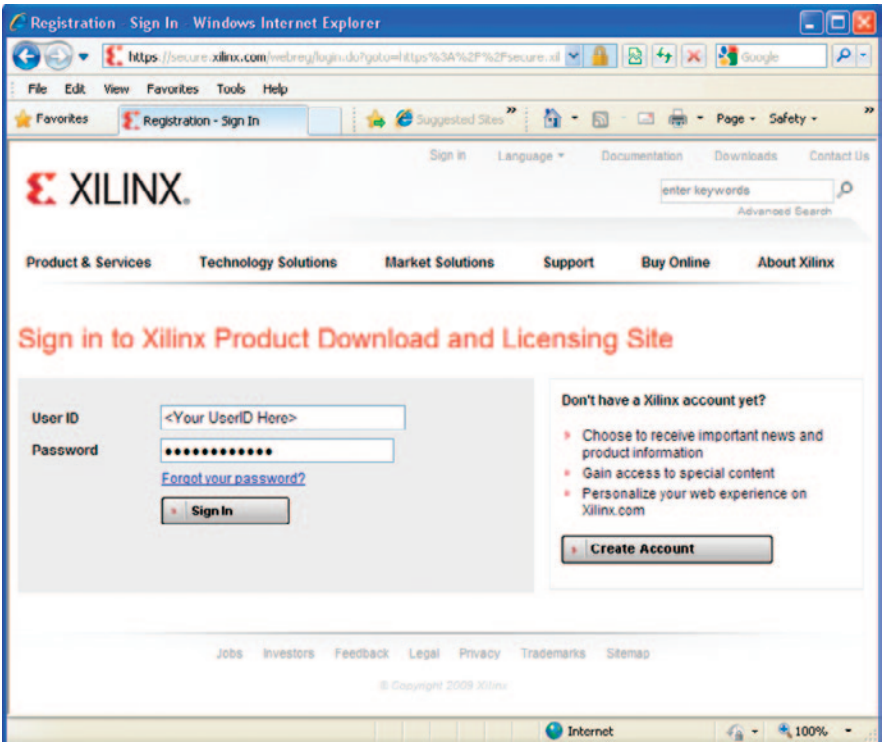

Figure 22: Sign In to Xilinx Product Download and Licensing Site

3. Log in if there is an existing account or create an account if needed.

   Note: User name and password are provided in an email sent when the kit was ordered. If the information is not available or has been misplaced, please contact Xilinx customer service. They will be able to provide support to access the account.

   http://www.xilinx.com/support/techsup/tappinfo.htm

4. After logging in, a shipping address verification may be requested. Click **Next** after the shipping address has been verified or updated.

5. Check the product **ISE Design Suite System Edition, Node-Locked License** and click on **Generate Node-Locked License** as shown below.

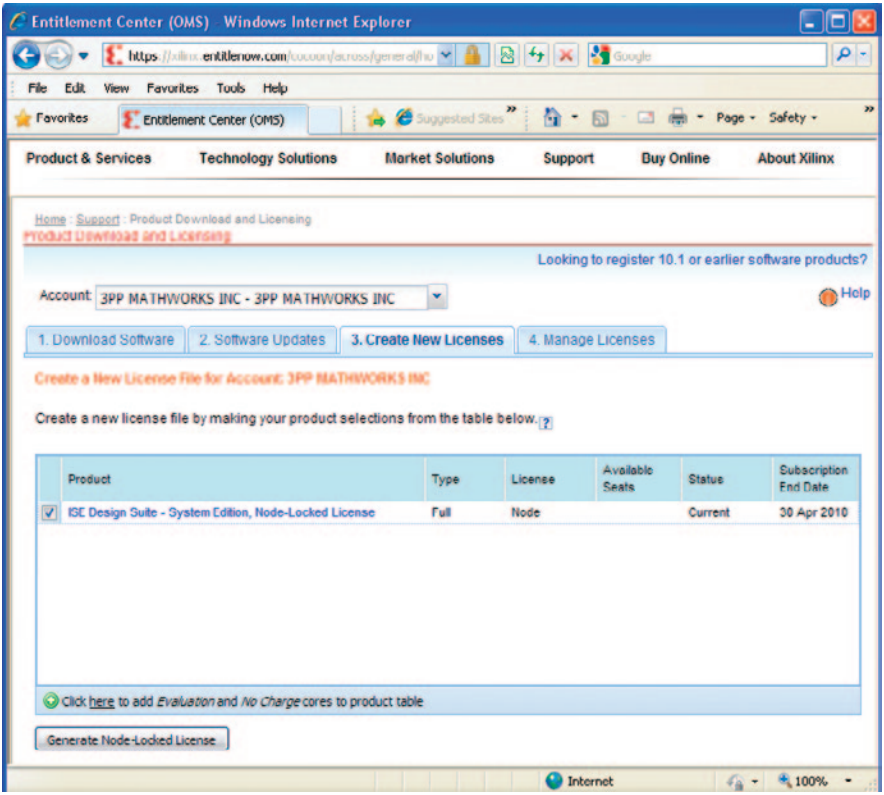

Figure 23: Xilinx Entitlement Center

6. Follow the instructions to generate the license by providing the Host OS information and Host ID (Disk Serial number or Ethernet MAC address) as shown in the following figure and click **Next**.

   Note: Laptop users may want to select their Disk ID or Wireless Ethernet card HostID. Laptops on docking stations might find there are three Ethernet HostIDs to choose from. If a docking station HostID is selected, then the license will only be active when the computer is docked. It is best to avoid the HostID of the RJ45 Ethernet connection on Laptop computers, as some Ethernet adapters will power down when not plugged into the network. If an Ethernet adapter is selected, it is best to select the wireless card.

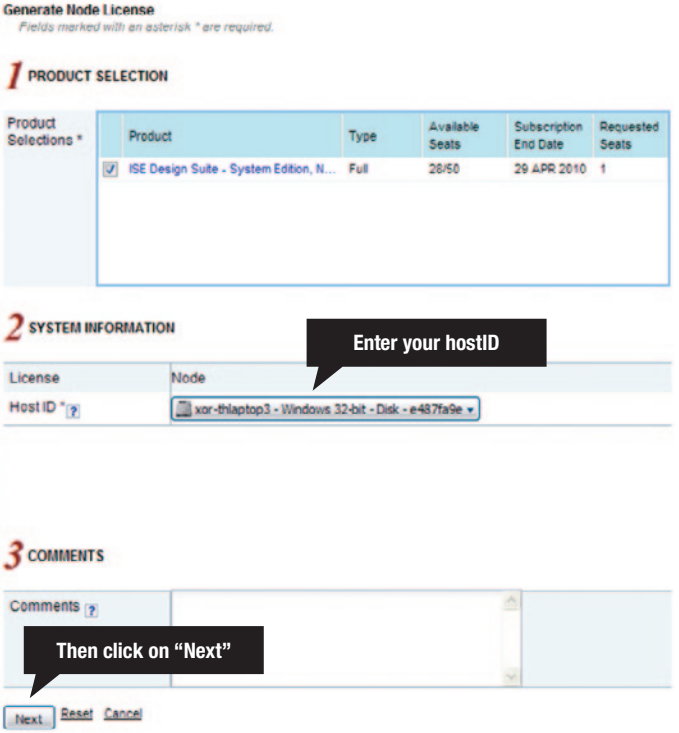

Figure 24: Selecting Your Host ID

7. Review the license request as show in *Figure 25* and click **Next**.

Figure 25: Reviewing the License Request

8. The generated license will be e-mailed in an E-mail similar to the one shown below.

   Note: These e-mails may appear in the junk mail folder. Save this file to a temp folder or the desktop.

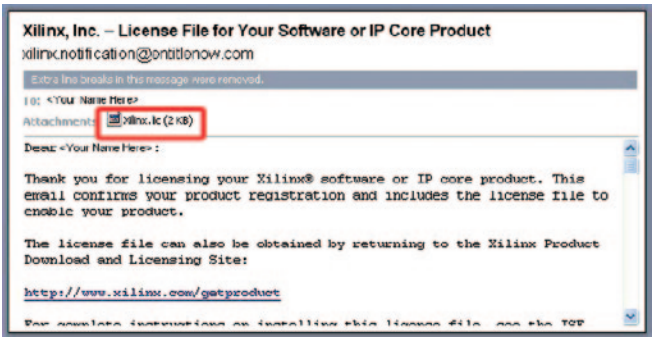

Figure 26: Xilinx License Notification E-mail

9. Start the Xilinx License Manager (Start >Programs >ISE Design Suite 12.3 >Manage Xilinx Licenses) and click on **Copy License** to install the license on the computer.

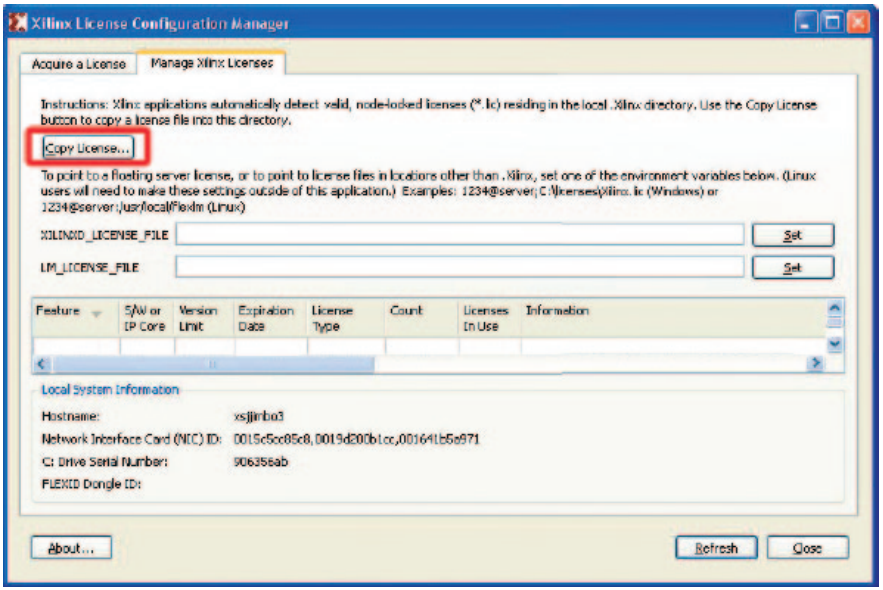

Figure 27: Manage Xilinx License Tab

10. Navigate to the saved Xilinx.lic file and select it as shown below.

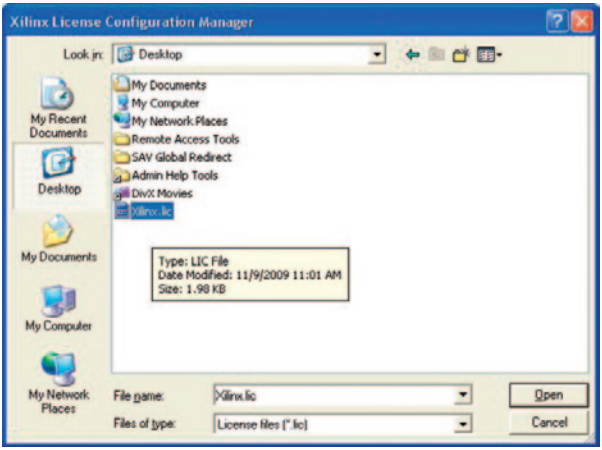

Figure 28: Select the Xilinx.lic File

11. The ISE software license has been successfully installed. Click **OK** on the Success Dialog (shown below) and close the Xilinx License Configuration Manager.

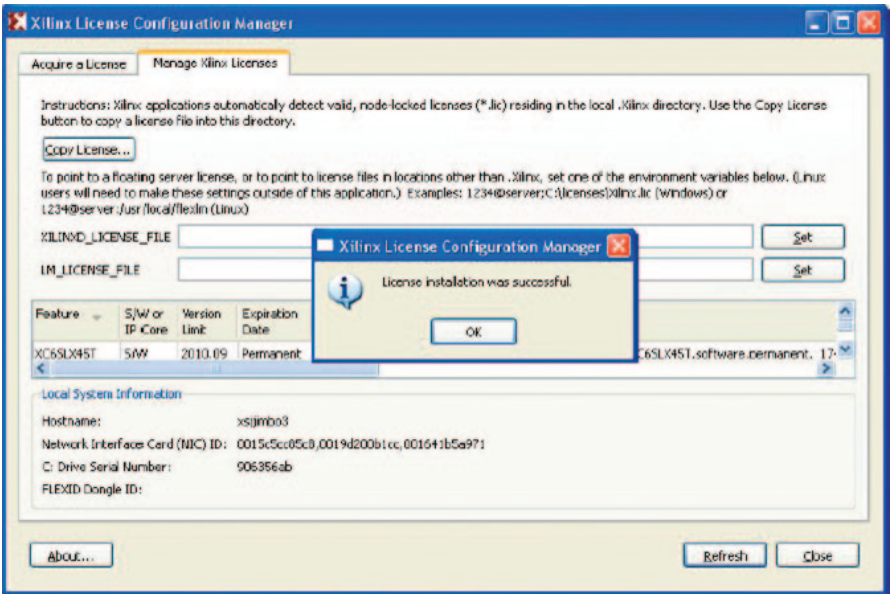

Figure 29: License and Installation Successful

Congratulations!
You have now installed the ISE Design Suite tools and setup the licenses for the System Edition of the tools. You are now ready to use Xilinx ISE Design Suite System Edition to create or modify your custom DSP design. For detailed information on licensing & installation, please refer the release notes available on-line at:

http://www.xilinx.com/support/documentation/

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