# RM3183

## Dual ARINC 429 Line Receiver

## Features

- Converts ARINC levels to serial data
- Adjustable noise filters
- TTL and CMOS compatible outputs
- Built-in test inputs
- Input protection circuitry
- Mil-Std-883B screening available
- 20-pin DIP and LCC packages available
- Dice with Mil visual screening available

## Description

The RM3183 is a dual line receiver designed to meet all requirements of the ARINC 429 interface specification. It contains two independent receiver channels which accept differential input signals and converts them to serial TTL data.

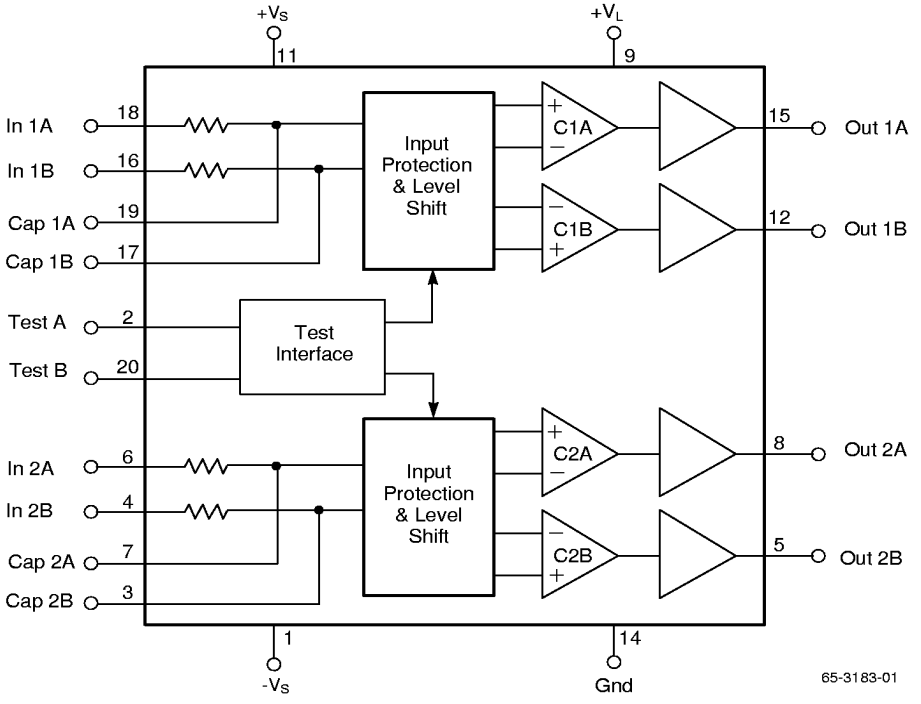
Input overvoltage protection is provided by special circuitry including dielectrically-isolated thin-film resistors and clamping diodes. Self-test logic inputs are provided for internal system tests. These inputs force the outputs to either a high, a low, or a null state for off-line system tests.

Input noise filtering is accomplished with external capacitors. Two are required for each channel and can be adjusted for best noise immunity at a specific data rate.

Three power supplies are needed plus ground. The input thresholds depend only on the logic supply, so a wide range of dual supplies can be accommodated.

The Fairchild RM3183 line receiver is the companion chip to the RM3182 line driver. Together they provide all the analog functions needed for the ARINC 429 interface. Digital data processing involving serial-to-parallel conversion and clock recovery can be accomplished using one of the ARINC interface ICs available or by discrete or gate array implementations.

## Block Diagram




Rev. 1.0.0

## Functional Description

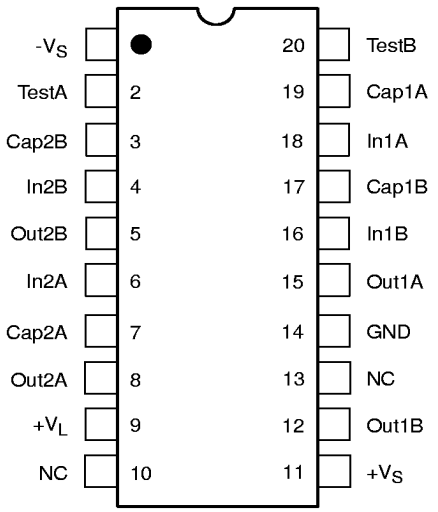
The RM3183 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: a resistor-diode input network, a window comparator, and a logic output buffer stage. The first stage provides overvoltage protection and biases the signal using voltage dividers and current sources which are internally connected to the $+V_L$ logic supply. This configuration provides excellent input common mode rejection and a stable reference voltage for the window comparators. Because the threshold for switching is determined by this circuitry, ±5% tolerance is recommended for the $+V_L$ supply. The test inputs will set the outputs to a predetermined state for built-in test capability. The ARINC inputs must be forced to 0V when using the test inputs. If the test inputs are not used, they should be grounded.

The window comparator stage generates two serial data streams, one having logic 1 states corresponding to ARINC "High" states (OUTA), and the other having logic 1 states corresponding to ARINC "Low" states (OUTB). An ARINC "Null" state at the inputs forces both outputs to logic 0. Thus, the ARINC clock signal is recovered by applying a NOR function to OUTA and OUTB.

The output stage generates a TTL compatible logic output capable of driving several gate inputs.

## Pin Assignments

Ceramic Dip
Top View

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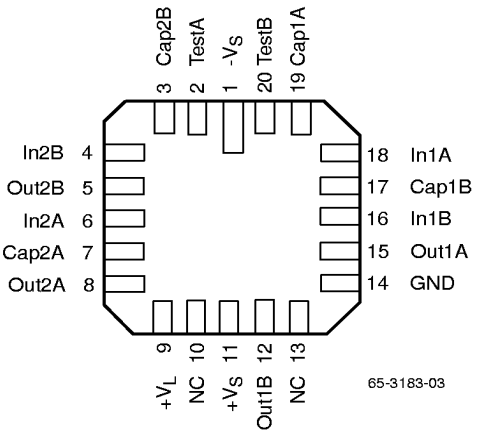
LCC
Top View

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## Absolute Maximum Ratings

| Parameter | | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | $+V_S$ | | +20 | VDC |
| | $-V_S$ | | –20 | VDC |
| | $+V_L$ | | +7 | VDC |
| Operating Temperature Range | | -55 | +125 | °C |
| Storage Temperature Range | | -65 | +150 | °C |
| Input Voltage Range | | | ±50 | V |
| Output Short Circuit Duration | | Not protected | | |
| Internal Power Dissipation | | | 900 | mW |
| Lead Soldering Temperature (60 seconds) | | | +300 | °C |

## Thermal Characteristics (Still air, soldered into PC board)

| | Ceramic DIP | LCC |
|---|---|---|
| Maximum Junction Temperature | +175°C | +175°C |
| Maximum $P_D$ $T_A$ < 50°C | 1042 mW | 925 mW |
| Thermal Resistance, $\theta J_C$ | 60°C/W | 37°C/W |
| Thermal Resistance, $\theta J_C$ | 120°C/W | 105°C/W |

## DC Electrical Characteristics

$T_A$ = -55°C to +125°C, ±12V ≤ $V_S$ ±15V, $V_L$ = +5V, unless otherwise noted

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | V(A)-V(B) | OUTA = 1 | | 6.5 | 10 | 13 | V |
| $V_{IL}$ | V(A)-V(B) | OUTB = 1 | | -6.5 | -10 | -13 | V |
| $V_{IN}$ | V(A)-V(B) | OUTA and OUTB = 0 | | -2.5 | 0 | +2.5 | V |
| $V_{IC}$(2) | V(A) and V(B)-GND | Maximum common mode frequency = 80 kHz | | | ±5 | | V |
| $R_I$ | Input resistance, Input A to Input B | | | 30 | 50 | | kΩ |
| $R_H$ | Input resistance, Input A to Gnd | | | 19 | 25 | | kΩ |
| $R_G$ | Input resistance, B to Gnd | | | 19 | 25 | | kΩ |
| $C_I$(1, 2) | Input capacitance, A to B | Filter caps disconnected | | | 3 | 10 | pF |
| $C_H$(1, 2) | Input capacitance, A to Gnd | Filter caps disconnected | | | 3 | 10 | pF |
| $C_G$(1, 2) | Input capacitance, B to Gnd | Filter caps disconnected | | | 3 | 10 | pF |
| **Test Inputs (TESTA, TESTB)** | | | | | | | |
| $V_{IH}$ | Logic 1 input voltage | | V(A) = 0V V(B) = 0V | 2.7 | | | V |
| $V_{IL}$ | Logic 0 input voltage | | | | | 0.0 | V |
| $I_{IH}$ | Logic 1 input current | $V_{IH}$ = 2.7V | | | 5 | 15 | µA |
| $I_{IL}$ | Logic 0 input current | $V_{IL}$ = 0.0V | | | 0.5 | 1.0 | µA |
| **Outputs** | | | | | | | |
| $V_{OH}$ | $I_{OH}$ = 100 µA | $T_A$ = 25°C | | 4.0 | 4.3 | | V |
| | $I_{OH}$ = 2.8 mA | Full temperature range | | 3.5 | 4.0 | | V |
| $V_{OL}$ | $I_{OL}$ = 100 µA | $T_A$ = 25°C | | | 0.02 | 0.08 | V |
| | $I_{OL}$ = 2.0 mA | Full temperature range | | | 0.3 | 0.8 | V |
| Tr | Rise Time | $C_L$ = 50 pF, $T_A$ = 25°C | | | 40 | 70 | ns |
| Tf | Fall Time | $C_L$ = 50 pF, $T_A$ = 25°C | | | 30 | 70 | ns |
| $T_{PLH}$ | Propagation delay Output low to high | $C_L$ = 50 pF, $f_O$ = 400 kHz Filter caps = 39 pF | | | 800 | | ns |
| $T_{PHL}$ | Output high to low | $T_A$ = 25°C | | | 320 | | ns |

## DC Electrical Characteristics (continued)

$T_A$ = -55°C to +125°C, ±12V ≤ $V_S$ ±15V, $V_L$ = +5V, unless otherwise noted

| Symbol | Parameter | Conditlons | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| $I_{CC}$ (+$V_S$) | Test inputs = 0V | ±$V_S$ = 15V, $T_A$ = 15°C | | 3.7 | 7.0 | mA |
| | | ±$V_S$ = 12V, $T_A$ = 15°C | | 3.0 | 6.0 | mA |
| $I_{EE}$ (-$V_S$) | Test inputs = 0V | ±$V_S$ = 15V, $T_A$ = 15°C | | 8.7 | 15.0 | mA |
| | | ±$V_S$ = 12V, $T_A$ = 15°C | | 7.4 | 14.0 | mA |
| $I_{DD}$ (+$V_L$) | Test inputs = 0V | ±$V_S$ = 15V, $T_A$ = 15°C | | 9.0 | 20.0 | mA |
| | | ±$V_S$ = 12V, $T_A$ = 15°C | | 8.6 | 18.0 | mA |

**Notes:**

1. With noise filter capacitors disconnected.
2. Guaranteed by design.

## Truth Table

| ARINC Inputs V(A) - V(B) | Test Inputs | | Outputs | |
|---|---|---|---|---|
| | TESTA | TESTB | OUTA | OUTB |
| Null | 0 | 0 | 0 | 0 |
| Low | 0 | 0 | 0 | 1 |
| High | 0 | 0 | 1 | 0 |
| V(A) = 0V, V(B) = 0V | 0 | 1 | 0 | 1 |
| V(A) = 0V, V(B) = 0V | 1 | 0 | 1 | 0 |
| V(A) = 0V, V(B) = 0V | 1 | 1 | 0 | 0 |

## Typical Performance Characteristics

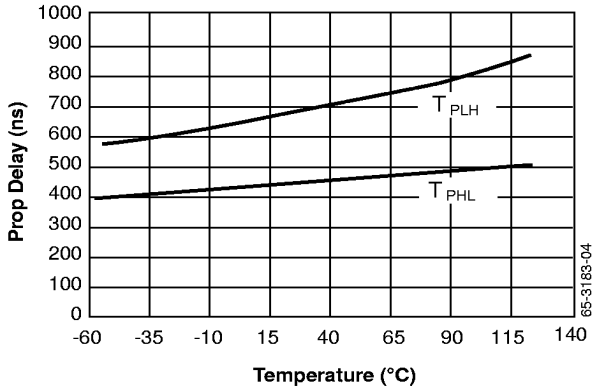



**Figure 1. Propagation Delay vs. Temperature**
**$C_L$ = 50 pF, $C_{FILTER}$ = 39 pF**

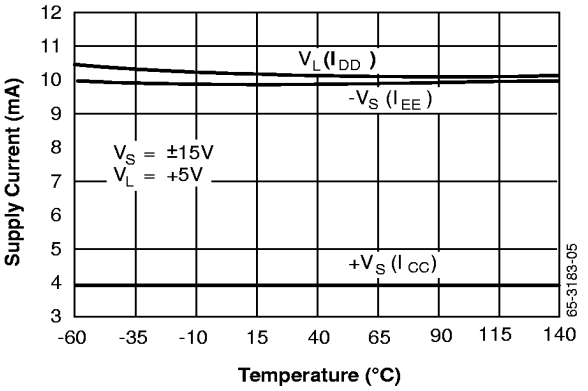



**Figure 2. Supply Current vs. Temperature**

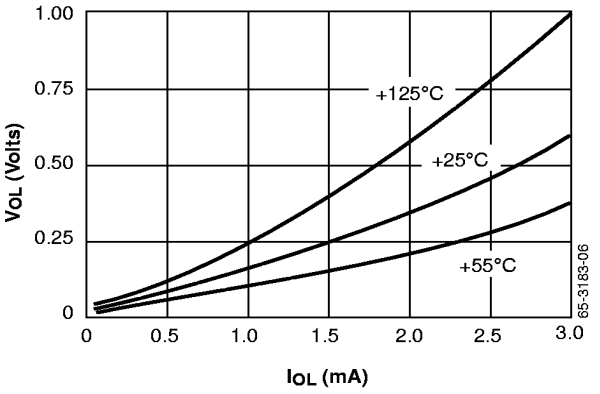



**Figure 3. Output Voltage Low vs. Output Current**

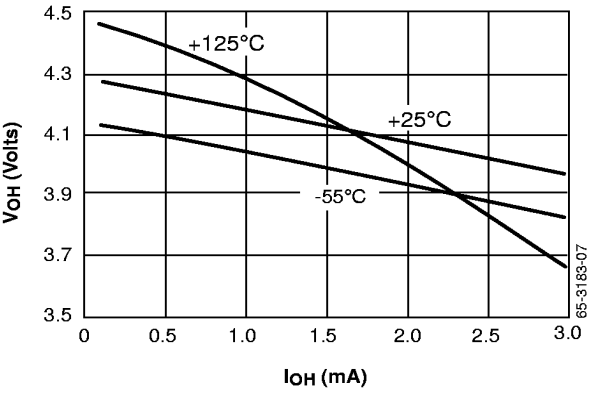



**Figure 4. Output Voltage High vs. Output Current**

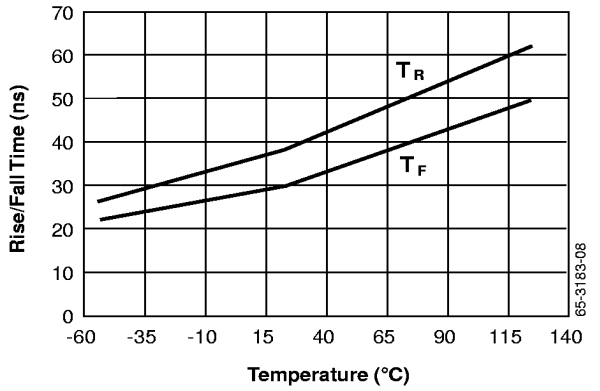



**Figure 5. $T_R$ and $T_F$ vs. Temperature**

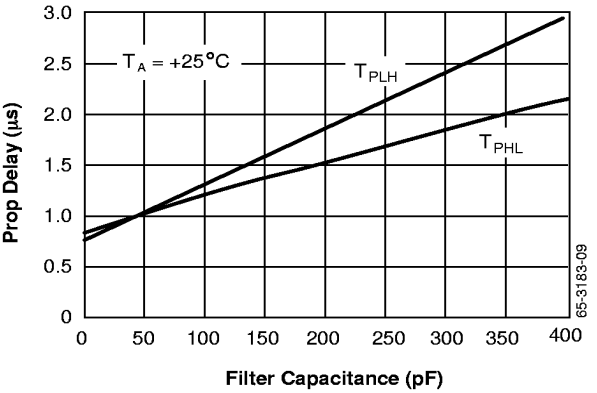



**Figure 6. Propagation Delay vs. Filter Capacitance**
**$T_A$ = 25°C**

## AC Test Waveforms

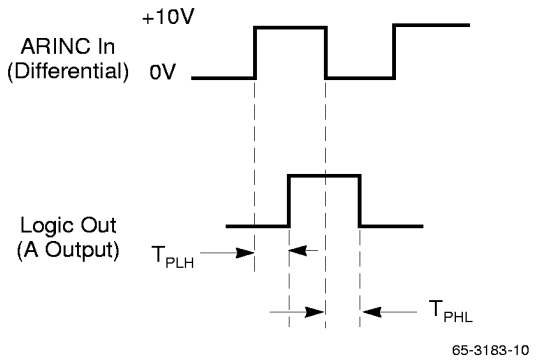



Figure 7. Propagation Delay

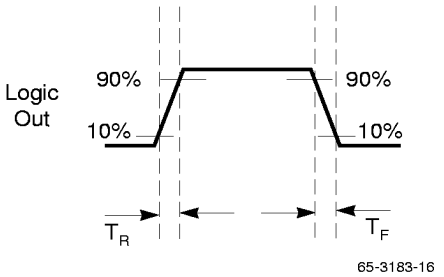
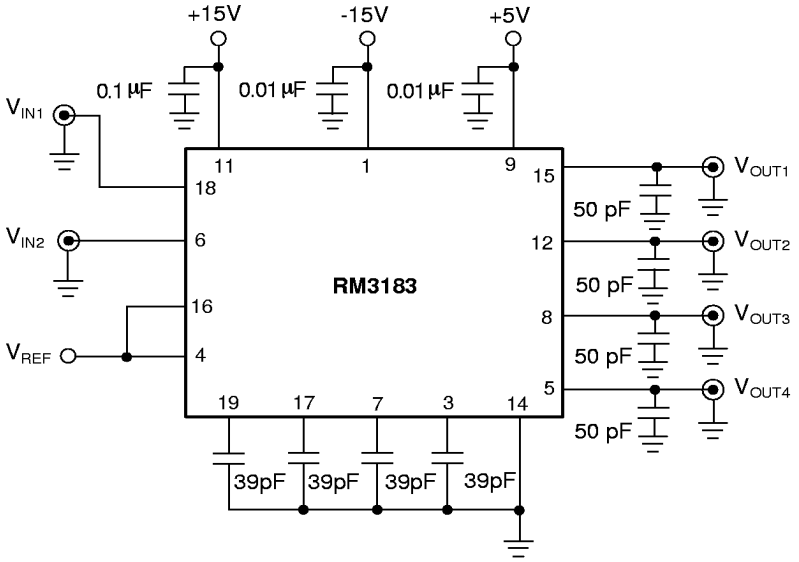



Figure 8. Rise/Fall Times

## Test Circuit




**Notes:**

1. $V_{IN}$ = 400 kHz square wave, -3.5V to +3.5V.
2. Set $V_{REF}$ = +3.5 V to test $V_{OUT1}$ and $V_{OUT3}$.
   Set $V_{REF}$ = -3.5 V to test $V_{OUT2}$ and $V_{OUT4}$.
3. 50 pF load capacitance includes probe and wiring capacitance.

Figure 9. AC Test Schematic Diagram

## Applications Information

The standard connections for the RM3183 are shown in Figure 1. Dual supplies from ±12 to ±15 VDC are recommended for the ±$V_S$ supplies. Decoupling of all supplies should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground connections should be sturdy and isolated from large switching currents to provide as quiet a ground reference as possible.

The noise filter capacitors are optional and are added to provide extra noise immunity by limiting the noise bandwidth of the input signal before it reaches the comparator. Two capacitors are required for each channel and they must all be the same value. The suggested capacitor value for a 100 KHz operation is 39 pF, which will give a noise bandwidth of approximately 800 KHz. For lower data rates, larger values of capacitance may be used to yield better noise performance. To get optimum performance, the following equation should be used to calculate capacitor value for a specific data rate:

$$C = \frac{3.95 \times 10^{-6}}{F_O}$$

$F_O$ = Data Rate (bits/sec)

The RM3183 can be used with Fairchild's RM3182 Line Driver to provide a complete analog ARINC 429 interface. A simple application which can be used for systems requiring a repeater-type circuit for long transmissions or test interfaces is given in Figure 2. More RM3182 drivers may be added to test multiple ARINC channels, as shown.

An all digital IC is available which forms a complete receiver system when combined with the RM3183. The Thomson EF4442 is a four channel ARINC 429 receiver IC which contains all the digital circuitry required to interface with an 8-bit processor. Each channel consists of a 32-bit register, an 8-bit status word comparator, and a 24-bit latch. A multiplexer and 8-bit data bus buffer form the interface to the system microprocessor. Figure 3 shows a typical ARINC application having both transmit and receive functions using four ICs: the EF4442, the RM3182 driver and two RM3183 dual receivers.

## Applications

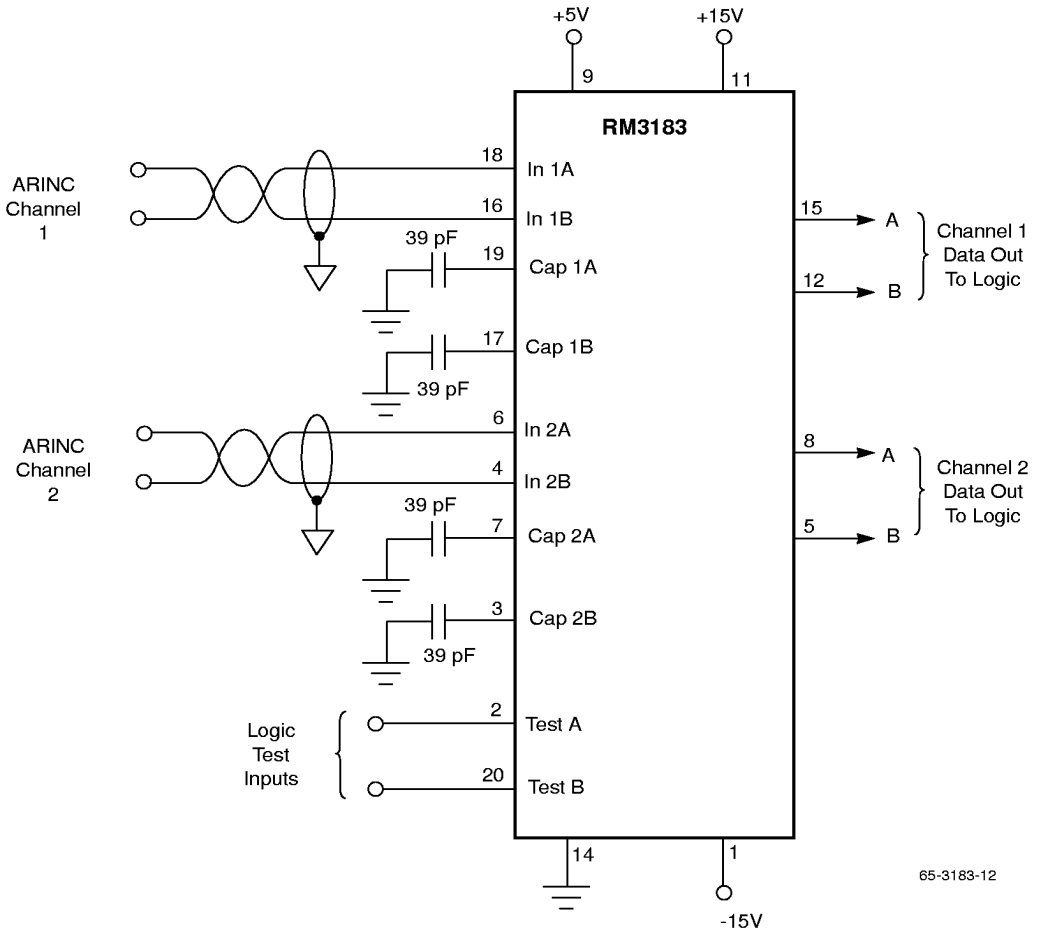



**Figure 9. ARINC Receiver Standard Connections**

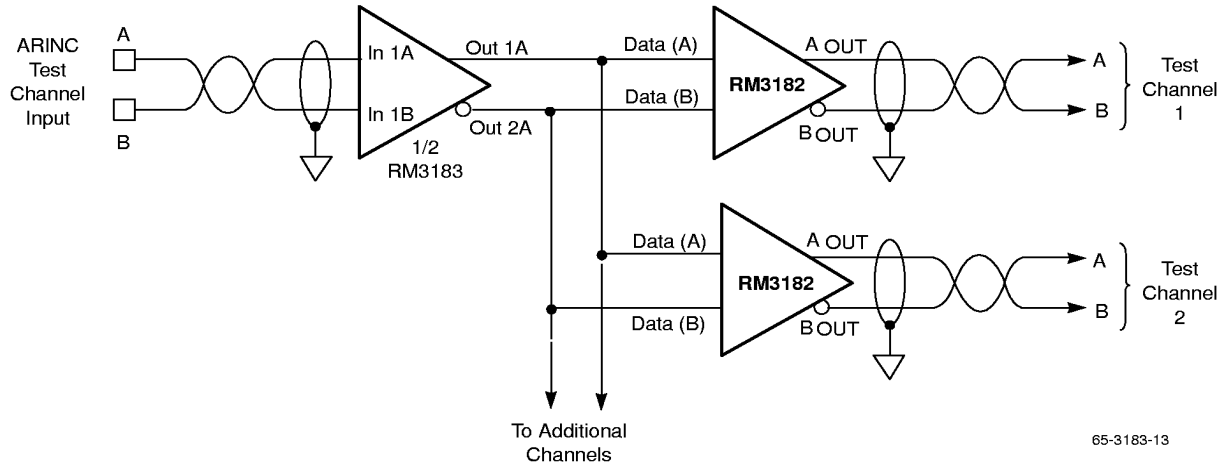



**Figure 10. Repeater Circuit**

## Applications (continued)

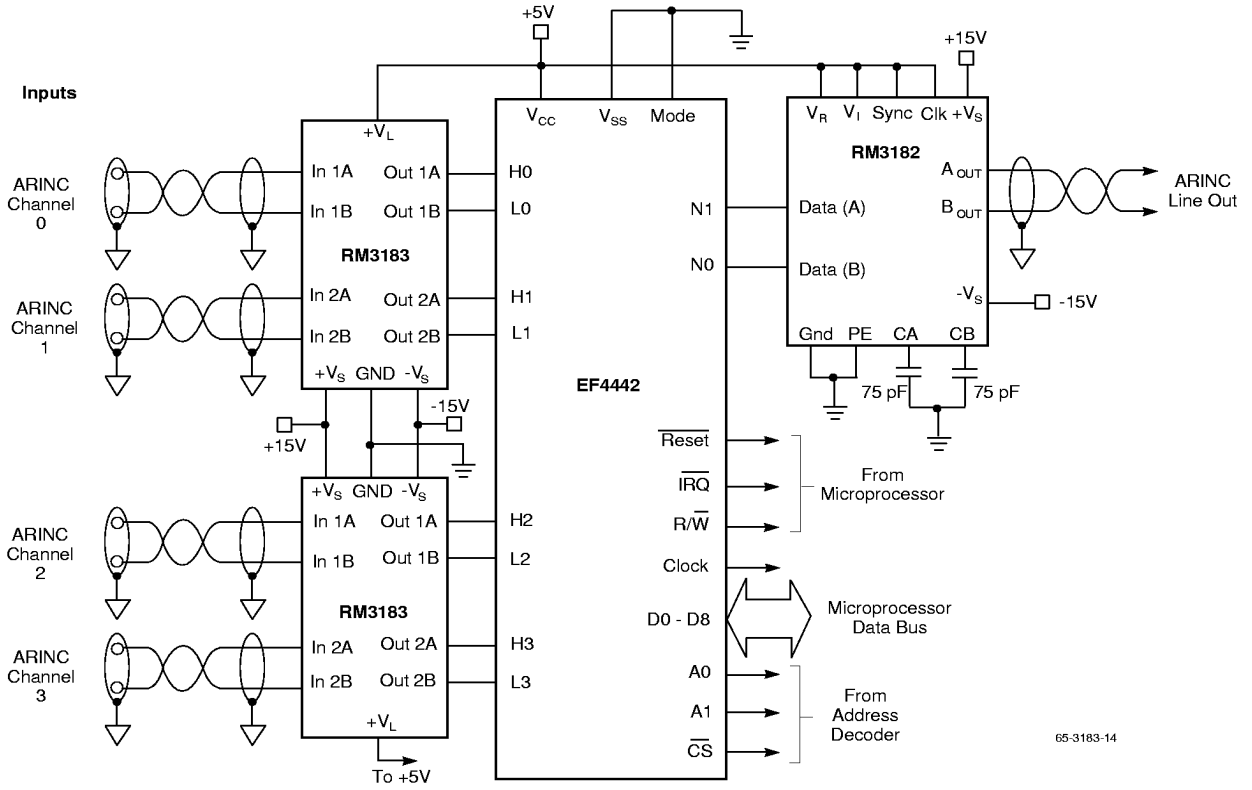



**Figure 11. Four-Channel ARINC Receiver Circuit**

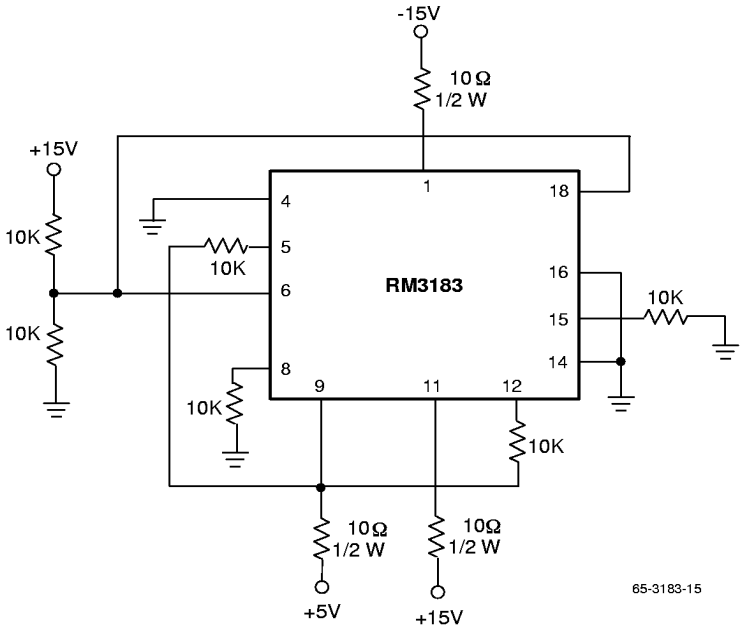



**Figure 12. Burn-In Circuit**

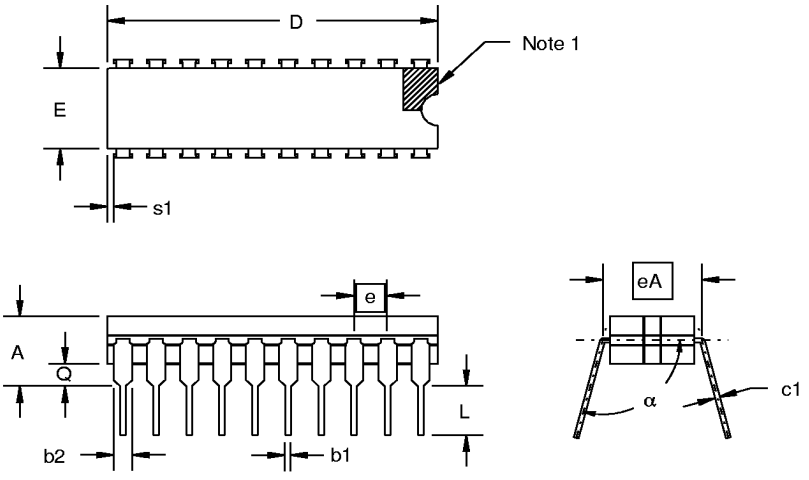
# Mechanical Dimensions

## 20-Lead Ceramic DIP

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | — | .200 | — | 5.08 | |
| b1 | .014 | .023 | .36 | .58 | 8 |
| b2 | .045 | .065 | 1.14 | 1.65 | 2, 8 |
| c1 | .008 | .015 | .20 | .38 | 8 |
| D | — | 1.060 | — | 25.92 | 4 |
| E | .220 | .310 | 5.59 | 7.87 | 4 |
| e | .100 BSC | | 2.54 BSC | | 5, 9 |
| eA | .300 BSC | | 7.62 BSC | | 7 |
| L | .125 | .200 | 3.18 | 5.08 | |
| Q | .015 | .060 | .38 | 1.52 | 3 |
| s1 | .005 | — | .13 | — | 6 |
| α | 90° | 105° | 90° | 105° | |

**Notes:**

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 10, 11 and 20 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corner's (leads number 1, 10, 11, and 20).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat, when lead finish is applied.
9. Eighteen spaces.



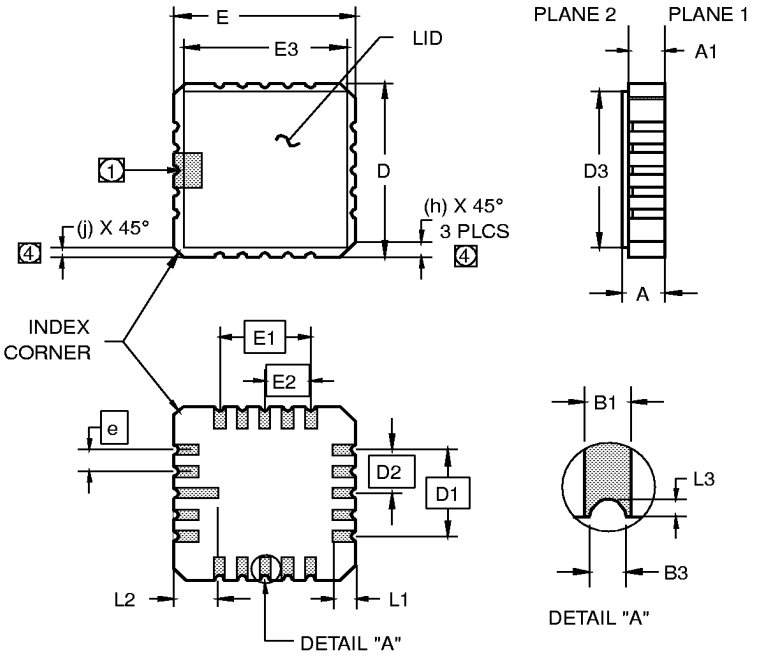
# Mechanical Dimensions (continued)

## 20-Terminal LCC

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | .060 | .100 | 1.52 | 2.54 | 3, 6 |
| A1 | .050 | .088 | 1.27 | 2.24 | 3, 6 |
| B1 | .022 | .028 | .56 | .71 | 2 |
| B3 | .006 | .022 | .15 | .56 | 2, 5 |
| D/E | .342 | .358 | 8.69 | 9.09 | |
| D1/E1 | .200 BSC | | 5.08 BSC | | |
| D2/E2 | .100 BSC | | 2.54 BSC | | |
| D3/E3 | — | .358 | — | 9.09 | |
| e | .050 BSC | | 1.27 BSC | | |
| h | .040 REF | | 1.02 REF | | 4 |
| j | .020 REF | | .51 REF | | 4 |
| L1 | .045 | .055 | 1.14 | 1.40 | |
| L2 | .075 | .095 | 1.91 | 2.41 | |
| L3 | .003 | .015 | .08 | .38 | 5 |
| ND/NE | 5 | | 5 | | |
| N | 20 | | 20 | | |

**Notes:**

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1, terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension "A" controls the overall package thickness. The maximum "A" dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension "B3" minimum and "L3" minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimensions "B3" and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.



## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RM3183S | 20 Lead Ceramic DIP | -55°C to +125°C |
| RM3183L | 20 Terminal Leadless Chip Carrier | -55°C to +125°C |





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