

4V Drive Pch + Pch MOSFET

QS8J5

● Structure

Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) High power package(TSMT8).
- 3) Low voltage drive(4V drive).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8J5		○

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-30	V	
Gate-source voltage	V_{GSS}	±20	V	
Drain current	Continuous	I_D	±5	A
	Pulsed	I_{DP}^{*1}	±20	A
Source current (Body Diode)	Continuous	I_s	-1	A
	Pulsed	I_{sp}^{*1}	-20	A
Power dissipation	P_D^{*2}	1.5	W / TOTAL	
		1.25	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

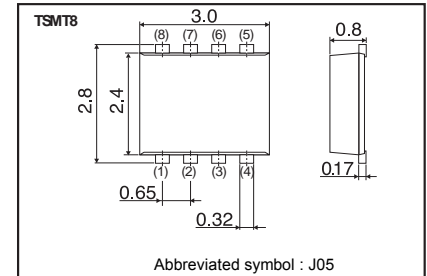
*2 Each terminal mounted on a ceramic board.

● Thermal resistance

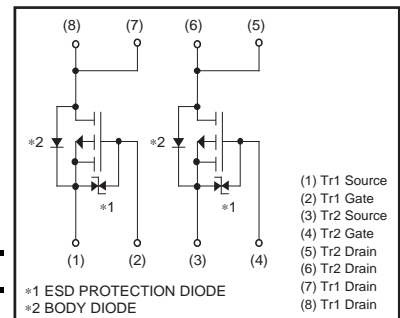
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)^*$	83.3	°C / W / TOTAL
		100	°C / W / ELEMENT

* Each terminal mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS}=-30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	28	39	mΩ	$I_D=-5A, V_{GS}=-10V$
		-	40	56		$I_D=-2.5A, V_{GS}=-4.5V$
		-	45	63		$I_D=-2.5A, V_{GS}=-4V$
Forward transfer admittance	$ Y_{fs} ^*$	3	-	-	S	$I_D=-5A, V_{DS}=-10V$
Input capacitance	C_{iss}	-	1100	-	pF	$V_{DS}=-10V$
Output capacitance	C_{oss}	-	150	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	130	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	9	-	ns	$I_D=-2.5A, V_{DD}=-15V$
Rise time	t_r *	-	40	-	ns	$V_{GS}=-10V$
Turn-off delay time	$t_{d(off)}$ *	-	90	-	ns	$R_L=6\Omega$
Fall time	t_f *	-	55	-	ns	$R_G=10\Omega$
Total gate charge	Q_g *	-	10.0	-	nC	$I_D=-5A, V_{DD}=-15V$
Gate-source charge	Q_{gs} *	-	3.6	-	nC	$V_{GS}=-5V$
Gate-drain charge	Q_{gd} *	-	3.0	-	nC	$R_L=3\Omega, R_G=10\Omega$

*Pulsed

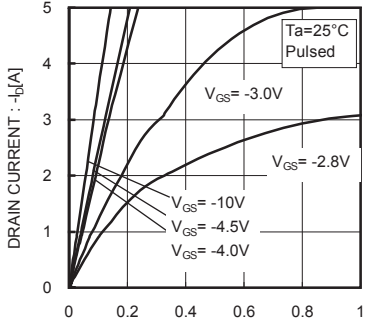
● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

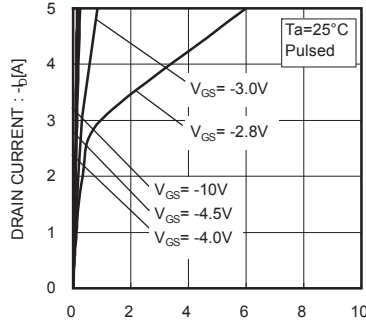
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	-	-	-1.2	V	$I_s=-5A, V_{GS}=0V$

*Pulsed

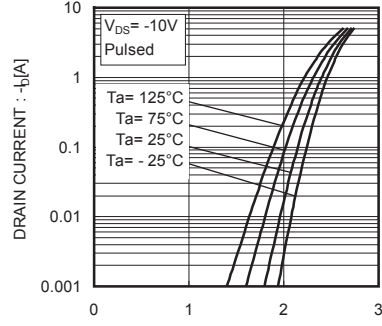
●Electrical characteristic curves



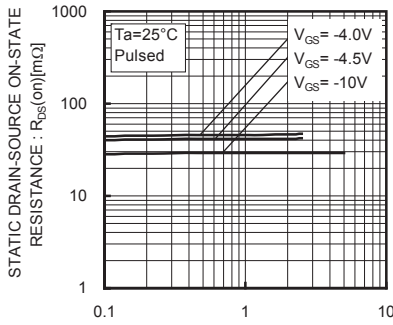
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]
Fig.1 Typical Output Characteristics (I)



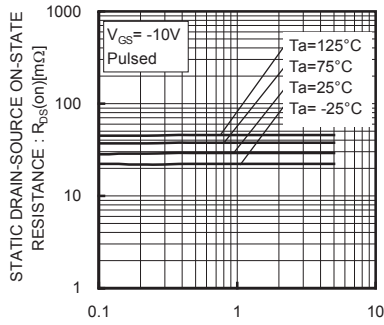
DRAIN-SOURCE VOLTAGE : $-V_{DS}$ [V]
Fig.2 Typical Output Characteristics (II)



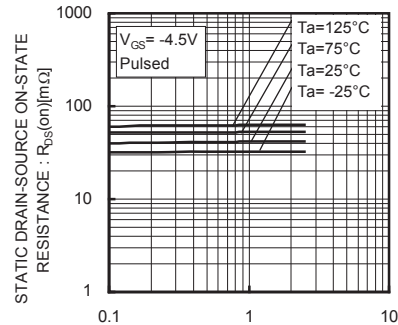
GATE-SOURCE VOLTAGE : $-V_{GS}$ [V]
Fig.3 Typical Transfer Characteristics



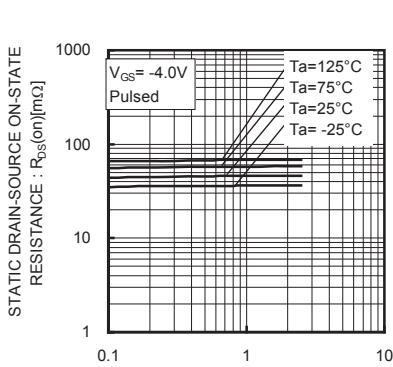
DRAIN-CURRENT : I_D [A]
Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)



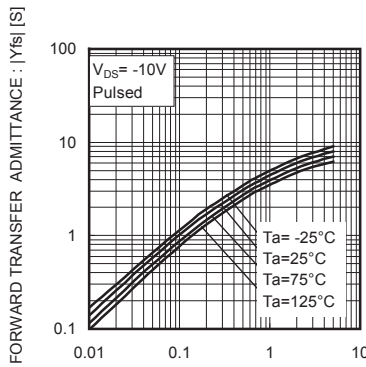
DRAIN-CURRENT : I_D [A]
Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)



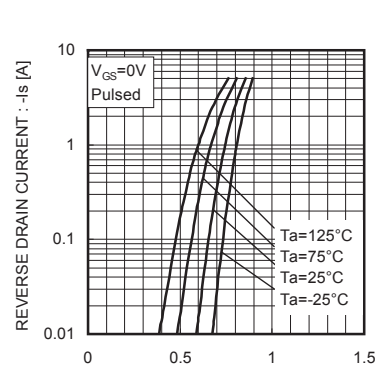
DRAIN-CURRENT : I_D [A]
Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)



DRAIN-CURRENT : I_D [A]
Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)



DRAIN-CURRENT : I_D [A]
Fig.8 Forward Transfer Admittance vs. Drain Current



SOURCE-DRAIN VOLTAGE : $-V_{SD}$ [V]
Fig.9 Reverse Drain Current vs. Source-Drain Voltage

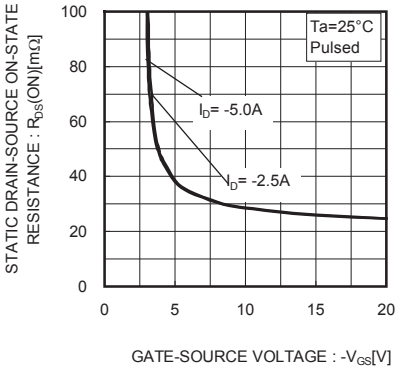
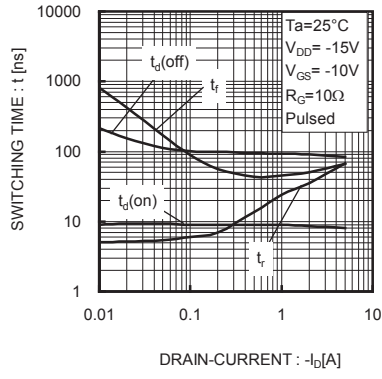


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage



.11 Switching Characteristics

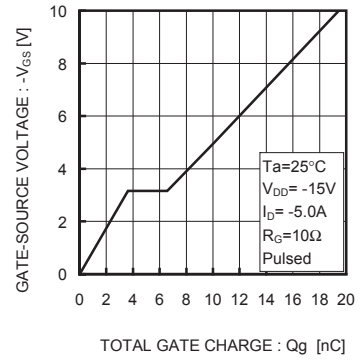


Fig.12 Dynamic Input Characteristics

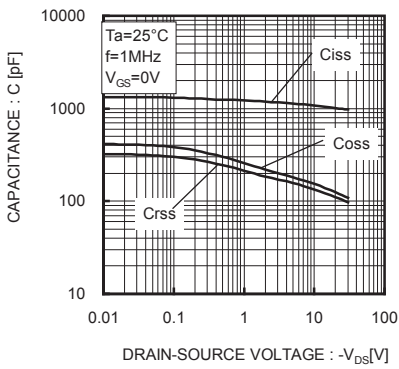


Fig.13 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

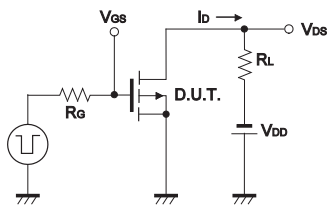


Fig.1-1 Switching Time Measurement Circuit

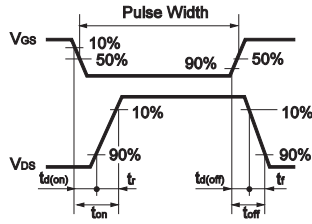


Fig.1-2 Switching Waveforms

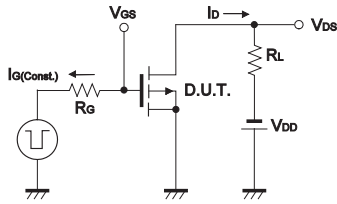


Fig.2-1 Gate Charge Measurement Circuit

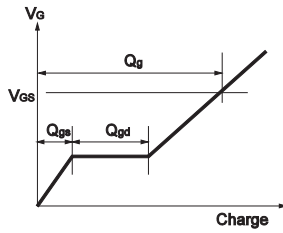


Fig.2-2 Gate Charge Waveform

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