National Semiconductor

DM74ALS1240A
Octal TRI-STATE® Bus Driver

General Description

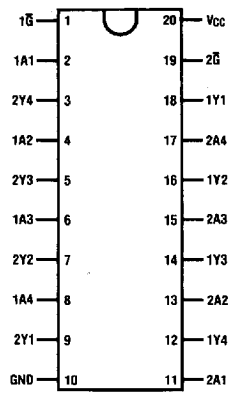
These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS240 and 'ALS241. The output TRI-STATE gating control is organized into two separate groups of four buffers. The 'ALS1240 control inputs symmetrically enable the respective outputs when set logic low. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS240, 241
- Low level drive current: 74ALS = 16 mA

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74ALS1240AWM
or DM74ALS1240AN
See NS Package Number M20B or N20A

Function Table

'ALS1240A

Input		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

H = High Level Logic State
L = Low Level Logic State
X = Don't Care (Either Low or High Level Logic State)
Z = High Impedance (Off) State

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	60.5°C/W
M Package	78.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74ALS1240A			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Operating Free Air Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			V
			I_{OH} = Max	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1240 Outputs High			5	8	mA
		Outputs Low			8	14	mA
		Outputs TRI-STATE			8	13	mA
		V_{CC} = 5.5V, ALS1241 Outputs High			7	11	mA
		Outputs Low			10	15	mA
		Outputs TRI-STATE			11	17	mA

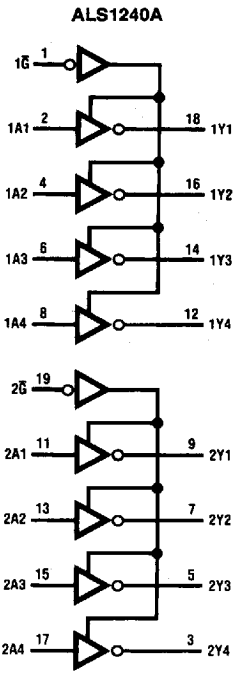
'ALS1240A Switching Characteristics

over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max		Units
				DM74ALS1240A		
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			2	13	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	Y	4	20	ns
t_{PZL}	Output Enable Time to Low Level Output			6	22	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	Y	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output			3	13	ns

Note 1: See Section 5 for test waveforms and output load.

Logic Diagram



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