PM5310

TBS™

TelecomBus Serializer

DATA SHEET

Proprietary and Confidential

Released

Issue 7 : November, 2001

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Revision History

Issue No.	Issue Date	Details of Change
1	Sept. 1999	Added func timing, registers, and operations sections.
2	Feb. 2000	Fixed Header, format of document, mechanical information, changed 1.8V to +- 5%, corrected LVDS diagram, added pinout, added pin #., changes res/resk to 3.16 from 4.75 k. Updated register descriptions and added numerous technical updates/corrections. DLL added.
3	May 2000	Updated active page switch over timing to switching two frames after CMP is asserted. Added J0 synchronization and initialization subsections. Changed connection information for ATB[0:1] pins. Added notes to registers 1A0, 1A1, 1C0, 1C1. Changed registers 132 - 137h, 142h, and 1CC to reserved. Changed indirect registers 0, 1, 2, 3 of address 1C1h to the correct indirect addresses 8, 9, A, and B respectively.
4	November 2000	Completed table 11. Changed the number of bytes req'd to go out of sync on PRBS monitors from 4 to 3. Updated section 14.9. Updated INCIJ0J1 bit definition to cover IJ0J1[1] override of IJ0J1[x] signals. Updated Monitor Error Count register definition to cover the possible counting of 2 extra bytes when losing sync. Updated section 14.9.2, the synci and syncv bit definitions to state that the prbs monitor's accumulator value must be checked after sync is declared to confirm that the monitor has not been falsely sync'd to an all 1 or all 0 pattern.

Issue No.	Issue Date	Details of Change
4 cont'd	November 2000	Clarified that syncv bit is only valid when monitor enabled. Also clarified synci in all register descriptions wrt concatenated payloads. Reg 53h was modified so that change, changei, refclki, sysclki bits were made reserved bits. Changed register Ch bit 15 from Reserved to unused. Clarified section 14.9.4 with regards to how error counts are accumulated for concatenated payloads. Changed bit 11 of reg21h, 31h, 41h to IP8ESEL from reserved. Added comment in 11.2.2 to indicate order of precedence in the 8b/10b encoding table. Clarified FUOI bit definition. Documented reg 52h, the DLL Reset register. Changed registers 1D0 and 1D1h to reserved (were the OT8D frame alignment status and interrupt bits). Clarified section 11.14 by stating OT8D operates in continuous character alignment. Changed max power from 4.2 W to 3.55 W. Changed all TIP bit occurrences from R/W to R. Changed OT8D interrupt and interrupt enable bits to reserved. In section 15.1 changed references about IJ0J1[4] and IPL[4] to IJ0J1[1] and IPL[1]. Removed from initialization section the writes to addr 135h, 145h, 155h etc. since they were unnecessary. Clarified the definition of the DLCV bit in the T8TE blocks. Corrected the information on how to force the PRGM blocks to transfer the accumulated error counts by writing to addr 05h or addr X0Ch (eg 10C, 20C etc). Clarified timing of TCMP, OCMP and RWSEL in pin descriptions. Numerous format/font changes. Updated absolute maximums table. Updated BSDL table. Changed "IDLE" (bit in multiple registers) to "CHARACTER OVERWRITE" and clarified the idle character description. Corrected title of reg 112h. Added Thaw parameter to the microprocessor write table. Added note in section 14.11 (point 4) about the need to write to the CSU registers on initialization. Added input pad tolerance spec to absolute maximum ratings section. Corrected point 8 in figure 10 to read S/UNI-MACH48 instead of TSE. Updated OPAIS pin description to indicate the signal is invalid during J0/Z0 timeslots.
4 cont'd	November 2000	Added note to receive LVDS pins and OJ0J1 pins to see section 14.19 with respect to using LVDS receive links independently. Added section 14.19. Added power consumption to the DC. Characteristics section. Clarified section 14.9 wrt PRGM non compatibility with external test equipment. IP8E_PRBS_ENA and ID8E_PRBS_ENA bits use clarified (see reg 101h, IADDR 8). Added 50 ma latch up current spec for RESK pin in Absolute Maximum Ratings section.

Issue No.	Issue Date	Details of Change
5	December, 2000	Modified I_{ILPU} D.C.Characteristics to be –200, -50, -4 µA. Added note in OPL pin description indicating OPL always high during H3 byte location when in MST mode. Modified registers 135h, 145h, 155h, to show bits 7 & 8 and registers 163h, 173h, 183h to show bits 12 and 13 and added notes to these registers w.r.t. disabling LVDS links for power savings. Added power up sequencing and Disabling Links for Power savings subsections (14.1 & 14.2). Added w.c. power for AVDH, AVDL, CSU_AVDH in D.C. Characteristics section.
5	January, 2001	Added descriptions for Registers 135h, 145h, 155h, 163h, 173h and 183h in the Register Memory Map. Added detail to power sequencing information. Added Section 14.1 power estimates. Added Sections 14.4 and 14.5. Added thermal information in Section 21.
5	January, 2001	Added note regarding FIFOERRI default value of “0” in Registers 0x131, 0x141, 0x151. Added note to 11.1.1 to explain that monitoring of TBS or MACH48 PRBS streams requires transmission in HPT mode. Added note that B1E1 insertion on the IP8E path will only occur if both B1E1_ENA and IP8E_PRBS_ENA are set to 1. Added warning about inadvertently clearing ERRORI when polling Register 0x53. Added TCB series termination note in Section 14.2. Removed erroneous statements that “for STS-Nc PRBS functions, only the master slice needs to be configured”. Added instructions to check CSU lock status and re-center transmit FIFOs in Section 14.17 (Initialization Procedure). Revealed TxDE Test Pattern registers. Fixed incorrect block instance references in the section that cross-references instance #2, #3 and #4 block registers to instance #1 register descriptions. Added Section 14.11 describing inter-relationships of receive decoder status bits. Added instructions for enabling RAPMI #1-#4 and RPTII based on datasheet errata.
5	February, 2001	Added JTAG AC Timing info. Changed temp spec from “Tc=-40 to +85C” to “Tc=-40C to Tj=+120C”. Clarified note on external interconnection of VDDI, VDDO, AVDH, AVDL pins. Changed VDDI spec to +/-5% from +/-10%. Changed VT+ limit in Section 17 from 2.0 to 2.2V and added SYSCLK to its pin list. Changed max power value from 3.55W to 2.95W. Changed max Iddop3.3V from 369mA to 330mA. Changed max Iddop1.8V from 1170mA to 1240mA. Added note to section 10 that Schmitt trigger inputs do not meet TTL levels. Added SYSCLK to Vth pin list in Section 17. Moved "LVDS Optimizations", "Hot Swapping" and "Trace Length" sections from "Functional Description" to "Operations". Added list of registers.

Issue No.	Issue Date	Details of Change
6	June, 2001	Updated Indirect Access section to discuss cases of BUSY bit being stuck at 1. Added J0RORDR bit on receive TSI blocks. Removed references to OT8D registers from the initialization procedure. Added description of AIS signals not being effected by PRBS insertion, which may over-ride attempts to insert a PRBS sequence into the SPE. Removed references to registers 110H, 120H from initialization section, included indirect access maximum BUSY times. Added Reset Timing. Changed JTAG ITV5[4] ID bit to 'H' to make JTAG version number 1H. Changed TBS Version/Part Number Register 012H to Default to 0x1531 (Changed VERSION field to 0x1)
6	July, 2001	Removed references to LPT mode. Added analog power supply filtering recommendations. Clarified which pins are AVDL and which are CSU_AVDL in pin description and diagram. Added functional description of DLL and corrected DLL register descriptions. Changed VDDO, AVDH spec to +/-5% from +/-10%. Added IDDOP on for AVDH, AVDL, VDDI, VDDO. Updated Power Sequencing to allow for hot swap of LVDS links. Added cycle times to complete Performance Counter Accumulation. Updated B1/E1 mismatch interrupt status.
7	Sept - Nov 2001	Clarified B1E1_ENA and Monitor B1E1 register to state that B1E1_ENA must be high before the Monitor B1E1 register will be updated with the current B1 and E1 values. Clarified LCVI description. Clarified pin description on IJ0J1 to state that V1 pulses on this input will cause errors. Added new Power Information section. Moved power filtering and sequencing into new section. Changed Ta=-40 to Tc=120 to Ta= -40 to Tj = 125 throughout. Updated thermal info. Added patents pending. Updated absolute max table. Changed device status to released.

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1 Features

- Encodes data from the Incoming parallel TelecomBus to a set of four working, a set of four protection, and a set of four auxiliary 777.6MHz (622Mbps) LVDS serial TelecomBus links with extended 8B/10B-based encoding.
- Decodes data from a set of four working, a set of four protection, and a set of four auxiliary 777.6MHz LVDS serial links with extended 8B/10B-based encoding to the Outgoing parallel TelecomBus stream.
- Provides capacity to carry an STS-12/STM-4 stream in each LVDS serial TelecomBus link. Four links can be aggregated to form an STS-48c/STM-16c stream.
- Provides capacity to carry an STS-12/STM-4 stream in each 8-bit bus of the parallel TelecomBus stream. Four 8-bit buses can be aggregated to carry an STS-48c/STM-16c stream.
- Provides redundant working, protection and auxiliary transmit LVDS serial TelecomBus streams and redundant receive LVDS serial TelecomBus streams for protection switching purposes.
- Supports through-traffic, drop-traffic and protection switching in UPSR, 2-fibre BLSR and 4-fibre BLSR applications in conjunction with a peer PM5310 TBS or companion PM5372 TSE^{TM} devices.
- Supports redundant working/protection time-space-time switch fabric.
- Provides Outgoing parallel TelecomBus selection of received Working, Protect, and Auxiliary data at STS-1 granularity.
- Provides independent time-slot interchange blocks on the Incoming and Outgoing parallel TelecomBus streams to allow arbitrary arrangement of time-slots at STS-1 granularity.
- Provides optional PRBS generation for each outgoing LVDS serial TelecomBus data link for off-line link verification.
- Provides optional PRBS generation for each 8-bit bus on the Outgoing parallel TelecomBus stream.
- Provides PRBS detection for each 8-bit bus on the Incoming parallel TelecomBus stream.
- Provides PRBS detection for each incoming LVDS serial TelecomBus stream for off-line link verification.
- Provides encoding of TelecomBus control signals at the multiplex section termination (MST) point and high-order path termination (HPT) point.
- Provides in-service link verification by optionally overwriting the B1 and E1 byte of each constituent STS-1/STM-0 with a unique software programmable byte and its complement.
- Uses extended 8B/10B-based line coding protocol on the serial links to provide transition density guarantee and DC balance and to offer a greater control character vocabulary than the standard 8B/10B protocol.

- Provides pins to coordinate updating of the connection map of the time-slot interchange blocks in the local device, peer TBS devices and companion PM5372 TSE devices.
- Derives all internal timing from a single 77.76MHz system clock.
- Provides a generic 16- bit microprocessor bus interface for configuration, control, and status monitoring.
- Implemented in 1.8V core and 3.3V I/O, 0.18µm CMOS and packaged in a 352 ball UBGA.
- Low power consumption of 2.82 W (typical).

2 Applications

- SONET/SDH Cross-connects
- SONET/SDH Add-Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- TelecomBus Backplane Driver

3 References

1. IEEE 802.3, “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications”, Section 36.2, 1998.

2. A.X. Widmer and P.A. Franaszek, “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code,” IBM Journal of Research and Development, Vol. 27, No 5, September 1983, pp 440-451.

3. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, “Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code,” December 4, 1984.

4. Telcordia Technologies – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, September 2000.

5. ITU, Recommendation G.707 - "Digital Transmission Systems – Terminal equipments - General", March 1996.

6. ITU, Rec Recommendation O.151 – “Error Performance Measuring Equipment Operating at the Primary Rate and Above", October 1992.

7. PMC-1990736, Transmit 8B/10B TelecomBus Encoder Telecom System Block Engineering Document, Issue 2.

8. PMC-1990735, Receive 8B/10B TelecomBus Decoder Telecom System Block Engineering Document, Issue 2.

9. PMC-1990758, SONET/SDH Time Slot Interchange Telecom System Block Engineering Document, Issue 2.

10. PMC-1990848, Pseudo Random Bit Sequence (PRBS) Generator and Monitor Telecom System Block Engineering Document, Issue 2.

11. PMC-1990737, CSU1250 and TXLVREF_1250 Analog Wrapper Telecom System Block Engineering Document, Issue 2.

4 Definitions

ADRU	Auxiliary Data Recovery Unit
CSTR	Clock Synthesis Unit (CSU)1250 and Transmit Low Voltage Reference (TXLVREF)1250 Analog Wrapper
DLL	Delay Lock Loop
DRU	Data Recovery Unit
FIFO	First-In-First-Out storage element
ID8E	Incoming Data 8B/10B Encoder
ITPP	Incoming TelecomBus PRBS Processor
IP8E	Incoming PRBS 8B/10B Encoder
LVDS	Low Voltage Differential Signaling
OTPG	Outgoing TelecomBus PRBS Generator
OT8D	Outgoing TelecomBus 8B/10B Decoder
PDRU	Protection Data Recovery Unit
PISO	Parallel to Serial Converter
PRBS	Pseudo-Random Bit Sequence
PRGM	SONET/SDH PRBS Generator/Monitor
RALV	Receive Auxiliary LVDS Interface
RA8D	Receive Auxiliary 8B/10B Decoder
RAPM	Receive Auxiliary PRBS Monitor
RATI	Receive Auxiliary Timeslot Interchange
RPLV	Receive Protection LVDS Interface
RP8D	Receive Protection 8B/10B Decoder
RPPM	Receive Protection PRBS Monitor
RPRM	Receive PRBS Monitor
RPTI	Receive Protection Timeslot Interchange
RWLV	Receive Working LVDS Interface
RW8D	Receive Working 8B/10B Decoder
RWPM	Receive Working PRBS Monitor
RWTI	Receive Working Timeslot Interchange
TADE	Transmit Auxiliary Disparity Encoder
TALV	Transmit Auxiliary LVDS Interface
TAPS	Transmit Auxiliary Serializer
TATI	Transmit Auxiliary Timeslot Interchange
TPDE	Transmit Protection Disparity Encoder
TPLV	Transmit Protection LVDS Interface
TPPS	Transmit Protection Serializer

TPTI	Transmit Protection Timeslot Interchange
TSI	Timeslot Interchange
TWDE	Transmit Working Disparity Encoder
TWLV	Transmit Working LVDS Interface
TWPS	Transmit Working Serializer
TWTI	Transmit Working Timeslot Interchange
WDRU	Working Data Recovery Unit

5 Application Examples

Figure 1 Multi-Service ATM/POS Switch Port Application

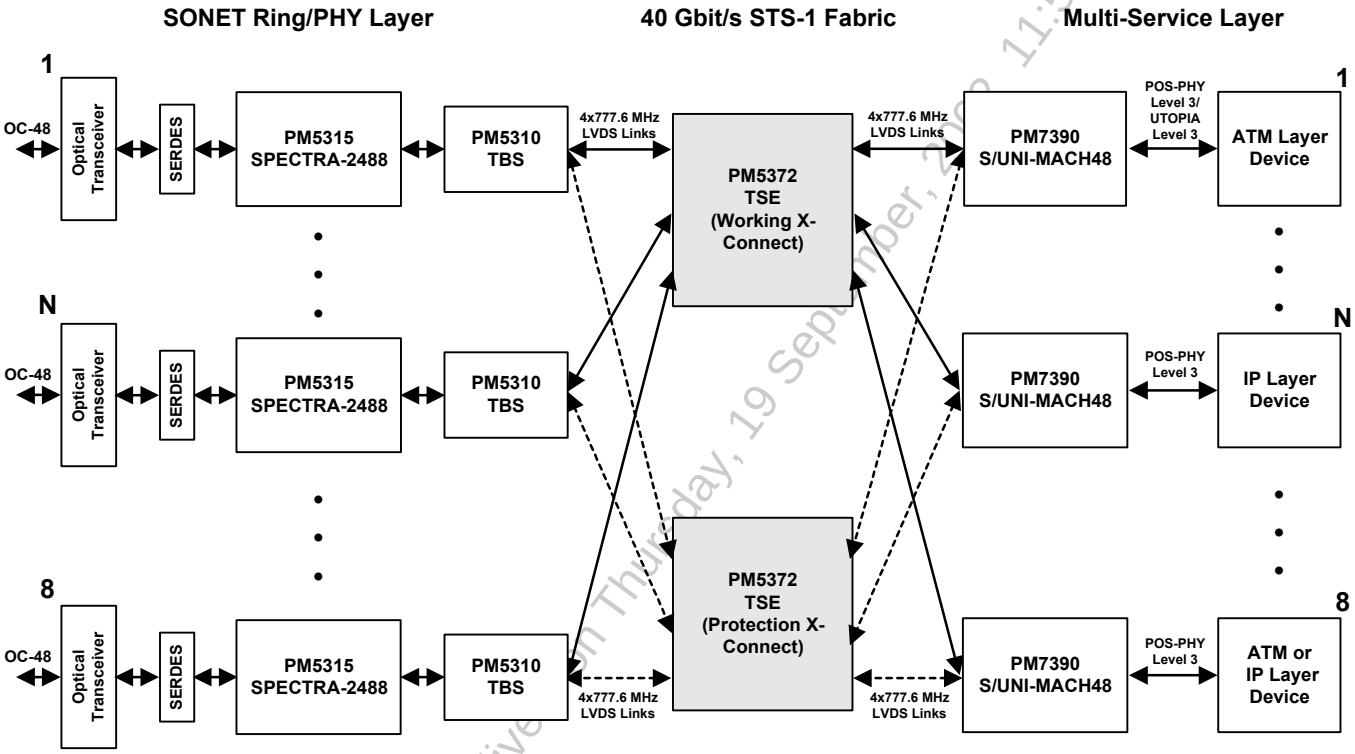
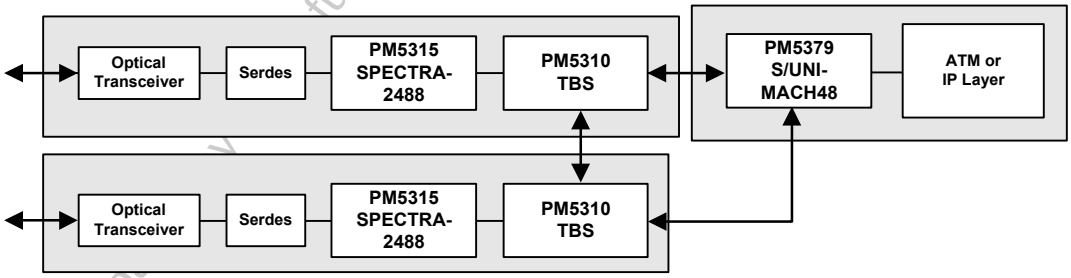
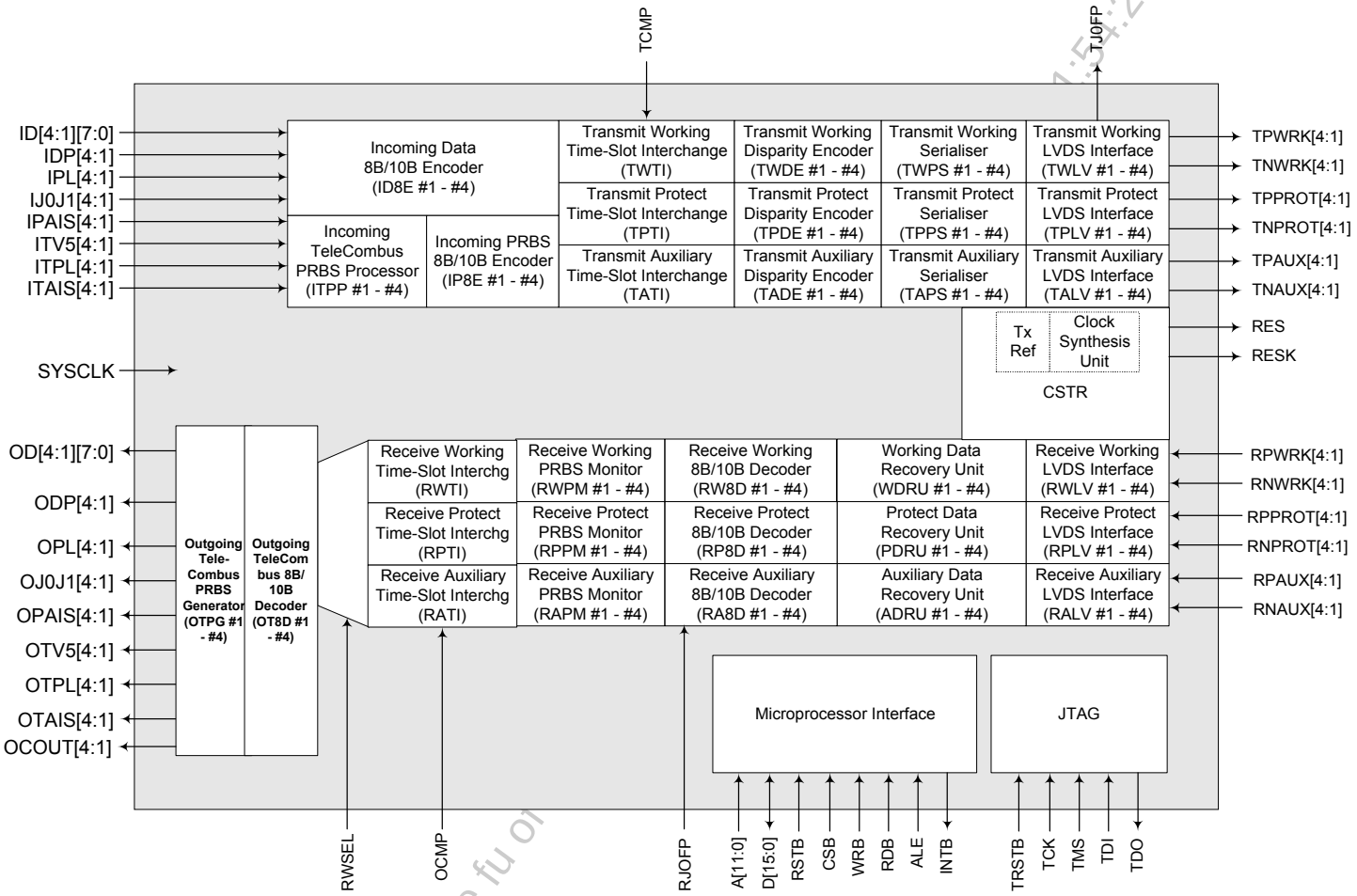


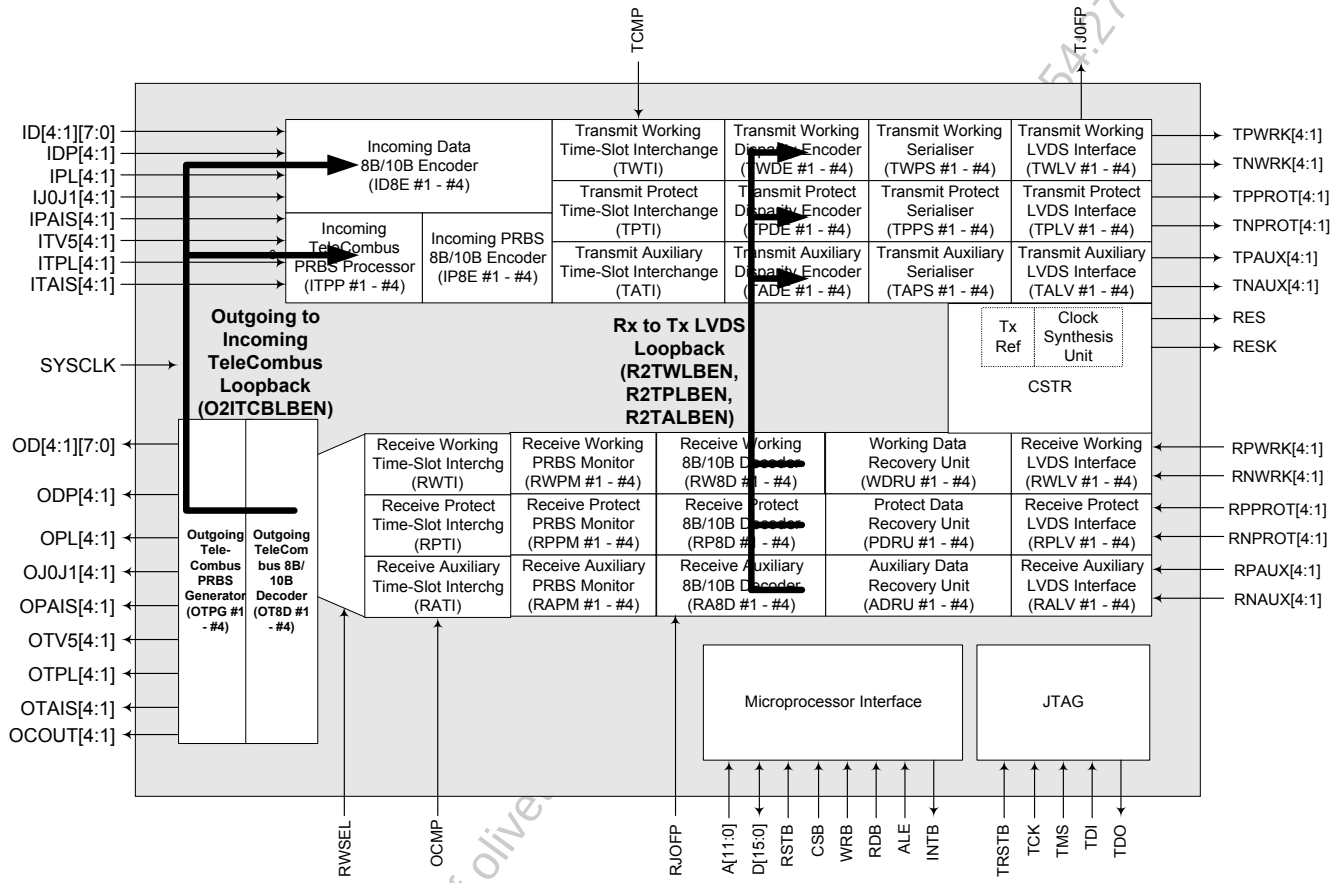
Figure 2 2.5 Gb/s Multi-service ADM

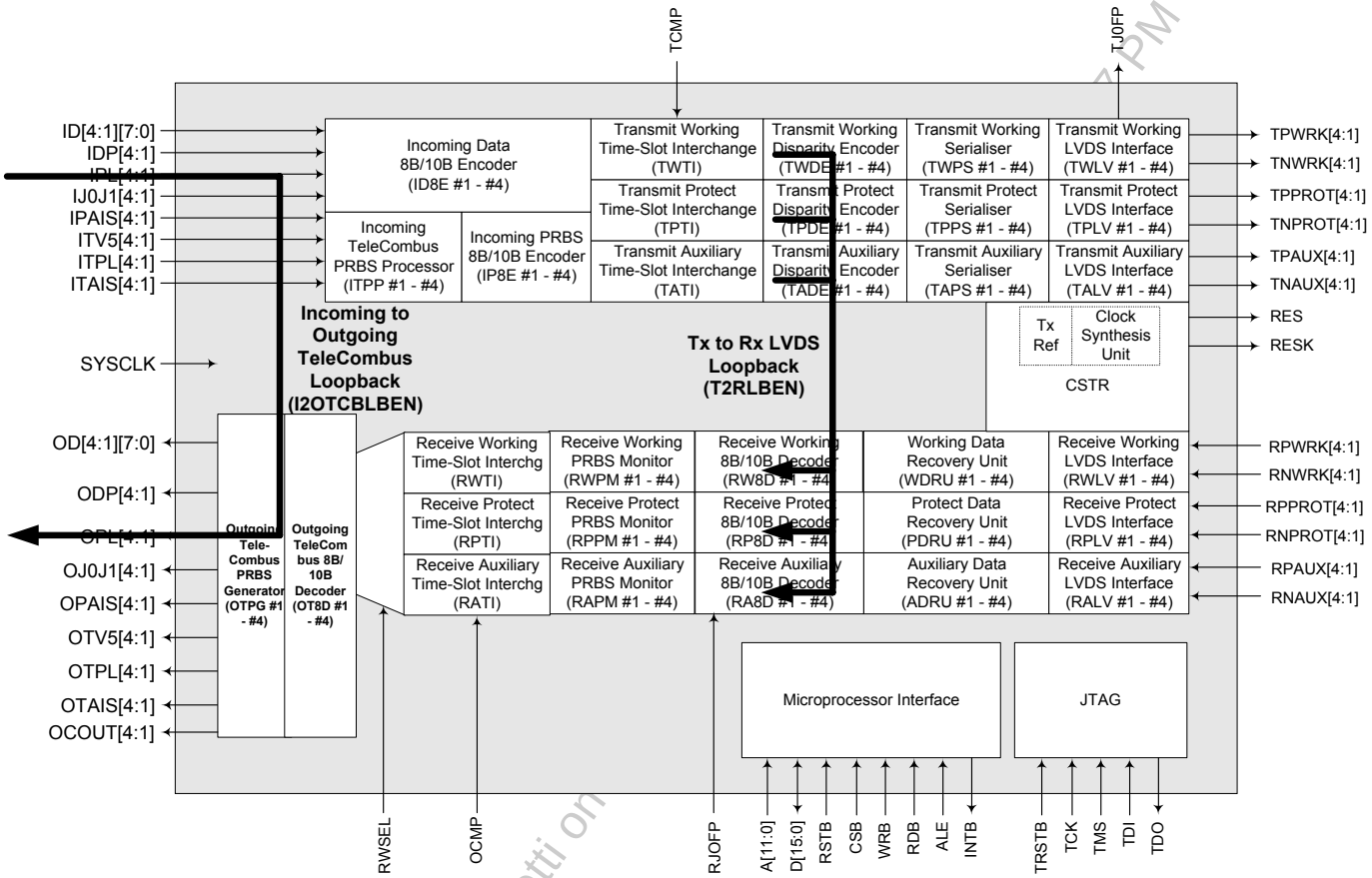


6 Block Diagram



7 Loopback Configurations





8 Description

The PM5310 TBS TelecomBus Serializer is a monolithic integrated circuit that implements conversion between byte-serial parallel TelecomBus and bit-serial 8B/10B-based serial TelecomBus data formats. The TBS can be used to connect SONET/SDH framer devices (e.g. PM5315 SPECTRA-2488 ™) to ATM/POS processor devices (e.g. PM7390 S/UNI®-MACH48), or to SONET/SDH cross-connect devices (e.g. PM5372 TSE ™). It can also be used to connect SONET/SDH tributary unit processors (e.g. PM5363 TUPP+622 ™) and PDH mapper devices (e.g. PM8315 TEMUX ™) to SONET/SDH cross-connect devices (e.g. PM5372 TSE).

In the ingress direction, the TBS connects an incoming parallel TelecomBus stream to a set of three LVDS serial TelecomBus links. The incoming parallel TelecomBus can carry an STS-48/STM-16 stream or four STS-12/STM-4 streams that share a common clock, and a common transport frame alignment. Incoming data is encoded into an extended set of 8B/10B characters and transferred onto three independent sets of 777.6 MHz LVDS serial TelecomBus links. Transport and payload frame boundaries, pointer justification events and alarm conditions are marked by 8B/10B control characters. A pseudo-random bit sequence (PRBS) processor is provided to monitor the incoming payload for the $X^{23} + X^{18} + 1$ pattern. Incoming payload bytes may be optionally overwritten with the locally generated PRBS pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the incoming TelecomBus stream. Time-slot interchange blocks are provided to allow arbitrary mapping of streams on the incoming parallel TelecomBus stream to each of the three sets of LVDS serial TelecomBus links at STS-1/AU3 granularity. Multicast is supported.

In the egress direction, the TBS connects three independent sets of 777.6 MHz LVDS serial TelecomBus links to an outgoing TelecomBus stream. Each link contains a constituent STS-12/STM-4 of an STS-48/STM-16 stream. Bytes on the links are carried as 8B/10B characters. The TBS decodes the characters into TelecomBus data and control signals. A pseudo-random bit sequence (PRBS) processor is provided to monitor the decoded payload for the $X^{23} + X^{18} + 1$ pattern. Decoded payload bytes may be optionally overwritten with the $X^{23} + X^{18} + 1$ pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle all legal mixes of STS-1/AU3, STS-3c/AU4, STS-12c/AU4-4c and STS-48c/AU4-16c in the LVDS links. Data on the outgoing TelecomBus stream may be sourced from arbitrary time-slots of any of the three sets of LVDS links.

9 Pin Diagram

The TBS is packaged in a custom Ultra-BGA with 352 balls.

Figure 3 Pin Diagram

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	OCMP	RSTB	NC	VDDI	INTB	NC	VDDI	A[3]	A[6]	A[9]	VSS	VSS	D[0]	D[3]	NC	D[9]	VDDI	D[15]	OD[1][0]	OD[1][2]	OD[1][6]	ODP[1]	VSS	VSS	A
B	VSS	VDDO	VSS	NC	NC	TRSTB	TDO	WRB	RDB	A[1]	A[4]	A[8]	A[10]	A(11)/TRS	D[1]	D[5]	D[7]	D[11]	D[14]	OPL[1]	VDDI	OD[1][5]	OCOUT[1]	VSS	VDDO	VSS	B
C	VSS	VSS	VDDO	TCMP	RWSEL	TCK	NC	NC	NC	ALE	A[2]	A[7]	NC	VDDI	D[2]	D[6]	D[10]	D[13]	OJOJ1[1]	OD[1][1]	OD[1][4]	NC	NC	VDDO	VSS	OTPL[1]	C
D	VSS	VSS	AVDH	VDDO	NC	VDDI	TMS	TDI	VDDO	CSB	A[0]	A[5]	NC	VDDO	D[4]	D[8]	D[12]	NC	VDDO	OD[1][3]	OD[1][7]	NC	VDDO	OPAIS[1]	OTV5[1]	VDDI	D
E	VSS	RES	AVDH	RESK																			OTAIS[1]	IJOJ1[1]	ID[1][0]	ID[1][3]	E
F	RNWRK[1]	RPWRK[1]	RNWRK[2]	RPWRK[2]																			IPL[1]	ID[1][1]	ID[1][4]	ID[1][6]	F
G	VSS	RNWRK[3]	RPWRK[3]	AVDL																			ID[1][2]	ID[1][5]	ID[1][7]	IDP[1]	G
H	RNWRK[4]	RPWRK[4]	TPWRK[1]	TNWRK[1]																			VDDO	VDDI	IPAIS[1]	ITV5[1]	H
J	VSS	TPWRK[2]	TNWRK[2]	AVDH																			NC	ITAIS[1]	VDDI	OPL[2]	J
K	TPWRK[3]	TNWRK[3]	TPWRK[4]	TNWRK[4]																			ITPL[1]	OJOJ1[2]	OD[2][1]	OD[2][3]	K
L	VSS	RNPROT[1]	RPPROT[1]	AVDL																			OD[2][0]	OD[2][2]	OD[2][4]	OD[2][6]	L
M	RNPROT[2]	RPPROT[2]	RNPROT[3]	RPPROT[3]																			OD[2][5]	OD[2][7]	OCOUT[2]	ODP[2]	M
N	RNPROT[4]	RPPROT[4]	CSU_AVDL	CSU_AVDH																			VDDO	OPAIS[2]	OTAIS[2]	VSS	N
P	TPPROT[1]	TNPROT[1]	CSU_AVDL	CSU_AVDL																			VDDI	OTV5[2]	OTPL[2]	VSS	P
R	TPPROT[3]	TNPROT[3]	TPPROT[2]	TNPROT[2]																			ID[2][2]	ID[2][0]	IPL[2]	IJOJ1[2]	R
T	VSS	TPPROT[4]	TNPROT[4]	AVDH																			NC	ID[2][4]	ID[2][3]	ID[2][1]	T
U	RNAUX[2]	RPAUX[2]	RNAUX[1]	RPAUX[1]																			ITAIS[2]	ID[2][7]	ID[2][5]	VDDI	U
V	VSS	RNAUX[3]	RPAUX[3]	AVDL																			VDDO	ITPL[2]	IDP[2]	ID[2][6]	V
W	TPAUX[1]	TNAUX[1]	RNAUX[4]	RPAUX[4]																			OD[3][0]	OJOJ1[3]	ITV5[2]	IPAIS[2]	W
Y	VSS	TPAUX[2]	TNAUX[2]	AVDH																			OD[3][4]	OD[3][1]	OPL[3]	VDDI	Y
AA	TPAUX[4]	TNAUX[4]	TPAUX[3]	TNAUX[3]																			OD[3][7]	NC	OD[3][2]	NC	AA
AB	VSS	ATB1	AVDH	ATB0																			ODP[3]	NC	OD[3][5]	OD[3][3]	AB
AC	VSS	VSS	AVDH	VDDO	TJ0FP	ITAIS[4]	ID[4][6]	VDDO	NC	NC	NC	OCOUT[4]	VDDO	NC	OPL[4]	NC	ID[3][7]	VDDO	ID[3][2]	NC	NC	OTAIS[3]	VDDO	NC	VDDI	OD[3][6]	AC
AD	VSS	VSS	VDDO	RJ0FP	VDDI	ID[4][7]	VDDI	ID[4][1]	IPL[4]	OTV5[4]	OPAIS[4]	OD[4][6]	OD[4][3]	OD[4][1]	SYSCLK	ITV5[3]	IPAIS[3]	ID[3][6]	ID[3][4]	VDDI	IPL[3]	OTV5[3]	OPAIS[3]	VDDO	VSS	OCOUT[3]	AD
AE	VSS	VDDO	VSS	ITPL[4]	IDP[4]	ID[4][4]	ID[4][2]	NC	VDDI	OTAIS[4]	NC	OD[4][5]	NC	OD[4][2]	VDDI	OJOJ1[4]	ITPL[3]	IDP[3]	VDDI	NC	ID[3][1]	VDDI	OTPL[3]	VSS	VDDO	VSS	AE
AF	VSS	VSS	ITV5[4]	IPAIS[4]	ID[4][5]	ID[4][3]	ID[4][0]	IJOJ1[4]	OTPL[4]	ODP[4]	OD[4][7]	OD[4][4]	VSS	VSS	OD[4][0]	NC	NC	ITAIS[3]	NC	ID[3][5]	ID[3][3]	ID[3][0]	IJOJ1[3]	NC	VSS	VSS	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

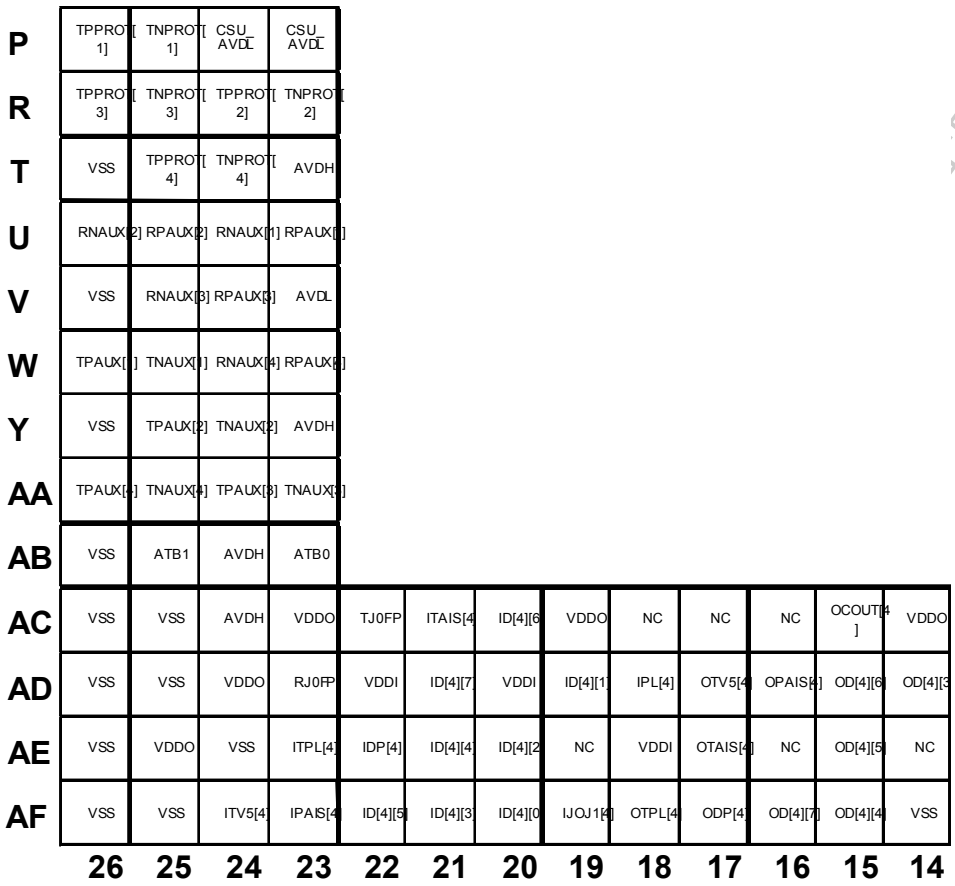
Figure 4 Pin Diagram Top Left Corner

	26	25	24	23	22	21	20	19	18	17	16	15	14
A	VSS	VSS	OCMP	RSTB	NC	VDDI	INTB	NC	VDDI	A[3]	A[6]	A[9]	VSS
B	VSS	VDDO	VSS	NC	NC	TRSTB	TDO	WRB	RDB	A[1]	A[4]	A[8]	A[10]
C	VSS	VSS	VDDO	TCMP	RWSEL	TCK	NC	NC	NC	ALE	A[2]	A[7]	NC
D	VSS	VSS	AVDH	VDDO	NC	VDDI	TMS	TDI	VDDO	CSB	A[0]	A[5]	NC
E	VSS	RES	AVDH	RESK									
F	RNWRK[1]	RPWRK[1]	RNWRK[2]	RPWRK[2]									
G	VSS	RNWRK[3]	RPWRK[3]	AVDL									
H	RNWRK[4]	RPWRK[4]	TPWRK[1]	TNWRK[1]									
J	VSS	TPWRK[2]	TNWRK[2]	AVDH									
K	TPWRK[3]	TNWRK[3]	TPWRK[4]	TNWRK[4]									
L	VSS	RNPROT[1]	RPPROT[1]	AVDL									
M	RNPROT[2]	RPPROT[2]	RNPROT[3]	RPPROT[3]									
N	RNPROT[4]	RPPROT[4]	CSU_AVDL	CSU_AVDH									

Figure 5 Pin Diagram Top Right Corner

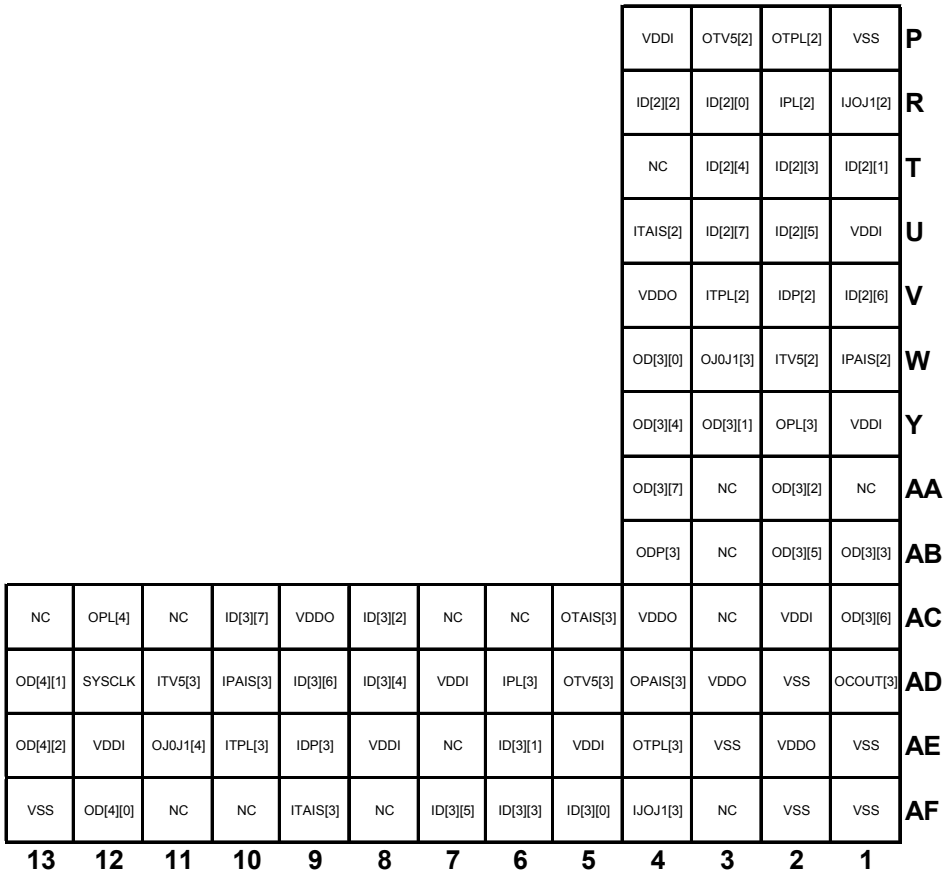
13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	D[0]	D[3]	NC	D[9]	VDDI	D[15]	OD[1][0]	OD[1][2]	OD[1][6]	ODP[1]	VSS	VSS	A
A[11]/TRS	D[1]	D[5]	D[7]	D[11]	D[14]	OPL[1]	VDDI	OD[1][5]	OCOUT[1]	VSS	VDDO	VSS	B
VDDI	D[2]	D[6]	D[10]	D[13]	OJ0J1[1]	OD[1][1]	OD[1][4]	NC	NC	VDDO	VSS	OTPL[1]	C
VDDO	D[4]	D[8]	D[12]	NC	VDDO	OD[1][3]	OD[1][7]	NC	VDDO	OPAIS[1]	OTV5[1]	VDDI	D
									OTAIS[1]	IJOJ1[1]	ID[1][0]	ID[1][3]	E
									IPL[1]	ID[1][1]	ID[1][4]	ID[1][6]	F
									ID[1][2]	ID[1][5]	ID[1][7]	IDP[1]	G
									VDDO	VDDI	IPAIS[1]	ITV5[1]	H
									NC	ITAIS[1]	VDDI	OPL[2]	J
									ITPL[1]	OJ0J1[2]	OD[2][1]	OD[2][3]	K
									OD[2][0]	OD[2][2]	OD[2][4]	OD[2][6]	L
									OD[2][5]	OD[2][7]	OCOUT[2]	ODP[2]	M
									VDDO	OPAIS[2]	OTAIS[2]	VSS	N

Figure 6 Pin Diagram Bottom Left Corner



	26	25	24	23	22	21	20	19	18	17	16	15	14
P	TPPROT[1]	TNPROT[1]	CSU_AVDL	CSU_AVDL									
R	TPPROT[3]	TNPROT[3]	TPPROT[2]	TNPROT[2]									
T	VSS	TPPROT[4]	TNPROT[4]	AVDH									
U	RNAUX[2]	RPAUX[2]	RNAUX[1]	RPAUX[1]									
V	VSS	RNAUX[3]	RPAUX[3]	AVDL									
W	TPAUX[1]	TNAUX[1]	RNAUX[4]	RPAUX[4]									
Y	VSS	TPAUX[2]	TNAUX[2]	AVDH									
AA	TPAUX[4]	TNAUX[4]	TPAUX[3]	TNAUX[3]									
AB	VSS	ATB1	AVDH	ATB0									
AC	VSS	VSS	AVDH	VDDO	TJ0FP	ITAIS[4]	ID[4][6]	VDDO	NC	NC	NC	OCOUT[4]	VDDO
AD	VSS	VSS	VDDO	RJ0FP	VDDI	ID[4][7]	VDDI	ID[4][1]	IPL[4]	OTV5[4]	OPAIS[4]	OD[4][6]	OD[4][3]
AE	VSS	VDDO	VSS	ITPL[4]	IDP[4]	ID[4][4]	ID[4][2]	NC	VDDI	OTAIS[4]	NC	OD[4][5]	NC
AF	VSS	VSS	ITV5[4]	IPAIS[4]	ID[4][5]	ID[4][3]	ID[4][0]	IJOJ1[4]	OTPL[4]	ODP[4]	OD[4][7]	OD[4][4]	VSS

Figure 7 Pin Diagram Bottom Right Corner



13	12	11	10	9	8	7	6	5	4	3	2	1	
									VDDI	OTV5[2]	OTPL[2]	VSS	P
									ID[2][2]	ID[2][0]	IPL[2]	IJOJ1[2]	R
									NC	ID[2][4]	ID[2][3]	ID[2][1]	T
									ITAIS[2]	ID[2][7]	ID[2][5]	VDDI	U
									VDDO	ITPL[2]	IDP[2]	ID[2][6]	V
									OD[3][0]	OJ0J1[3]	ITV5[2]	IPAIS[2]	W
									OD[3][4]	OD[3][1]	OPL[3]	VDDI	Y
									OD[3][7]	NC	OD[3][2]	NC	AA
									ODP[3]	NC	OD[3][5]	OD[3][3]	AB
NC	OPL[4]	NC	ID[3][7]	VDDO	ID[3][2]	NC	NC	OTAIS[3]	VDDO	NC	VDDI	OD[3][6]	AC
OD[4][1]	SYSCLK	ITV5[3]	IPAIS[3]	ID[3][6]	ID[3][4]	VDDI	IPL[3]	OTV5[3]	OPAIS[3]	VDDO	VSS	OCOUT[3]	AD
OD[4][2]	VDDI	OJ0J1[4]	ITPL[3]	IDP[3]	VDDI	NC	ID[3][1]	VDDI	OTPL[3]	VSS	VDDO	VSS	AE
VSS	OD[4][0]	NC	NC	ITAIS[3]	NC	ID[3][5]	ID[3][3]	ID[3][0]	IJOJ1[3]	NC	VSS	VSS	AF

10 Pin Description

Pin Name	Type	Pin No.	Function
Receive Serial Data Interface (25 Signals)			
RPWRK[4] RNWRK[4] RPWRK[3] RNWRK[3] RPWRK[2] RNWRK[2] RPWRK[1] RNWRK[1]	Analog LVDS Input	H25 H26 G24 G25 F23 F24 F25 F26	**Receive Working Serial Data.** The differential receive working serial data links (RPWRK[4:1]/RNWRK[4:1]) carry the receive SONET/SDH STS-48 frame data from an upstream working source, in bit serial format. Each differential pair carries a constituent STS-12 of the receive working stream. Data on RPWRK[*X*]/RNWRK[*X*] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential pairs in RPWRK[4:1]/RNWRK[4:1] are frequency locked but not phase locked. RPWRK[4:1]/RNWRK[4:1] are nominally 777.6 MHz data streams. Unused LVDS inputs may be left floating, or the inputs may be grounded. In either case the analog blocks (RXLV and the DRU) should be disabled to reduce power consumption. Tying one pin high and the corresponding pin of an input pair low will apply voltage across the internal termination resistor, which will increase system power consumption. Note: please refer to section 14.19 for information on using the receive LVDS links independently.
RPPROT[4] RNPROT[4] RPPROT[3] RNPROT[3] RPPROT[2] RNPROT[2] RPPROT[1] RNPROT[1]		N25 N26 M23 M24 M25 M26 L24 L25	**Receive Protection Serial Data.** The differential receive protection serial data links (RPPROT[4:1]/RNPROT[4:1]) carry the receive SONET/SDH STS-48 frame data from an upstream protection source, in bit serial format. Each differential pair carries a constituent STS-12 of the receive protection stream. Data on RPPROT[*X*]/RNPROT[*X*] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. The four differential signal pairs in RPPROT[4:1]/RNPROT[4:1] are frequency locked but not phase locked. RPPROT[4:1]/RNPROT[4:1] are nominally 777.6 MHz data streams. Unused LVDS inputs may be left floating, or the inputs may be grounded. In either case the analog blocks (RXLV and the DRU) should be disabled to reduce power consumption. Tying one pin high and the corresponding pin of an input pair low will apply voltage across the internal termination resistor, which will increase system power consumption. Note: please refer to section 14.19 for information on using the receive LVDS links independently.

Pin Name	Type	Pin No.	Function
RPAUX[4] RNAUX[4] RPAUX[3] RNAUX[3] RPAUX[2] RNAUX[2] RPAUX[1] RNAUX[1]	Analog LVDS Input	W23 W24 V24 V25 U25 U26 U23 U24	**Receive Auxiliary Serial Data.** The differential receive auxiliary serial data links (RPAUX[4:1]/RNAUX[4:1]) carry the receive SONET/SDH STS-48 frame data from an upstream auxiliary source, in bit serial format. Each differential pair carries a constituent STS-12 of the receive auxiliary stream. Data on RPAUX[*X*]/RNAUX[*X*] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is transmitted first and the bit ‘j’ is transmitted last. The four differential pairs in RPAUX[4:1]/RNAUX[4:1] are frequency locked but not phase locked. RPAUX[4:1]/RNAUX[4:1] are nominally 777.6 MHz data streams. Unused LVDS inputs may be left floating, or the inputs may be grounded. In either case the analog blocks (RXLV and the DRU) should be disabled to reduce power consumption. Tying one pin high and the corresponding pin of an input pair low will apply voltage across the internal termination resistor, which will increase system power consumption. Note: please refer to section 14.19 for information on using the receive LVDS links independently.
RJ0FP	Input	AD23	**Receive Serial Interface Frame Pulse.** The receive serial interface frame pulse signal (RJ0FP) provides system timing of the receive serial interface. RJ0FP is set high once every 9720 SYSCLK cycles, or integer multiples thereof, to indicate that a 125 μs J0 frame boundary has been received. The RJ0DLY[13:0] bits (register 005h) are used to align the J0 character on the Receive Serial TelecomBus interface (RPWRK[4:1]/RNWRK[4:1], RPWRK[4:1]/RNWRK[4:1], and RPAUX[4:1]/RNAUX[4:1]) with RJ0FP. RJ0FP is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Outgoing TelecomBus stream (64 Signals)			
OD[4][7] OD[4][6] OD[4][5] OD[4][4] OD[4][3] OD[4][2] OD[4][1] OD[4][0] OD[3][7] OD[3][6] OD[3][5] OD[3][4] OD[3][3] OD[3][2] OD[3][1] OD[3][0] OD[2][7] OD[2][6] OD[2][5] OD[2][4] OD[2][3] OD[2][2] OD[2][1] OD[2][0] OD[1][7] OD[1][6] OD[1][5] OD[1][4] OD[1][3] OD[1][2] OD[1][1] OD[1][0]	Output	AF16 AD15 AE15 AF15 AD14 AE13 AD13 AF12 AA4 AC1 AB2 Y4 AB1 AA2 Y3 W4 M3 L1 M4 L2 K1 L3 K2 L4 D6 A4 B5 C6 D7 A5 C7 A6	**Outgoing Data.** The outgoing data buses (OD[4][7:0], OD[3][7:0], OD[2][7:0], OD[1][7:0]) carry the SONET/SDH OC-48 frame data in byte serial format. OD[*x*][7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit transmitted first. OD[*x*][0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit transmitted last. Each of the four outgoing data buses carries a constituent STS-12 stream, which are transport frame aligned. OD[1][7:0] carries the first STS-12 stream transmitted while OD[4][7:0] carries the last. Association of STS-1 octets in OD[*x*][7:0] to data in the receive working LVDS links, the receive protection LVDS links and the receive auxiliary LVDS links is software configurable. OD[*x*][7:0] are updated on the rising edge of SYSCLK.
ODP[4] ODP[3] ODP[2] ODP[1]	Output	AF17 AB4 M1 A3	**Outgoing Data Parity.** The outgoing data parity bus (ODP[4:1]) reports the parity of the corresponding outgoing data bus (OD[4:1][7:0]), and may optionally include OJ0J1[4:1] and OPL[4:1] in the calculation. ODP[*x*] reports odd parity on the outgoing parallel TelecomBus when the OOP register bit is set high and even parity when the OOP register bit is set low. ODP[*x*] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
OPL[4] OPL[3] OPL[2] OPL[1]	Output	AC12 Y2 J1 B7	**Outgoing Payload Active.** The outgoing payload active bus (OPL[4:1]) distinguishes between transport overhead bytes and synchronous payload / high order virtual container bytes in the corresponding outgoing data bus (OD[4:1][7:0]). OPL[*x*] is set high to mark each payload / HO-VC byte on OD[*x*][7:0] and set low to mark each transport overhead byte on OD[*x*][7:0]. OPL[4:1] is updated on the rising edge of SYSCLK. Note: when in MST mode, OPL is set high during H3 byte locations since H1/H2 pointer interpretation has not yet been performed. In HPT mode, OPL indicates whether H3 is part of the payload or not.
OJ0J1[4] OJ0J1[3] OJ0J1[2] OJ0J1[1]	Output	AE11 W3 K3 C8	**Outgoing Composite Transport and Payload Frame Pulse.** The outgoing composite transport and payload frame pulse bus (OJ0J1[4:1]) identifies the STS/STM frame and the synchronous payload envelope / high order virtual container frame boundaries on the corresponding outgoing data bus (OD[4:1][7:0]). All four OJ0J1[4:1] are set high and all four OPL[4:1] are set low simultaneously to mark the first J0 byte of the STS/STM frame on the OD[1][7:0] bus. OJ0J1[*x*] is set high when OPL[*x*] is set high to mark each J1 byte of the SPE / HO-VC frame on the OD[*x*][7:0] bus. OJ0J1[4:1] is updated on the rising edge of SYSCLK. Note: J0 indications are caused by the RJ0FP input and RJ0DLY information, and so are under system control. J0 indications will occur every 125us even if RJ0FP only occurs at some multiple of 125us greater than one. J1 indications are derived from information received on the serial data links, so are not under system control.
OPAIS[4] OPAIS[3] OPAIS[2] OPAIS[1]	Output	AD16 AD4 N3 D3	**Outgoing High-order Path Alarm Indication Signal.** The outgoing high-order path Alarm Indication Signal bus (OPAIS[4:1]) identifies bytes of STS-N/STM-M streams that are in high-order path AIS alarm on the corresponding outgoing data bus (OD[4:1][7:0]). OPAIS[*x*] is set high to mark the stream in AIS alarm on the OD[*x*][7:0] bus. OPAIS[4:1] is valid during all bytes when J0/Z0 switching is enabled in the RTSI blocks, otherwise the contents of OPAIS[4:1] are invalid during the J0/Z0 bytes only. OPAIS[4:1] is updated on the rising edge of SYSCLK.
OCOUT[4] OCOUT[3] OCOUT[2] OCOUT[1]		AC15 AD1 M2 B4	**Outgoing Controllable Output.** The outgoing controllable output bus (OCOUT[4:1]) marks SONET/SDH octets on the corresponding outgoing data bus (OD[4:1][7:0]) on a per STS-1 basis. It is controlled by the COUT*x* register bits in the Outgoing TelecomBus PRBS Generator (OTPG) block. OCOUT[4:1] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
OTV5[4] OTV5[3] OTV5[2] OTV5[1]	Output	AD17 AD5 P3 D2	**Outgoing Tributary Payload Frame Pulse.** The outgoing tributary payload frame pulse bus (OTV5[4:1]) identifies the tributary synchronous payload envelope / low order virtual container frame boundaries on the corresponding outgoing data bus (OD[4:1][7:0]). OTV5[*x*] is set high to mark the various V5 bytes on the OD[*x*][7:0] bus. The OTV5[x] signal is asserted high when the device has received a low order path frame alignment 8B/10B character on serial links from a device which supports LPT encoding. OTV5[4:1] is updated on the rising edge of SYSCLK.
OTPL[4] OTPL[3] OTPL[2] OTPL[1]	Output	AF18 AE4 P2 C1	**Outgoing Tributary Payload Active.** The outgoing tributary payload active bus (OTPL[4:1]) is set high to mark each tributary synchronous payload / low order virtual container byte in the corresponding outgoing data bus (OD[4:1][7:0]). OTPL[*x*] is set low at STS/STM transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1, V2, V3 and V4). The OTPL[x] signal is asserted high when the device has received a non low order path payload overhead 8B/10B character (RSOH, MSOH, POH, R, V1, V2, V3, V4) on serial links from a device which supports LPT encoding. OTPL[4:1] is updated on the rising edge of SYSCLK.
OTAIS[4] OTAIS[3] OTAIS[2] OTAIS[1]	Output	AE17 AC5 N2 E4	**Outgoing Low-order Path Alarm Indication Signal.** The outgoing low-order path Alarm Indication Signal bus (OTAIS[4:1]) identifies bytes of tributary unit streams that are in low-order path AIS alarm on the corresponding outgoing data bus (OD[4:1][7:0]). The OTAIS[x] signal is generated when the device has received a low order path AIS 8B/10B character on serial links from a device which supports LPT encoding. OTAIS[*x*] is set high to mark the stream in AIS alarm on the OD[*x*][7:0] bus. OTAIS[4:1] is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Input TelecomBus stream (60 Signals)			
ID[4][7] ID[4][6] ID[4][5] ID[4][4] ID[4][3] ID[4][2] ID[4][1] ID[4][0] ID[3][7] ID[3][6] ID[3][5] ID[3][4] ID[3][3] ID[3][2] ID[3][1] ID[3][0] ID[2][7] ID[2][6] ID[2][5] ID[2][4] ID[2][3] ID[2][2] ID[2][1] ID[2][0] ID[1][7] ID[1][6] ID[1][5] ID[1][4] ID[1][3] ID[1][2] ID[1][1] ID[1][0]	Input	AD21 AC20 AF22 AE21 AF21 AE20 AD19 AF20 AC10 AD9 AF7 AD8 AF6 AC8 AE6 AF5 U3 V1 U2 T3 T2 R4 T1 R3 G2 F1 G3 F2 E1 G4 F3 E2	**Incoming Data.** The incoming data buses (ID[4][7:0], ID[3][7:0], ID[2][7:0], ID[1][7:0]) carry the SONET/SDH STS-48 frame data in byte serial format. ID[*x*][7] is the most significant bit, corresponding to bit 1 of each SONET/SDH octet, the bit transmitted first. ID[*x*][0] is the least significant bit, corresponding to bit 8 of each SONET/SDH octet, the bit transmitted last. Each of the four incoming data buses carries a constituent STS-12 stream, which are transport frame aligned. ID[1][7:0] carries the first STS-12 stream transmitted while ID[4][7:0] carries the last. Association of STS-1 octets in ID[*x*][7:0] to data in the transmit working serial data links, the transmit protection serial data links, and the auxiliary serial data links is configured by the Transmit TelecomBus Time-slot Interchange blocks. ID[*x*][7:0] are sampled on the rising edge of SYSCLK.
IDP[4] IDP[3] IDP[2] IDP[1]	Input	AE22 AE9 V2 G1	**Incoming Data Parity.** The incoming data parity bus (IDP[4:1]) reports the parity of the corresponding incoming parallel TelecomBus, and may optionally include IJ0J1[4:1] and IPL[4:1] in the calculation. IDP[*x*] is expected to report odd parity relative when the IOP register bit is set high and even parity when the IOP register bit is set low. IDP[*x*] is sampled on the rising edge of SYSCLK. See note on the INCIJ0J1 in the register description section with regards to including IJ0J1 in parity calculations.

Pin Name	Type	Pin No.	Function
IPL[4] IPL[3] IPL[2] IPL[1]	Input	AD18 AD6 R2 F4	**Incoming Payload Active.** The incoming payload active bus (IPL[4:1]) distinguishes between transport overhead / section overhead bytes from synchronous payload / high order virtual container bytes in the corresponding incoming data bus (ID[4:1][7:0]). IPL[*x*] is set high to mark each payload / HO-VC byte on OD[*x*][7:0] and set low to mark each transport overhead / section overhead byte on ID[*x*][7:0]. IPL[4:1] is sampled on the rising edge of SYSCLK.
IJ0J1[4] IJ0J1[3] IJ0J1[2] IJ0J1[1]	Input	AF19 AF4 R1 E3	**Incoming Composite Transport and Payload Frame Pulse.** The incoming composite transport and payload frame pulse bus (IJ0J1[4:1]) identifies the STS/STM frame and the synchronous payload envelope / high order virtual container frame boundaries on the corresponding incoming data bus (ID[4:1][7:0]). IJ0J1[1] should be set high and IPL[1] is set low to mark the first J0 byte of the STS/STM frame on the four ID[*x*][7:0] buses. IJ0J1[4:2] should be set high when IJ0J1[1] is set high to mark the first J0 byte. Incoming TelecomBus streams must have a common transport frame alignment. IJ0J1[*x*] should be set high when IPL[*x*] is set high to mark each J1 byte of the SPE / HO-VC frame on the ID[*x*][7:0] bus. IJ0J1[4:1] is sampled on the rising edge of SYSCLK. Note that some PMC framers, such as the SPECTRA – 622, have an output pin that is capable of sourcing pulses to indicate the presence of J0, J1, and V1 data on the data bus. V1 pulses must not be present on the IJ0J1 pins as they will be interpreted as J1 pulses and will corrupt the datasteam. Devices such as the SPECTRA –622 must have the pulsing on V1 bytes disabled. This can be done by disabling the feature through a register on the device.
IPAIS[4] IPAIS[3] IPAIS[2] IPAIS[1]	Input	AF23 AD10 W1 H2	**Incoming High Order Path AIS.** The incoming high order path alarm bus (IPAIS[4:1]) identifies STS/STM streams on the corresponding incoming data bus (ID[4:1][7:0]) that are in high order path AIS state. IPAIS[*x*] is set high when the stream on ID[*x*][7:0] is in AIS and is set low when the stream is out of AIS state. When IPAIS[x] is asserted an 8B/10B control character indicating Path AIS will be transmitted instead of the data on the corresponding ID[x][7:0] bus. IPAIS[4:1] should not be asserted during the J0/Z0 byte, as these bytes are not switched with the related path. IPAIS[4:1] is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
ITV5[4] ITV5[3] ITV5[2] ITV5[1]	Input	AF24 AD11 W2 H1	**Incoming Tributary Payload Frame Pulse.** The incoming tributary payload frame pulse bus (ITV5[4:1]) identifies the tributary synchronous payload envelope / low order virtual container frame boundaries on the corresponding incoming data bus (ID[4:1][7:0]). ITV5[*x*] is set high to mark the various V5 bytes on the ID[*x*][7:0] bus. The ITV5[x] signal may be used in loopback modes, but will not affect the 8B/10B encoding operation of the TBS. ITV5[4:1] is sampled on the rising edge of SYSCLK.
ITPL[4] ITPL[3] ITPL[2] ITPL[1]	Input	AE23 AE10 V3 K4	**Incoming Tributary Payload Active.** The incoming tributary payload active bus (ITPL[4:1]) is set high to mark each tributary synchronous payload / low order virtual container byte in the corresponding incoming data bus (ID[4:1][7:0]). ITPL[*x*] is set low at STS/STM transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1, V2, V3 and V4). The ITPL[x] signal may be used in loopback modes, but will not affect the 8B/10B encoding operation of the TBS. ITPL[4:1] is sampled on the rising edge of SYSCLK.
ITAIS[4] ITAIS[3] ITAIS[2] ITAIS[1]	Input	AC21 AF9 U4 J3	**Incoming Tributary Path AIS.** The incoming tributary path AIS bus (ITAIS[4:1]) identifies virtual tributary / tributary unit streams on the corresponding incoming data bus (ID[4:1][7:0]) that are in low order path AIS state. ITAIS[*x*] is set high when the stream on ID[*x*][7:0] is in AIS and is set low when the stream is out of AIS state. The ITAIS[x] signal may be used in loopback modes, but will not affect the 8B/10B encoding operation of the TBS. ITAIS[4:1] is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Transmit Serial Data Interface (25 Signals)			
TPWRK[4] TNWRK[4] TPWRK[3] TNWRK[3] TPWRK[2] TNWRK[2] TPWRK[1] TNWRK[1]	Analog LVDS Output	K24 K23 K26 K25 J25 J24 H24 H23	**Transmit Working Serial Data.** The differential transmit working serial data links (TPWRK[4:1]/TNWRK[4:1]) carries the transmit SONET/SDH STS-48 frame data to a downstream working sink, in bit serial format. Each differential pair carries a constituent STS-12 of the transmit working stream. Data on TPWRK/TNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Unused transmit LVDS pins should be left unconnected.

Pin Name	Type	Pin No.	Function
TPPROT[4] TNPROT[4] TPPROT[3] TNPROT[3] TPPROT[2] TNPROT[2] TPPROT[1] TNPROT[1]	Analog LVDS Output	T25 T24 R26 R25 R24 R23 P26 P25	**Transmit Protection Serial Data.** The differential transmit protection serial data links (TPPROT[4:1]/TNPROT[4:1]) carries the transmit SONET/SDH STS-48 frame data to a downstream protection sink, in bit serial format. Each differential pair carries a constituent STS-12 of the transmit protection stream. Data on TPPROT/TNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Unused transmit LVDS pins should be left unconnected.
TPAUX[4] TNAUX[4] TPAUX[3] TNAUX[3] TPAUX[2] TNAUX[2] TPAUX[1] TNAUX[1]	Analog LVDS Output	AA26 AA25 AA24 AA23 Y25 Y24 W26 W25	**Transmit Auxiliary Serial Data.** The differential transmit auxiliary serial data links (TPAUX[4:1]/TNAUX[4:1]) carries the transmit SONET/SDH STS-48 frame data to a downstream auxiliary sink, in bit serial format. Each differential pair carries a constituent STS-12 of the transmit auxiliary stream. Data on TPAUX/TNAUX is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. Unused transmit LVDS pins should be left unconnected.
TJ0FP	Output	AC22	**Transmit Serial Interface Frame Pulse.** The transmit serial interface frame pulse signal (TJ0FP) provides system timing of the transmit serial interface. TJ0FP is set high once every 9720 SYSCLK cycles to indicate that the J0 frame boundary 8B/10B character has been serialized out on the transmit working serial data links (TPWRK[4:1]/TNWRK[4:1]), the transmit protection serial data links (TPWRK[4:1]/TNWRK[4:1]), and the transmit auxiliary serial data links (TPAUX[4:1]/TNAUX[4:1]). TJ0FP is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
Microprocessor Interface (33 Signals)			
CSB	Input	D17	**Chip Select Bar.** The active low chip select signal (CSB) controls microprocessor access to registers in the TBS device. CSB is set low during TBS Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses. If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.

Pin Name	Type	Pin No.	Function
RDB	Input	B18	**Read Enable Bar.** The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the TBS device. RDB is set low and CSB is also set low during TBS Microprocessor Interface Port register read accesses. The TBS drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	B19	**Write Enable Bar.** The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the TBS device. WRB is set low and CSB is also set low during TBS Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	A7 B8 C9 D10 B9 C10 A9 D11 B10 C11 B11 D12 A11 C12 B12 A12	**Microprocessor Data Bus.** The bi-directional data bus, D[15:0] is used during TBS Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.
A[11]/TRS A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B13 B14 A15 B15 C15 A16 D15 B16 A17 C16 B17 D16	**Microprocessor Address Bus.** The microprocessor address bus (A[11:0]) selects specific Microprocessor Interface Port registers during TBS register accesses. A[11] is also the Test Register Select (TRS) address pin and selects between normal and test mode register accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	C17	**Address Latch Enable.** The address latch enable signal (ALE) is active high and latches the address bus (A[11:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the TBS to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
INTB	Open Drain Output	A20	**Interrupt Request Bar**. The active low interrupt enable signal (INTB) output goes low when a TBS interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Pin Name	Type	Pin No.	Function
General Function (5 Signals)			
SYSCLK	Input	AD12	**System Clock.** The system clock signal (SYSCLK) is the master clock for the TBS device. SYSCLK must be a 77.76 MHz clock, with a nominal 50% duty cycle. ID[4:1][7:0], IDP[4:1], IPL[4:1], IJ0J1[4:1], IPAIS[4:1], ITV5[4:1], ITPL[4:1], ITAIS[4:1] and RJ0FP are sampled on the rising edge of SYSCLK. TJ0FP, OD[4:1][7:0], ODP[4:1], OPL[4:1], OJ0J1[4:1], OTV5[4:1], OTPL[4:1], and OCOUT[4:1] are updated on the rising edge of SYSCLK.
TCMP	Input	C23	**Transmit Connection Memory Page.** The transmit connection memory page select signal (TCMP) controls the selection of the connection memory page in the three Transmit Time-slot Interchange blocks (TWTI, TPTI and TATI). TCMP is exclusive-ORed with the CMPSEL bit in the TWTI/TPTI and TATI Configuration and Status Registers. For any of the three Transmit Timeslot Interchange blocks, if the corresponding CMPSEL bit is set low, then when TCMP is set high, connection memory page 1 is selected for that block. With the CMPSEL bit low, when TCMP is set low, connection memory page 0 is selected. When the CMPSEL bit is set high, setting TCMP high will select memory page 0 while setting TCMP low will select memory page 1. TCMP is sampled on the rising edge of SYSCLK when IJ0J1[1] is set high and IPL[1] is set low i.e. the frame boundary. Changes to the connection memory page selection are synchronized to the frame boundary of the frame following the next transport frame (i.e. two frame boundaries after the TCMP signal is sampled).

Pin Name	Type	Pin No.	Function
OCMP	Input	A24	**Outgoing Connection Memory Page.** The outgoing data bus connection memory page select signal (OCMP) controls the selection of the connection memory page in the three Outgoing Time-slot Interchange blocks (RWTI, RPTI and RATI). OCMP is exclusive-ORed with the CMPSEL bit in the RWTI, RPTI and RATI Configuration and Status Registers. For any of the three Receive Timeslot Interchange blocks, if the corresponding CMPSEL bit is set low, then when OCMP is set high, connection memory page 1 is selected for that block. With the CMPSEL bit low, when OCMP is set low, connection memory page 0 is selected. When the CMPSEL bit is set high, setting OCMP high will select memory page 0 while setting OCMP low will select memory page 1. OCMP is sampled on the rising edge of SYSCLK at the J0 byte location as defined by the receive serial interface frame pulse signal (RJ0FP). Changes to the connection memory page selection are synchronized to the transport frame boundary of the frame following the next frame (i.e. Two frame boundaries after the OCMP signal has been sampled).
RWSEL	Input	C22	**Receive Working Serial Data Select.** The receive working serial data select signal (RWSEL) selects between sourcing outgoing data (OD[4:1][7:0]) from the receive working serial data links (RPWRK[4:1]/RNWRK[4:1]) or the receive protection serial data links (RPPROT[4:1]/RNPROT[4:1]) when the RWSEL_EN register bit is logic 1 (register 001H). RWSEL is ignored when RWSEL_EN is logic 0, and instead the RxTSEN register bits are used to select between working, protect, and auxiliary serial links with STS-1 granularity. When RWSEL is set high, the working serial bus is selected after the RWTI. When RWSEL is set low, the protection serial bus is selected after the RPTI. In either case time slot interchange can be performed on the data before being sent on the outgoing TelecomBus. RWSEL is sampled on the rising edge of SYSCLK at the J0 byte location as defined by the receive serial interface frame pulse signal (RJ0FP). Changes to the selection of the working and protection serial streams are synchronized to the transport frame boundary of the frame following the next frame (i.e. two frame boundaries after RWSEL is sampled).
RSTB	Input	A23	**Reset.** The active low reset signal (RSTB) provides an asynchronous TBS reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.

Pin Name	Type	Pin No.	Function
JTAG Interface (5 Signals)			
TCK	Input	C21	**Test Clock.** The JTAG test clock signal (TCK) provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	D20	**Test Mode Select.** The JTAG test mode select signal (TMS) controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	D19	**Test Data Input.** The JTAG test data input signal (TDI) carries test data into the TBS via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tri-state	B20	**Test Data Output.** The JTAG test data output signal (TDO) carries test data out of the TBS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when scanning of data is in progress.
TRSTB	Input	B21	**Test Reset Bar.** The active low JTAG test reset signal (TRSTB) provides an asynchronous TBS test access port (TAP) controller reset via the IEEE P1149.1 TAP. TRSTB is a Schmitt triggered input with an integral pull-up resistor. The TAP controller must be placed in the Test-Logic-Reset state after applying power to the device to guarantee correct device operation. This is easily accomplished by connecting TRSTB to the RSTB input and performing a device reset, but is not necessary if another method of resetting the TAP controller is implemented.

Pin Name	Type	Pin No.	Function
Analog Test Bus (2 Signals)			
ATB0	Analog	AB23	**Analog test bus (ATB0).** ATB0 is used for PMC validation and testing. This pin must be grounded.
ATB1	Analog	AB25	**Analog test bus (ATB1).** ATB1 is used for PMC validation and testing. This pin must be grounded.

Pin Name	Type	Pin No.	Function
External Resistors (2 Signals)			
RES	Analog	E25	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8 V VREF voltage onto RES, therefore forcing 252µA of current to flow through the resistor.
RESK	Analog	E23	**Reference Resistor Connection.** An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8 V VREF voltage onto RES, therefore forcing 252µA of current to flow through the resistor.

Pin Name	Type	Pin No.	Function
Analog Low Voltage Power (6 Signals)			
AVDL[2:0]	Power	G23 L23 V23	The analog power pins (AVDL[2:0]) should be connected to a well-decoupled +1.8 V DC supply. Note that the CSU_AVDL is included in references to AVDL throughout this document unless otherwise noted.
CSU_AVDL[2:0]	Power	P23 N24 P24	The CSU low voltage analog power pins (CSU_AVDL[2:0]) should be connected to a well-decoupled +1.8 V DC supply. Note that the CSU_AVDL is included in references to AVDL throughout this document unless otherwise noted.

Pin Name	Type	Pin No.	Function
Analog High Voltage Power (8 Signals)			
CSU_AVDH	Power	N23	The CSU analog power pin. It should be connected to a well-decoupled +3.3 V DC supply. Note that the CSU_AVDH is included in references to AVDH throughout this document unless otherwise noted.
AVDH[6:0]	Power	AB24 AC24 D24 E24 J23 T23 Y23	The analog power pins (AVDH[6:0]) should be connected to a well-decoupled +3.3 V DC supply. Note that the CSU_AVDH is included in references to AVDH throughout this document unless otherwise noted.

Pin Name	Type	Pin No.	Function
Digital Core Power (20 Signals)			
VDDI[19:0]	Power	A18 A21 A8 AC2 AD20 AD22 AD7 AE12 AE18 AE5 AE8 B6 C13 D1 D21 H3 J2 P4 U1 Y1	The digital core power pins (VDDI[19:0]) should be connected to a well-decoupled +1.8 V DC supply.

Pin Name	Type	Pin No.	Function
Digital I/O Power (21 Signals)			
VDDO[20:0]	Power	AC14 AC19 AC23 AC4 AC9 AD24 AD3 AE2 AE25 B2 B25 C24 C3 D13 D18 D23 D4 D8 H4 N4 V4	The digital I/O power pins (VDDO[20:0]) should be connected to a well-decoupled +3.3 V DC supply.

Pin Name	Type	Pin No.	Function
Ground (40 Signals)			
VSS[39:0]	Power	A1 A13 A14 A2 A25 A26 AB26 AC25 AC26 AD2 AD25 AD26 AE1 AE24 AE26 AE3 AF1 AF13 AF14 AF2 AF25 AF26 B1 B24 B26 B3 C2 C25 C26 D25 D26 E26 G26 J26 L26 N1 P1 T26 V26 Y26	The ground pins (VSS[39:0]) should be connected to GND.

Pin Name	Type	Pin No.	Function
No Connect (36 Signals)			
NC[35:0]	No Connect	A10 A19 A22 AA1 AA3 AB3 AC11 AC13 AC16 AC17 AC18 AC3 AC6 AC7 AE14 AE16 AE19 AE7 AF10 AF11 AF3 AF8 B22 B23 C14 C18 C19 C20 C4 C5 D14 D22 D5 D9 J4 T4	The No Connect pins (NC[35:0]) are internally unconnected and can be left floating.
Total (352 Signals)			

Notes on Pin Description:

1. Schmitt trigger inputs (RSTB, TRSTB and SYSCLK) do not tolerate TTL levels.
2. All other TBS inputs and bi-directionals except the LVDS links present minimum capacitive loading, operate at TTL logic levels and can tolerate 3.3V input levels.
3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
4. All TBS outputs have 12 mA drive capability, except the INTB open drain output, the TDO output which have 6 mA drive capability, and the D[15:0] bi-directional outputs which have 8 mA drive capacity.
5. The VDDI and AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the TBS. Similarly, the VDDO and AVDH power pins must be connected externally to avoid device malfunction or damage.
6. The VDDI, VDDO, AVDH, and AVDL power pins all share a common ground.

7. See section 17.2 for information on Power Sequencing

11 Functional Description

11.1 Incoming TelecomBus PRBS Processor

The Incoming TelecomBus PRBS Processor block (ITPP) provides in-service and off-line diagnostics of the incoming TelecomBus stream and equipment downstream of the three sets of transmit LVDS links. A total of four ITPP blocks are instantiated in the TBS device. Each ITPP has the capacity to monitor and source PRBS data of an STS-12/STM-4 stream. A set of four ITPP blocks may be configured to service an STS-48c/STM-16-16c stream.

11.1.1 PRBS Detector

Each ITPP block has an independent PRBS detector and generator. The PRBS detector sub-block in ITPP #1 to ITPP #4 monitors the four sections of the incoming data stream ID[1][7:0] to ID[4][7:0], respectively. When enabled, the PRBS detector sub-block monitors synchronous payload envelope (SPE) / higher order virtual container (VC3 or VC4-Xc) bytes in the incoming data stream. The incoming data is compared against the expected value derived from an internal linear feedback shift register (LFSR) with a polynomial of $X^{23} + X^{18} + 1$. If the incoming data fails to match the expected value for three consecutive bytes, the PRBS detector sub-block will enter out-of-synchronization (OOS) state. The LFSR will be re-initialized using the incoming data bytes. The new LFSR seed is confirmed by comparison with subsequent incoming data bytes. The PRBS detector sub-block will exit the OOS state when the incoming data matches the LFSR output for three consecutive bytes. The PRBS detector sub-block will remain in the OOS state and re-load the LFSR if confirmation failed. The PRBS sub-block counts PRBS byte errors and optionally generates interrupts when it enters and exits the OOS state.

The PRBS detector sub-block may be configured to also monitor the B1 and E1 bytes in the incoming data stream. The B1 byte in each incoming STS-1/STM-0 is compared with an independently software programmable value. The E1 byte is compared with the complement of the programmable value. An interrupt is optionally generated when there is a mismatch in the comparison of the B1 or E1 bytes on a per-STS1 basis. When enabled to do so, the incoming B1 bytes are captured in a set of software readable registers. This facility allows in-service diagnosis of provisioning errors in upstream cross-connect devices.

11.1.2 PRBS Generator

The PRBS generator sub-block in ITPP #1 to ITPP #4 may optionally overwrite the data in incoming data stream ID[1][7:0] to ID[4][7:0], respectively. When enabled, the PRBS generator sub-block inserts synchronous payload envelope (SPE) / higher order virtual container (VC3 or VC4-Xc) bytes into the serial transmit links. The inserted data is derived from an internal linear feedback shift register (LFSR) with a polynomial of $X^{23} + X^{18} + 1$. The PRBS generator must be configured for the same payload concatenation level as the incoming stream which is to have PRBS inserted (STS-1, STS-3c, STS-12c or STS-48c). Note that PRBS insertion into the SPE has no effect on TelecomBus control signals, which will take priority over the data stream. For this reason it is important to ensure that none of the control signals, such as IPAIS[4:1], are continuously asserted when attempting PRBS insertion.

The user may insert PRBS into the data passing through the ID8E, IP8E, or both. Each TTSI is independently configurable to select the data from the ID8E or IP8E on a per-STS-1 basis via the IP8ESEL register bits.

The PRBS generator sub-block may be configured to optionally insert a software programmable byte into the B1 byte of each STS-1/STM-0 stream the serial transmit links. The E1 bytes may be over-written to the complement of the value inserted into the B1 bytes. This facility allows in-service diagnosis of provisioning errors in downstream cross-connect devices.

11.2 Incoming Data 8B/10B Encoder

The Incoming Data 8B/10B Encoder block (ID8E) constructs an 8B/10B character stream from an incoming TelecomBus carrying an STS-12/STM-4 stream. A total of four ID8E blocks are instantiated in the TBS device. ID8E #1 to ID8E #4 processes incoming data streams ID[1][7:0] to ID[4][7:0], respectively.

11.2.1 Frame Counter

The Frame Counter sub-block keeps track of the octet identity of the incoming data stream. It is initialized by the J0 pulse on the IJ0J1[1] and IPL[1] signals. It identifies the positive stuff opportunity (PSO) and negative stuff opportunity (H3) bytes within the transport frame so that high-order path pointer justification events can be identified and encoded.

11.2.2 8B/10B Encoder

The 8B/10B encoder sub-block converts bytes in the incoming STS-12/STM-4 stream to 8B/10B characters. It can operate in multiplex section termination (MST) or high-order path termination (HPT) modes. The modes relate to the level of SONET/SDH processing capability in the external device driving the incoming TelecomBus (ID[4:1][7:0]).

In MST mode, the upstream device is a multiplex section terminator. It has identified transport frame boundaries. The first J0 byte (J0) is encoded by an 8B/10B control character. Incoming TelecomBus signals ITV5[4:1], ITPL[4:1], and ITAIS[4:1] and the J1 portion of IJ0J1[4:1] are ignored.

In HPT mode, the upstream device is a high-order path terminator and has performed pointer processing to identify STS/AU level pointer justification events. It has processed all the STS/VC3/VC4 path overhead bytes. The H3 bytes in the absence of negative pointer justification events, the PSO byte in the presence of positive pointer justification events may be encoded. Additionally, the J1 byte may be encoded. Note that the encoding of J1 bytes (and all control characters in general), causes a loss of the specific data carried in the byte. In the case of the J1 byte, encoding in HPT mode will decode to a data value ‘h00 making path trace or other user-defined functions unusable across the serial links. Incoming TelecomBus signals ITV5[4:1], ITPL[4:1], and ITAIS[4:1] are ignored.

Note that in drop-and-continue operation, the TBS must be configured to regard the upstream device as one appropriate for the continued path.

Table 1 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into two sections, one for each software configurable mode of operation. When the TelecomBus control signals conflict each other, the 8B/10B control characters are generated according to the sequence of the table, with the characters at the top of the table taking precedence over those lower in the table.

Table 1 Serial TelecomBus 8B/10B Character Mapping

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 1010	110000 0101	IJ0 = ’b1 IPL = ‘b0 Transport frame alignment
K.28.4-	001111 0010	-	IPAIS = ’b1 High-order path AIS
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL = ‘b0 High-order path H3 byte position, no negative justification event
K28.0+	-	110000 1011	IPL = ‘b0 High-order path PSO byte position, positive justification event
K28.6	001111 0110	110000 1001	IJ1 = ’b1 IPL = ‘b1 High-order path frame alignment

11.3 Incoming PRBS 8B/10B Encoder

The Incoming PRBS 8B/10B Encoder block (IP8E) constructs an 8B/10B character stream from the output of the Incoming TelecomBus PRBS Processor. A total of four IP8E blocks are instantiated in the TBS device. IP8E #1 to IP8E #4 process data from ITPP #1 to ITPP #4, respectively. The IP8E is functionally identical to the ID8E block.

11.4 Transmit Time-slot Interchange

The Transmit Time-slot Interchange (TTSI) block re-arranges the constituent STS-1/STM-0 streams of an STS-48/STM-16 stream in a software configurable order. The TTSI blocks also support multicast where an incoming STS-1/STM-0 stream is placed on two or more outgoing time-slots. A total of three TTSI blocks are instantiated in the TBS device. The Transmit Working Time-slot Interchange block (TWTI) performs time-slot re-arrangement for data destined for the working transmit LVDS links (TPWRK[4:1]/TNWRK[4:1]). The Transmit Protection Time-slot Interchange block (TPTI) services the protection transmit LVDS links (TPPROT[4:1]/TNPROT[4:1]) while the Transmit Auxiliary Time-slot Interchange block (TATI) services the auxiliary transmit LVDS links (TPAUX[4:1]/TNAUX[4:1]).

11.4.1 Data Buffer

The Data Buffer block contains a double buffer structure. The incoming data stream is first loaded into an input shift register. The Frame Counter sub-block initiates a transfer of the data to the holding register once all 48 constituent STS-1/STM-0 streams have been shifted in. The data is read out of the holding register in the order specified by the Connection Memory sub-block.

11.4.2 Connection Memory

The Connection Memory sub-block contains two mapping pages: page 0 and page 1. One page is designated the active page and the other the standby page. Selection between which page is to be active and which is to be standby is controlled by the TCMP signal. The TCMP signal is exclusive-ORed with the CMPSEL bit of the TTSI block. The Connection Memory sub-block samples the value on the TCMP signal at the J0 byte position of the incoming data stream and swaps the active/standby status of the two pages at the first A1 byte of the frame after the next frame i.e. on the second frame boundary after the TCMP signal is sampled. If the CMPSEL bit is used to trigger a page swap, the swap takes place at the start of the next frame. This arrangement allows all devices in a cross-connect system to be updated in a coordinated fashion. Consequently, STS-1/STM-0 streams not being assigned new time-slots are unaffected by page swaps.

11.5 Transmit 8B/10B Running Disparity Encoder

The Transmit 8B/10B Running Disparity Encoder (TRDE) block corrects the running disparity of an 8B/10B character stream. The input data to the TRDE blocks originated from either the ID8E or the IP8E blocks at which point they have correct running disparity. However, due to the time-slot re-arrangement activities of the Transmit Time-slot Interchange blocks, the running disparity is no longer consistent. The TRDE block inverts the 6B and 4B sub-characters to ensure correct running disparity.

A total of twelve TRDE blocks are instantiated in the TBS device. Four TRDE blocks, Transmit Working Disparity Encoder (TWDE #1 to #4) are dedicated to the working transmit LVDS links (TPWRK[4:1]/TNWRK[4:1]). The Transmit Protection Disparity Encoder (TPDE #1 to #4) correct running disparity for characters destined for the protection transmit LVDS links (TPPROT[4:1]/TNPROT[4:1]) while the Transmit Auxiliary Disparity Encoder blocks (TADE #1 to #4) service the auxiliary transmit LVDS links (TPAUX[4:1]/TNAUX[4:1]).

11.6 Transmit Serializer

The Transmit Serializer (PISO) block converts 8B/10B characters to bit-serial format. A total of twelve PISO blocks are instantiated in the TBS device. Four PISO blocks, Transmit Working Serializer (TWPS #1 to #4) are dedicated to the working transmit LVDS links (TPWRK[4:1]/TNWRK[4:1]). The Transmit Protection Serializer (TPPS #1 to #4) generate serial streams for the protection transmit LVDS links (TPPROT[4:1]/TNPROT[4:1]) while the Transmit Auxiliary Serializer blocks (TAPS #1 to #4) are associated with the auxiliary transmit LVDS links (TPAUX[4:1]/TNAUX[4:1]).

11.7 LVDS Transmitter

The LVDS Transmitter (TXLV) blocks convert 8B/10B encoded digital bit-serial streams to LVDS signaling levels. A total of twelve TXLV blocks are instantiated in the TBS device. Four TXLV blocks, Transmit Working LVDS Interface (TWLV #1 to #4) drive the working transmit LVDS links (TPWRK[4:1]/TNWRK[4:1]). The Transmit Protection LVDS Interface blocks (TPLV #1 to #4) drive the protection transmit LVDS links (TPPROT[4:1]/TNPROT[4:1]) while the Transmit Auxiliary LVDS Interface blocks (TALV #1 to #4) are associated with the auxiliary transmit LVDS links (TPAUX[4:1]/TNAUX[4:1]).

11.8 CSTR

The Clock Synthesis Unit and Transmit Voltage Reference Generator (CSTR) block generates the 777.6 MHz clock for the transmit and receive LVDS links as well as the bias voltages and currents for the LVDS Transmitters.

11.9 DLL

The Digital Delay Locked Loop adjusts the internal version of SYSCLK to compensate for buffer, pad, and wiring delays in the clock tree. This allows for improved margin for setup and hold times on the SYSCLK synchronous digital I/O of the TBS. The DLL accepts the SYSCLK given to the device, as well as a feedback signal internal to the device called REFCLK. REFCLK is simply the clock applied to all the flip-flops in the device (IE a tap from the bottom of the clock tree). The DLL internally delays SYSCLK such that the time from a rising edge on SYSCLK to that rising edge arriving at an internal flip-flop is exactly one period of SYSCLK. Since SYSCLK is periodic this makes it appear that the rising edge of the clock arriving at the device and the rising edge of the clock arriving at the flip-flops in the TBS are coincident.

Under most conditions the operation of the DLL is transparent to the user. The only time this is not true is during start-up and during error conditions which can be diagnosed via the DLL registers.

11.10 LVDS Receiver

The LVDS Receiver (RXLV) block converts LVDS signaling levels to 8B/10B encoded digital bit-serial data. A total of twelve RXLV blocks are instantiated in the TBS device. Four RXLV blocks, Receive Working LVDS Interface (RWLV #1 to #4) connect to the working receive LVDS links (RPWRK[4:1]/RNWRK[4:1]). The Receive Protection LVDS Interface blocks (RPLV #1 to #4) connect to the protection receive LVDS links (RPPROT[4:1]/RNPROT[4:1]) while the Receive Auxiliary LVDS Interface blocks (RALV #1 to #4) are associated with the auxiliary receive LVDS links (RPAUX[4:1]/RNAUX[4:1]).

11.11 Data Recovery Unit

The Data Recovery Unit (DRU) block monitors the receive LVDS link for transitions to determine the extent of bit cycles on the link. It then adjusts its internal timing to sample the link in the middle of the data "eye". A total of twelve DRU blocks are instantiated in the TBS device. Four DRU blocks, Working Data Recovery Units (WDRU #1 to #4) retrieve data from the working receive LVDS links (RPWRK[4:1]/RNWRK[4:1]). The Protection Data Recovery Unit (PDRU #1 to #4) processes the protection receive LVDS links (RPPROT[4:1]/RNPROT[4:1]) while the Auxiliary Data Recovery Units (RALV #1 to #4) are associated with the auxiliary receive LVDS links (RPAUX[4:1]/RNAUX[4:1]).

The DRU block also converts the serial data stream into 10-bit words. The words are constructed from ten consecutive received bits without regard to 8B/10B character boundaries.

11.12 Receive 8B/10B TelecomBus Decoder

The Receive 8B/10B TelecomBus Decoder (R8TD) block frames to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. A total of twelve R8TD blocks are instantiated in the TBS device. Four R8TD blocks, Receiver Working 8B/10B Decoder blocks (RW8D #1 to #4) perform framing and elastic store functions on data retrieved from the working receive LVDS links (RPWRK[4:1]/RNWRK[4:1]). The Receive 8B/10B Decoder blocks (RP8D #1 to #4) process data on the protection receive LVDS links (RPPROT[4:1]/RNPROT[4:1]) while the Receive Auxiliary 8B/10B Decoder blocks (RA8D #1 to #4) are associated with the auxiliary receive LVDS links (RPAUX[4:1]/RNAUX[4:1]).

11.12.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated receive LVDS link and that of the system clock (SYSCLK). Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

11.12.2 Frame Counter

The Frame Counter sub-block keeps track of the octet identity of the outgoing data stream. It is initialized by a delayed version of the RJ0FP signal. The frame counter identifies the positive stuff opportunity (PSO) and negative stuff opportunity (H3) bytes within the transport frame so that high-order path pointer justification events can be identified and decoded.

11.12.3 Character Alignment

The character alignment sub-block locates character boundaries in the incoming 8B/10B data stream. The framer logic may be in one of two states, SYNC state or HUNT state. It uses the 8B/10B control character (K28.5) used to encode the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. The sub-block monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in IEEE 802.3. Excessive LCVs force the framer logic to the HUNT state.

Normal operation progresses when the character alignment sub-block is in the SYNC state. 8B/10B characters are extracted from the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If 5 or more LCVs are detected in a window of 15 characters, the character alignment sub-block enters the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. The original character alignment is maintained until the next K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block reverts to the SYNC state.

11.12.4 Frame Alignment

The frame alignment sub-block monitors the data read from the FIFO buffer sub-block for the J0 character (K28.5). When the frame counter sub-block indicates the J0 byte position, the block expects a J0 character to be read from the FIFO. If a J0 character is read out of the FIFO at other byte positions, a J0 byte error counter is incremented. When the counter reaches a count of 3, the frame alignment sub-block enters the HUNT state. The next time a J0 character is read from the FIFO, the associated read address is latched and the sub-block moves back to the SYNC state if the character alignment state machine has been in the SYNC state since the previous J0. The J0 byte error counter is cleared when a J0 byte is read from the FIFO at the expected position.

11.12.5 Character Decode

The character decode sub-block decodes the incoming 8B/10B control characters into an extended set of TelecomBus control signals. Table 2 shows the mapping of 8B/10B control characters into TelecomBus control signals. The table is divided into three sections, one for each mode of operation of the 8B/10B encoder in an external device upstream of the TBS. The character decoder sub-block itself is not mode sensitive. Note that decoded characters are passed to the Receive PRBS Monitor blocks and terminate there. Non decoded characters continue to the Receive Time-Slot Interchange blocks.

Table 2 Serial TelecomBus 8B/10B character decoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
K28.5	001111 1010	110000 0101	OJ0 = ‘b1 (‘b0 if not aligned with system frame pulse) OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘h00 Transport frame alignment
K28.0-	001111 0100	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘h00 High-order path H3 byte, no negative justification event
K28.0+	-	110000 1011	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘h00 High-order path PSO byte, positive justification event
K.28.4-	001111 0010	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b1 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘hFF High-order path AIS
K28.6	001111 0110	110000 1001	OJ0 = ‘b0 OJ1 = ‘b1 (‘b0 if OPL = ‘b0) OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘h00 High-order path frame alignment
K27.7-	110110 1000	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘h00 Low order path frame alignment

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
K27.7+	-	001001 0111	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00100000 Low order path frame alignment
K28.7-	001111 1000	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00010000 Low order path frame alignment
K28.7+	-	110000 0111	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00110000 Low order path frame alignment
K29.7-	101110 1000	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00000001 Low order path frame alignment
K29.7+	-	010001 0111	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00100001 Low order path frame alignment
K30.7-	011110 1000	-	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00010001 Low order path frame alignment

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
K30.7+	-	100001 0111	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b1 OD = ‘b00110001 Low order path frame alignment
K23.7	111010 1000	000101 0111	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b0 OTV5 = ‘b0 OD = ‘h00 Non low-order path payload overhead bytes (RSOH, MSOH, POH, R, V1, V2, V3, V4)
K.28.4+	-	110000 1101	OJ0 = ‘b0 OJ1 = ‘b0 OPAIS = ‘b0 OTAIS = ‘b1 OTV5 = ‘b0 OD = ‘hFF Low-order path AIS

11.13 Receive PRBS Monitor

NOTE:

1. In order for the TBS to be able to monitor a PRBS data stream from another TBS or S/UNI-MACH48 CHESS device, the data must be transmitted in HPT mode. The TBS transmit channels can be configured for HPT mode by using the TMODE bits in the IP8E or ID8E blocks (Registers 0x112, 0x113, 0x122, 0x123, etc.). If the PRBS stream traverses multiple devices, every transmitter along the path must be set to encode the PRBS stream in HPT mode.
2. The Receive PRBS Monitor block (RPRM) provides in-service and off-line diagnostics of the receive LVDS links. A total of twelve blocks are instantiated in the TBS device. Four RPRM blocks, Receive Working PRBS Monitor (RWPM #1 to #4) connect to the working receive LVDS links (RPWRK[4:1]/RNWRK[4:1]). The Receive Protection PRBS Monitor blocks (RPPM #1 to #4) connect to the protection receive LVDS links (RPPROT[4:1]/RNPROT[4:1]) while the Receive Auxiliary PRBS Monitor blocks (RAPM #1 to #4) are associated with the auxiliary receive LVDS links (RPAUX[4:1]/RNAUX[4:1]). The RPRM block is functionally identical to the monitor section of the ITPP block. Note that PRBS Monitor blocks always have an associated generator block. In the case of the RPRM blocks, the associated generators are not used with one exception. The generator blocks associated with the RPPM #1 to #4 blocks are used for the OTPG blocks described below in section 11.15.

11.14 Receive Time-slot Interchange

The Receive Time-slot Interchange (RTSI) block re-arranges the constituent STS-1/STM-0 streams of an STS-48/STM-16 stream in a software configurable order. The RTSI block also support multicast where an STS-1/STM-0 stream from one of the three receive LVDS links is placed on two or more outgoing time-slots. A total of three RTSI blocks are instantiated in the TBS device. The Receive Working Time-slot Interchange block (RWTI) performs time-slot re-arrangement for data sourced from the working receive LVDS links (RPWRK[4:1]/RNWRK[4:1]). The Received Protection Time-slot Interchange block (RPTI) services the protection receive LVDS links (RPPROT[4:1]/RNPROT[4:1]) while the Receive Auxiliary Time-slot Interchange block (RATI) services the auxiliary receive LVDS links (RPAUX[4:1]/RNAUX[4:1]).

11.15 Outgoing TelecomBus 8B/10B Decoder

The Outgoing TelecomBus 8B/10B Decoder (OT8D) decodes 10 bit 8B/10B data characters into TelecomBus signals using the same character decoding as the R8TD blocks. There are four OT8D blocks (OT8D #1 to #4). These blocks are functionally similar to the RW8D blocks but operate in a continuous “in character alignment” state.

11.16 Outgoing TelecomBus PRBS Generator

The Outgoing TelecomBus PRBS Generator block (OTPG) optionally inserts PRBS pattern on a per STS-1/STM-0 onto the Outgoing TelecomBus stream. A total of four OTPG blocks are instantiated in the TBS device. Each OTPG has the capacity to source PRBS data of an STS-12/STM-4 stream. A set of four OTPG blocks may be configured to service an STS-48c/STM-16-16c stream. The OTPG block is functionally identical to the generator section of the ITPP block. Note that PRBS Generator blocks always have an associated monitor block. In the case of the OTPG blocks, the associated generators are the RPPM blocks described in section 11.12. Since these blocks share their processor interface, there are some subtle issues at the register level. These are described in the relevant register sections.

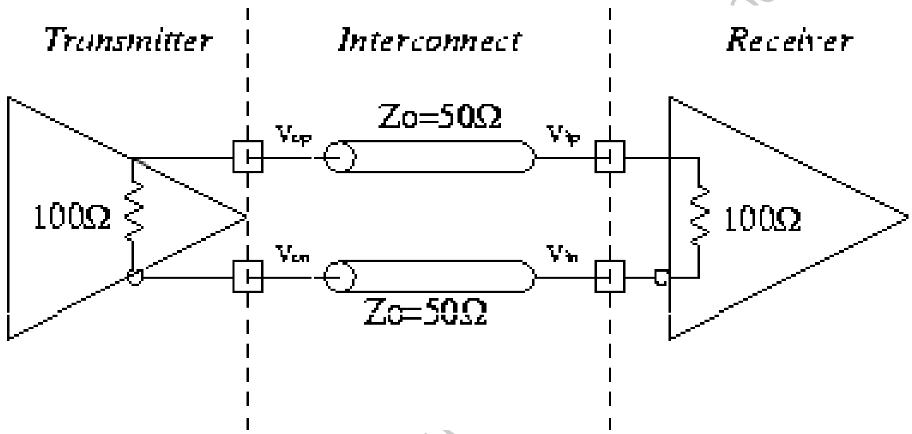
Note that PRBS insertion into the SPE has no effect on TelecomBus control signals, which will usually take priority over the data stream. For this reason it is important to ensure that none of the control signals, such as OPAIS[4:1], are continuously asserted when attempting PRBS insertion. If OPAIS[4:1] is inserted, the PRBS sequence may not be properly received by other devices.

11.17 LVDS Overview

The LVDS family of cells allows the implementation of 777.6 MHz LVDS links. A reference clock of 77.76MHz is required. Four 777.6 MHz LVDS form a set of high-speed serial data links for passing an STS-48 aggregate data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated in Figure 8 below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 8 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz SYSCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from SYSCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). It is expected that the clock source of the transmitter and the receiver are the same to ensure that the data throughput at both ends of the link are identical.

Data must contain sufficient transition density to allow reliable operation of the data recovery units.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors and up to 1m of backplane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately 350mV.

The LVDS system is comprised of the LVDS Receiver (RXLV), LVDS Transmitter (TXLV), Clock Synthesis Unit and Transmitter Reference (CSTR), data recovery unit (DRU) and parallel to serial converter (PISO).

11.18 Microprocessor Interface

The Microprocessor Interface block provides normal and test mode registers, and logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation. Test mode registers are used to enhance testability of the TBS. The register set is accessed as follows:

Table 3 Register Memory Map

Address	Register	
000H	TBS Master Incoming Configuration and Control	
001H	TBS Master Outgoing Configuration and Control	
002H	TBS Master Input Signal Activity, Accumulation Trigger	
003H	TBS Master Reset	
004H	TBS Parity Error Interrupt Status	
005H	TBS Master Receive Synchronization Delay and Accumulation Transfer	
006H	FREE User Register	
007H	Reserved	
008H	TBS Master Interrupt Enable #1	
009H	TBS Master Interrupt Enable #2	
00AH	TBS Master Interrupt Enable #3	
00BH	TBS Master Interrupt Enable #4	
00CH	TBS Master TSI, CSTR, and DLL Interrupt Enable	
00DH	TBS Master Interrupt Status #1	
00EH	TBS Master Interrupt Status #2	
00FH	TBS Master Interrupt Status #3	
010H	TBS Master Interrupt Status #4	
011H	TBS Master TSI, CSTR, and DLL Interrupt Status	
012H	TBS Version/Part Number	
013H	TBS Part Number/Manufacturer ID	
014H – 01FH	Reserved	
020H	TWTI Registers	Indirect Address
021H		Indirect Data
022H		Configuration and Status
023H		Interrupt Status
024H – 02FH		Reserved
030H	TPTI Registers	Indirect Address
031H		Indirect Data
032H		Configuration and Status
033H		Interrupt Status
034H – 03FH		Reserved
040H	TATI Registers	Indirect Address
041H		Indirect Data
042H		Configuration and Status
043H		Interrupt Status
044H – 04FH		Reserved
050H	DLL Registers	Configuration
051H		Reserved

Address	Register	
052H		DLL Reset
053H		Control Status
054H – 05FH		Reserved
060H – 07FH	Reserved	
080H	RWTI Registers	Indirect Address
081H		Indirect Data
082H		Configuration and Status
083H		Interrupt Status
084H – 08FH		Reserved
090H	RPTI Registers	Indirect Address
091H		Indirect Data
092H		Configuration and Status
093H		Interrupt Status
094H – 09FH		Reserved
0A0H	RATI Registers	Indirect Address
0A1H		Indirect Data
0A2H		Configuration and Status
0A3H		Interrupt Status
0A4H – 0AFH		Reserved
0B0 – 0BF	Outgoing TelecomBus I/F #1 Reserved	
0C0 – 0CF	Outgoing TelecomBus I/F #2 Reserved	
0D0 – 0DF	Outgoing TelecomBus I/F #3 Reserved	
0E0 – 0EF	Outgoing TelecomBus I/F #4 Reserved	
0F0H – 0FFH	Reserved	
100H	ITPP #1 Registers	Indirect Address
101H		Indirect Data
102H		Generator Payload Configuration
103H		Monitor Payload Configuration
104H		Monitor Byte Error Interrupt Status
105H		Monitor Byte Error Interrupt Enable
106H		Monitor B1/E1 Mismatch Interrupt Status
107H		Monitor B1/E1 Mismatch Interrupt Enable
108H		Reserved
109H		Monitor Synchronization Interrupt Status
10AH		Monitor Synchronization Interrupt Enable
10BH		Monitor Synchronization State
10CH		Performance Counters Transfer Trigger
10DH – 10FH		Reserved
110H	ID8E #1 Registers	Reserved
111H		Reserved

Address	Register	
112H		Time-slot Configuration #1
113H		Time-slot Configuration #2
114H – 11FH		Reserved
120H	IP8E #1 Registers	Reserved
121H		Reserved
122H		Time-slot Configuration #1
123H		Time-slot Configuration #2
124H – 12FH		Reserved
130H	TWDE #1 Registers	Control and Status
131H		Interrupt Status
132H		Reserved
133H		Reserved
134H		Test Pattern
135H		TWDE Analog Control
136H – 13FH		Reserved
140H	TPDE #1 Registers	Control and Status
141H		Interrupt Status
142H		Reserved
143H		Reserved
144H		Test Pattern
145H		TPDE Analog Control
146H – 14FH		Reserved
150H	TADE #1 Registers	Control and Status
151H		Interrupt Status
152H		Reserved
153H		Reserved
154H		Test Pattern
155H		TADE Analog Control
156H – 15FH		Reserved
160H	RW8D #1 Registers	Control and Status
161H		Interrupt Status
162H		Line Code Violation Count
163H		RW8D Analog Control
164H – 16FH		Reserved
170H	RP8D #1 Registers	Control and Status
171H		Interrupt Status
172H		Line Code Violation Count
173H		RP8D Analog Control
174H – 17FH		Reserved
180H	RA8D #1	Control and Status

Address	Register	
181H	Registers	Interrupt Status
182H		Line Code Violation Count
183H		RA8D Analog Control
184H – 18FH		Reserved
190H	RWPM #1 Registers	Indirect Address
191H		Indirect Data
192H		Reserved
193H		Monitor Payload Configuration
194H		Monitor Byte Error Interrupt Status
195H		Monitor Byte Error Interrupt Enable
196H		Monitor B1/E1 Mismatch Interrupt Status
197H		Monitor B1/E1 Mismatch Interrupt Enable
198H		Reserved
199H		Monitor Synchronization Interrupt Status
19AH		Monitor Synchronization Interrupt Enable
19BH		Monitor Synchronization State
19CH		Performance Counters Transfer Trigger
19DH – 19FH		Reserved
1A0H – 1AFH	RPPM #1 Registers	Same register map as RWPM #1
1B0H – 1BFH	RAPM #1 Registers	Same register map as RWPM #1
1C0H	OTPG #1 Registers	Indirect Address
1C1H		Indirect Data
1C2H – 1CFH		Reserved
1D0H– 1DFH	OT8D #1 Registers	Reserved
1E0H – 1EFH	Reserved	
200H – 20FH	ITPP #2 Registers	
210H – 21FH	ID8E #2 Registers	
220H – 22FH	IP8E #2 Registers	
230H – 23FH	TWDE #2 Registers	
240H – 24FH	TPDE #2 Registers	
250H – 25FH	TADE #2 Registers	
260H – 26FH	RW8D #2 Registers	
270H – 27FH	RP8D #2 Registers	
280H – 28FH	RA8D #2 Registers	
290H – 29FH	RWPM #2 Registers	
2A0H – 2AFH	RPPM #2 Registers	
2B0H – 2BFH	RAPM #2 Registers	
2C0H – 2CFH	OTPG #2 Registers	

Address	Register	
2D0H – 2DFH	OT8D #2 Registers	
2E0H – 2FFH	Reserved	
300H – 30FH	ITPP #3 Registers	
310H – 31FH	ID8E #3 Registers	
320H – 32FH	IP8E #3 Registers	
330H – 33FH	TWDE #3 Registers	
340H – 34FH	TPDE #3 Registers	
350H – 35FH	TADE #3 Registers	
360H – 36FH	RW8D #3 Registers	
370H – 37FH	RP8D #3 Registers	
380H – 38FH	RA8D #3 Registers	
390H – 39FH	RWPM #3 Registers	
3A0H – 3AFH	RPPM #3 Registers	
3B0H – 3BFH	RAPM #3 Registers	
3C0H – 3CFH	OTPG #3 Register	
3D0H – 3DFH	OT8D #3 Registers	
3E0H – 3FFH	Reserved	
400H – 40FH	ITPP #4 Registers	
410H – 41FH	ID8E #4 Registers	
420H – 42FH	IP8E #4 Registers	
430H – 43FH	TWDE #4 Registers	
440H – 44FH	TPDE #4 Registers	
450H – 45FH	TADE #4 Registers	
460H – 46FH	RW8D #4 Registers	
470H – 47FH	RP8D #4 Registers	
480H – 48FH	RA8D #4 Registers	
490H – 49FH	RWPM #4 Registers	
4A0H – 4AFH	RPPM #4 Registers	
4B0H – 4BFH	RAPM #4 Registers	
4C0H – 4CFH	OTPG #4 Register	
4D0H – 4DFH	OT8D #4 Registers	
4D0H – 4FFH	Reserved	
500H	CSTR	Control
501H		Interrupt Enable and Status
502H		Interrupt Indication
503H		Reserved
504H – 50FH	Reserved	
510H – FFFH	Reserved	

For all register accesses, CSB must be set low.

12 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the TBS. Normal mode registers (as opposed to test mode registers) are selected when A[11] is set low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TBS to determine the programming state of each block.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect TBS operation unless otherwise noted.

Register 000H TBS Master Incoming Configuration and Control

Bit	Type	Function	Default
Bit 15	R/W	O2ITCBLBEN	0
Bit 14	R/W	R2TWLBEN	0
Bit 13	R/W	R2TPLBEN	0
Bit 12	R/W	R2TALBEN	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IPE[4]	0
Bit 8	R/W	IPE[3]	0
Bit 7	R/W	IPE[2]	0
Bit 6	R/W	IPE[1]	0
Bit 5	R/W	TTSI_MODE[1]	0
Bit 4	R/W	TTSI_MODE[0]	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	INCIPL	0
Bit 1	R/W	INCIJ0J1	0
Bit 0	R/W	IOP	0

This register configures the TBS functionality that is related to dataflow from the Incoming TelecomBus stream to the Transmit Serial Data links.

IOP

The incoming odd parity bit (IOP) controls the expected parity on the Incoming TelecomBus stream. When IOP is set high, the parity of the parity signal set, together with IDP[*X*] is expected to be odd. When IOP is set low, the expected parity is even. Membership of the parity set always includes ID[*X*][7:0], and may include input signals IJ0J1[*X*] and IPL[*X*] as controlled by the INCIJ0J1 and INCIPL bits, respectively.

INCIJ0J1

The include incoming composite frame pulse bit (INCIJ0J1) controls whether the IJ0J1[*X*] input signal participates in the incoming parity calculations. When INCIJ0J1 is set high, the parity signal set includes the IJ0J1[*X*] input. Note that when IJ0J1 [1]=1 and IPL[1] = 0 (J0 byte indication), IJ0J1[2], IJ0J1[3], and IJ0J1[4] are overwritten with the IJ0J1[1] signal. The TBS requires that the J0 bytes are aligned across the incoming parallel TelecomBus for proper operation. If this convention is followed, the parity calculation for all four sections of the TelecomBus will be correct. Should the TelecomBus be operated in such a manner that the J0 bytes do not align across all 4 sections, then the INCIJ0J1 bit should be set to 0. When INCIJ0J1 is set low, parity is calculated without regard to the state of IJ0J1[*X*]. The IOP bit controls selection of odd or even parity.

INCIPL

The include incoming payload active bit (INCIPL) controls whether the IPL[*X*] input signal participates in the incoming parity calculations. When INCIPL is set high, the parity signal set includes the IPL[*X*] input. When INCIPL is set low, parity is calculated without regard to the state of IPL[*X*]. The IOP bit controls selection of odd or even parity.

TTSI_MODE[1:0]

The transmit serial TelecomBus TimeSlot Interchange Mode (TTSI_MODE[1:0]) bits are used to set the TWTI, TPTI, and TATI to either bypass or custom mapping mode.

Table 4 TWTI, TPTI, and TATI Mapping Modes

TTSI_MODE[1:0]	TWTI, TPTI, and TATI mode
00	User configured timeslot mapping
01	Bypass mode (no remapping)
10	Reserved
11	Reserved

IPE[4:1]

The incoming parity error interrupt enable bits (IPE[4:1]) controls the assertion of interrupts due to parity errors on the Incoming TelecomBus. When IPE[*X*] is set high, the occurrence of a parity error on the incoming parity signal (IDP[*X*]) will cause an interrupt to be asserted on INTB. When IPE[*X*] is set low, incoming parity errors will not cause an interrupt.

R2TALBEN

The receive to transmit auxiliary serial link loopback enable bit (R2TALBEN) controls line loopback of the auxiliary serial links. When R2TALBEN is set high, data on the receive auxiliary serial links (RPAUX[4:1]/RNAUX[4:1]) are character aligned and looped back to the corresponding transmit auxiliary serial links (TPAUX[4:1]/TNAUX[4:1]). When R2TALBEN is set low, the auxiliary transmit links carry data from the Incoming TelecomBus stream.

R2TPLBEN

The receive to transmit protection serial link loopback enable bit (R2TPLBEN) controls line loopback of the protection serial links. When R2TPLBEN is set high, data on the receive protection serial links (RPPROT[4:1]/RNPROT[4:1]) are character aligned and looped back to the corresponding transmit protection serial links (RPPROT[4:1]/RNPROT[4:1]). When R2TPLBEN is set low, the protection transmit links carry data from the Incoming TelecomBus stream.

R2TWLBEN

The receive to transmit working serial link loopback enable bit (R2TWLBEN) controls line loopback of the working serial links. When R2TWLBEN is set high, data on the receive working serial links (RPAUX[4:1]/RNAUX[4:1]) are character aligned and looped back to the corresponding transmit working serial links (TPAUX[4:1]/TNAUX[4:1]). When R2TWLBEN is set low, the working transmit links carry data from the Incoming TelecomBus stream.

O2ITCBLBEN

The outgoing to incoming TelecomBus stream loopback enable bit (O2ITCBLBEN) controls diagnostic loopback of the TelecomBus streams. When O2ITCBLBEN is set high, data on the Outgoing TelecomBus stream (OD[*X*][7:0]) is routed to the Incoming TelecomBus stream (ID[*X*][7:0]). When O2ITCBLBEN is set low, the Incoming TelecomBus stream is independent of the Outgoing TelecomBus stream.

Register 001H TBS Master Outgoing Configuration and Control

Bit	Type	Function	Default
Bit 15	R/W	I2OTCBLBEN	0
Bit 14	R/W	T2RLBEN	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RTSI_MODE[1]	0
Bit 4	R/W	RTSI_MODE[0]	1
Bit 3	R/W	RWSEL_EN	0
Bit 2	R/W	INCOPL	0
Bit 1	R/W	INCOJ0J1	0
Bit 0	R/W	OOP	0

This register configures the TBS functionality that is related to dataflow from the Receive Serial Data links to the Outgoing stream.

OOP

The outgoing odd parity bit (OOP) controls the expected parity on the Outgoing TelecomBus stream. When OOP is set high the parity of the parity signal set, together with ODP[*X*] is expected to be odd. When OOP is set low, the expected parity is even. Membership of the parity set always includes OD[*X*][7:0], and may include input signals OJ0J1[*X*] and OPL[*X*] as controlled by the INCOJ0J1 and INCOPL bits, respectively.

INCOJ0J1

The include outgoing composite frame pulse bit (INCOJ0J1) controls whether the OJ0J1[*X*] input signal participates in the outgoing parity calculations. When INCOJ0J1 is set high the parity signal set includes the OJ0J1[*X*] input. When INCOJ0J1 is set low, parity is calculated without regard to the state of OJ0J1[*X*]. The OOP bit controls selection of odd or even parity.

INCOPL

The include outgoing payload active bit (INCOPL) controls whether the OPL[*X*] input signal participates in the outgoing parity calculations. When INCOPL is set high, the parity signal set includes the OPL[*X*] input. When INCOPL is set low, parity is calculated without regard to the state of OPL[*X*]. The OOP bit controls selection of odd or even parity.

RWSEL_EN

The RWSEL_EN bit is used to enable the RWSEL input pin. When RWSEL_EN is logic 1, the RWSEL input signal is used to globally select between the working RPWRK/RNWRK[4:1] and protection RPPROT/RNPROT[4:1] serial TelecomBus links. When RWSEL_EN is logic 0, the RWSEL input is ignored and selection between the working, protection, and auxiliary serial TelecomBus links can be done on a per timeslot basis using the RWTSEN, RPTSEN, or RATSEN register bits in the indirect data registers in the RWTI, RPTI and RATI blocks respectively.

RTSI_MODE[1:0]

The receive TelecomBus TimeSlot Interchange Mode (RTSI_MODE[1:0]) bits are used to set the RWTI, RPTI, and RATI to either bypass or custom mapping mode.

Table 5 RWTI, RPTI, and RATI Mapping Modes

RTSI_MODE[1:0]	RWTI, RPTI, and RATI mode
00	User configured timeslot mapping
01	Bypass mode (no remapping)
10	Reserved
11	Reserved

T2RLBEN

The transmit to receive serial link loopback enable bit (T2RLBEN) controls diagnostic loopback of the working, protect, and auxiliary serial links. When T2RLBEN is set high, data on the transmit working, protect, and auxiliary serial links (TPWRK[4:1]/TNWRK[4:1], TPPROT[4:1]/TNPROT[4:1], TPAUX[4:1]/TNAUX[4:1]) are looped back to the corresponding receive working, protect, and auxiliary serial links (RPWRK[4:1]/RNWRK[4:1], RPPROT[4:1]/RNPROT[4:1], RPAUX[4:1]/RNAUX[4:1]). When T2RLBEN is set low data carried by the receive serial links are processed normally.

I2OTCBLBEN

The incoming to outgoing TelecomBus stream loopback enable bit (I2OTCBLBEN) controls line loopback of the TelecomBus streams. When I2OTCBLBEN is set high, data on the Incoming TelecomBus stream (ID[*X*][7:0]) is routed to the Outgoing TelecomBus stream (OD[*X*][7:0]). When I2OTCBLBEN is set low, the Outgoing TelecomBus stream is independent of the Incoming TelecomBus stream.

Register 002H TBS Master Input Signal Activity, Accumulation Trigger

Bit	Type	Function	Default
Bit 15	R	IDA[4]	0
Bit 14	R	IPCA[4]	0
Bit 13	R	ITCA[4]	0
Bit 12		Unused	X
Bit 11	R	IDA[3]	0
Bit 10	R	IPCA[3]	0
Bit 9	R	ITCA[3]	0
Bit 8		Unused	X
Bit 7	R	IDA[2]	0
Bit 6	R	IPCA[2]	0
Bit 5	R	ITCA[2]	0
Bit 4		Unused	X
Bit 3	R	IDA[1]	0
Bit 2	R	IPCA[1]	0
Bit 1	R	ITCA[1]	0
Bit 0	R	SYSCLKA	X

This register provides activity monitoring on major TBS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the various performance monitor accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 1.0 second or shorter. The bits in this register are not affected by write accesses.

SYSCLKA

The SYSCLK active bit (SYSCLKA) monitors for low to high transitions on the SYSCLK input. SYSCLKA is set high on a rising edge of SYSCLK, and is set low when this register is read.

ITCA[4:1]

The tributary control active bits (ITCA[4:1]) monitor for low to high transitions on the ITPL[4:1] and ITV5[4:1] inputs. ITCA[*X*] is set high when rising edges have been observed on both the ITPL[*X*] and ITV5[*X*] inputs since the last read, and is set low after this register is read.

IPCA[4:1]

The high-order path control active bits (IPCA[4:1]) monitor for low to high transitions on the IPL[4:1] and IJ0J1[4:1] inputs. IPCA[*X*] is set high when rising edges have been observed on both the IPL[*X*] and IJ0J1[*X*] inputs since the last read, and is set low after this register is read.

IDA[4:1]

The incoming data bus active bits (IDA[4:1]) monitor for low to high transitions on the ID[4:1][7:0] buses. IDA[*X*] is set high when rising edges have been observed on all the signals on the ID[*X*][7:0] bus since the last read, and is set low after this register is read.

Register 003H TBS Master Reset

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET	0
Bit 13	R/W	TWRESET	0
Bit 12	R/W	TPRESET	0
Bit 11	R/W	TARESET	0
Bit 10	R/W	RWRESET	0
Bit 9	R/W	RPRESET	0
Bit 8	R/W	RARESET	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RARESET

The receive auxiliary serial data link reset bit (RARESET) allows the circuitry supporting the RPAUX[4:1]/RNAUX[4:1] LVDS links in the TBS to be reset under software control. When the RARESET bit is set high, the blocks RALV #1 to #4, ADRU #1 to #4, RA8D #1 to #4 and the RATI are held in reset and/or disabled. When RARESET is set low, the receive auxiliary serial data links are active.

The RARESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the RARESET bit, thus negating the receive auxiliary serial data link software reset.

RPRESET

The receive protection serial data link reset bit (RPRESET) allows the circuitry supporting the RPPROT[4:1]/RNPROT[4:1] LVDS links in the TBS to be reset under software control. When the RPRESET bit is set high, the blocks RPLV #1 to #4, PDRU #1 to #4, RP8D #1 to #4, and the RPTI are held in reset and/or disabled. When RPRESET is set low, the receive protection serial data links are active.

The RPRESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the RPRESET bit, thus negating the receive protection serial data link software reset.

RWRESET

The receive working serial data link reset bit (RWRESET) allows the circuitry supporting the RPWRK[4:1]/RNWRK[4:1] LVDS links in the TBS to be reset under software control. When the RWRESET bit is set high, the blocks RWLV #1 to #4, WDRU #1 to #4, RW8D #1 to #4, and the RWTI are held in reset and/or disabled. When RWRESET is set low, the receive working serial data links are active.

The RWRESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the RWRESET bit, thus negating the receive working serial data link software reset.

TARESET

The transmit auxiliary serial data link reset bit (TARESET) allows the circuitry supporting the TPAUX[4:1]/TNAUX[4:1] LVDS links in the TBS to be reset under software control. When the TARESET bit is set high, the blocks TALV #1 to #4, TAPS #1 to #4, TADE #1 to #4, and TATI are held in reset and/or disabled. When TARESET is set low, the transmit auxiliary serial data links are active.

The TARESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the TARESET bit, thus negating the transmit auxiliary serial data link software reset.

TPRESET

The transmit protection serial data link reset bit (TPRESET) allows the circuitry supporting the TPPROT[4:1]/TNPROT[4:1] LVDS links in the TBS to be reset under software control. When the TPRESET bit is set high, the blocks TPLV #1 to #4, TPPS #1 to #4, TPDE #1 to #4, and TPTI are held in reset and/or disabled. When TPRESET is set low, the transmit protection serial data links are active.

The TPRESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the TPRESET bit, thus negating the transmit protection serial data link software reset.

TWRESET

The transmit working serial data link reset bit (TWRESET) allows the circuitry supporting the TPWRK[4:1]/TNWRK[4:1] LVDS links in the TBS to be reset under software control. When the TWRESET bit is set high, the blocks TWLV #1 to #4, TWPS #1 to #4, TWDE #1 to #4, and TWTI are held in reset and/or disabled. When TWRESET is set low, the transmit working serial data links are active.

The TWRESET bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. A hardware reset clears the TWRESET bit, thus negating the transmit working serial data link software reset.

ARESET

The analog reset bit (ARESET) allows the analog circuitry in the TBS to be reset and disabled under software control. When the ARESET bit is set high, all TBS analog circuitry is held in reset and disabled. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset and enable it. Holding TBS in analog reset state places it into a low power, disabled mode. Note that the CSTR will be reset but will remain enabled, so that it is in a standby mode. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET

The digital reset bit (DRESET) allows the digital circuitry in the TBS to be reset under software control. When the DRESET bit is set high, all TBS digital circuitry is held in reset with the exception of this register and the CSU portion of the CSTR. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. Holding TBS in digital reset state places it into a low power, digital standby mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 004H TBS Master Parity Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	IPI[4]	X
Bit 6	R	IPI[3]	X
Bit 5	R	IPI[2]	X
Bit 4	R	IPI[1]	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports the status of the Incoming TelecomBus stream parity checkers in the TBS.

IPI[4:1]

The incoming parity error interrupt bits (IPI[4:1]) report parity errors in the Incoming TelecomBus stream. IPI[*X*] is set high when a parity error is detected on IDP[*X*]. If the corresponding IPE[*X*] bit in the TBS Master Incoming Configuration and Control register is set high, the interrupt output (INTB) is activated. When this register is read, all four IPI[4:1] bits (and the corresponding interrupt) are cleared.

Register 005H TBS Master Accumulation Transfer and Receive Synchronization Delay

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14		Unused	X
Bit 13	R/W	RJ0DLY[13]	0
Bit 12	R/W	RJ0DLY[12]	0
Bit 11	R/W	RJ0DLY[11]	0
Bit 10	R/W	RJ0DLY[10]	0
Bit 9	R/W	RJ0DLY[9]	0
Bit 8	R/W	RJ0DLY[8]	0
Bit 7	R/W	RJ0DLY[7]	0
Bit 6	R/W	RJ0DLY[6]	0
Bit 5	R/W	RJ0DLY[5]	0
Bit 4	R/W	RJ0DLY[4]	0
Bit 3	R/W	RJ0DLY[3]	0
Bit 2	R/W	RJ0DLY[2]	0
Bit 1	R/W	RJ0DLY[1]	0
Bit 0	R/W	RJ0DLY[0]	0

This register reports the status of the transfer of performance monitor counts to holding register and controls the delay from the RJ0FP input signal to the time when the TBS may safely process the J0 characters delivered by the receive working serial data links (RPWRK[4:1]/RNWRK[4:1]), the receive protection serial data links (RPPROT[4:1]/RNPROT[4:1]), and the receive auxiliary serial data links (RPAUX[4:1]/RNAUX[4:1]).

RJ0DLY[13:0]

The receive transport frame delay bits (RJ0FP[13:0]) controls the delay, in SYSCLK cycles, inserted by the TBS before processing the J0 characters delivered by the three sets of the receive working serial data links (RPWRK[4:1]/RNWRK[4:1], RPPROT[4:1]/RNPROT[4:1], and RPAUX[4:1]/RNAUX[4:1]). RJ0DLY is set such that after the specified delay, all active receive links would have delivered the J0 character. The relationships of RJ0FP, RJ0DLY[13:0] and the system configuration are described in Figures 3 and 4 of the Functional Timing section.

TIP

The transfer in progress bit (TIP) reports the status of latching performance monitor counting into holding registers. TIP is set high when a transfer is initiated by a write access to the TBS Master Input Signal Activity, Accumulation Trigger register. It is set low when all the counters in the TBS have transferred their values to holding registers. The updated counts are now available for reading at the designated registers.

Register 006H FREE User Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

This register holds whatever value is written into it and is available for user use. This register is cleared by reset.

FREE[7:0]

The software ID register (FREE) holds whatever value is written into it. Reset clears the contents of this register. This register has no impact on the operation of the TBS.

Register 008H TBS Master Interrupt Enable #1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	Reserved	0
Bit 13	R/W	RWPME[1]	0
Bit 12	R/W	RPPME[1]	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	RW8DE[1]	0
Bit 9	R/W	RP8DE[1]	0
Bit 8	R/W	RA8DE/RAPME[1]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	TWDEE[1]	0
Bit 3	R/W	TPDEE[1]	0
Bit 2	R/W	TADEE[1]	0
Bit 1	R/W	ITPPE[1]	0
Bit 0	R/W	Reserved	0

This register enables interrupts originating from the ITPP #1, TADE #1, TPDE #1, TWDE #1, RA8D #1, RP8D #1, RW8D #1, RAPM #1, RPPM #1, RWPM #1 blocks in the TBS.

ITPPE[1]

The ITPP #1 interrupt enable bit (ITPPE[1]) enables the block ITPP #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in ITPP #1 to determine the event causing the interrupt and to clear the interrupt. The ITPPE[1] bit will not affect interrupts disabled at ITPP #1.

TADEE[1]

The TADE #1 interrupt enable bit (TADEE[1]) enables the block TADE #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TADE #1 to determine the event causing the interrupt and to clear the interrupt. The TADEE[1] bit will not affect interrupts disabled at TADE #1.

TPDEE[1]

The TPDE #1 interrupt enable bit (TPDEE[1]) enables the block TPDE #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TPDE #1 to determine the event causing the interrupt and to clear the interrupt. The TPDEE[1] bit will not affect interrupts disabled at TPDE #1.

TWDEE[1]

The TWDE #1 interrupt enable bit (TWDEE[1]) enables the block TWDE #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TWDE #1 to determine the event causing the interrupt and to clear the interrupt. The TWDEE[1] bit will not affect interrupts disabled at TWDE #1.

RA8DE/RAPME[1]

The RA8D #1 and RAPM #1 interrupt enable bit (RA8DE/RAPME[1]) enables the blocks RA8D #1 and RAPM #1 as the sources of a pending interrupt. It is necessary to read the various interrupt enable registers in RA8D #1 and RAPM #1 to determine the event causing the interrupt and to clear the interrupt. The RA8DE/RAPME[1] bit will not affect interrupts disabled at RA8D #1 and RAPM #1.

RP8DE[1]

The RP8D #1 interrupt enable bit (RP8DE[1]) enables the block RP8D #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RP8D #1 to determine the event causing the interrupt and to clear the interrupt. The RP8DE[1] bit will not affect interrupts disabled at RP8D #1.

RW8DE[1]

The RW8D #1 interrupt enable bit (RW8DE[1]) enables the block RW8D #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RW8D #1 to determine the event causing the interrupt and to clear the interrupt. The RW8DE[1] bit will not affect interrupts disabled at RW8D #1.

RPPME[1]

The RPPM #1 interrupt enable bit (RPPME[1]) enables the block RPPM #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RPPM #1 to determine the event causing the interrupt and to clear the interrupt. The RPPME[1] bit will not affect interrupts disabled at RPPM #1.

RWPME[1]

The RWPM #1 interrupt enable bit (RWPME[1]) enables the block RWPM #1 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RWPM #1 to determine the event causing the interrupt and to clear the interrupt. The RWPME[1] bit will not affect interrupts disabled at RWPM #1.

Reserved

The reserved bits (RESERVED) must be set to set low for correct operation of the TBS.

Register 009H TBS Master Interrupt Enable #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	Reserved	0
Bit 13	R/W	RWPME[2]	0
Bit 12	R/W	RPPME[2]	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	RW8DE[2]	0
Bit 9	R/W	RP8DE[2]	0
Bit 8	R/W	RA8DE/RAPME[2]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	TWDEE[2]	0
Bit 3	R/W	TPDEE[2]	0
Bit 2	R/W	TADEE[2]	0
Bit 1	R/W	ITPPE[2]	0
Bit 0	R/W	Reserved	0

This register enables interrupts originating from the ITPP #2, TADE #2, TPDE #2, TWDE #2, RA8D #2, RP8D #2, RW8D #2, RAPM #2, RPPM #2, RWPM #2 blocks in the TBS.

ITPPE[2]

The ITPP #2 interrupt enable bit (ITPPE[2]) enables the block ITPP #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in ITPP #2 to determine the event causing the interrupt and to clear the interrupt. The ITPPE[2] bit will not affect interrupts disabled at ITPP #2.

TADEE[2]

The TADE #2 interrupt enable bit (TADEE[2]) enables the block TADE #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TADE #2 to determine the event causing the interrupt and to clear the interrupt. The TADEE[2] bit will not affect interrupts disabled at TADE #2.

TPDEE[2]

The TPDE #2 interrupt enable bit (TPDEE[2]) enables the block TPDE #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TPDE #2 to determine the event causing the interrupt and to clear the interrupt. The TPDEE[2] bit will not affect interrupts disabled at TPDE #2.

TWDEE[2]

The TWDE #2 interrupt enable bit (TWDEE[2]) enables the block TWDE #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TWDE #2 to determine the event causing the interrupt and to clear the interrupt. The TWDEE[2] bit will not affect interrupts disabled at TWDE #2.

RA8DE/RAPME[2]

The RA8D #2 and RAPM #2 interrupt enable bit (RA8DE/RAPME[2]) enables the blocks RA8D #2 and RAPM #2 as the sources of a pending interrupt. It is necessary to read the various interrupt enable registers in RA8D #2 and RAPM #2 to determine the event causing the interrupt and to clear the interrupt. The RA8DE/RAPME[2] bit will not affect interrupts disabled at RA8D #2 and RAPM #2.

RP8DE[2]

The RP8D #2 interrupt enable bit (RP8DE[2]) enables the block RP8D #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RP8D #2 to determine the event causing the interrupt and to clear the interrupt. The RP8DE[2] bit will not affect interrupts disabled at RP8D #2.

RW8DE[2]

The RW8D #2 interrupt enable bit (RW8DE[2]) enables the block RW8D #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RW8D #2 to determine the event causing the interrupt and to clear the interrupt. The RW8DE[2] bit will not affect interrupts disabled at RW8D #2.

RPPME[2]

The RPPM #2 interrupt enable bit (RPPME[2]) enables the block RPPM #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RPPM #2 to determine the event causing the interrupt and to clear the interrupt. The RPPME[2] bit will not affect interrupts disabled at RPPM #2.

RWPME[2]

The RWPM #2 interrupt enable bit (RWPME[2]) enables the block RWPM #2 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RWPM #2 to determine the event causing the interrupt and to clear the interrupt. The RWPME[2] bit will not affect interrupts disabled at RWPM #2.

Reserved

The reserved bits (RESERVED) must be set to set low for correct operation of the TBS.

Register 00AH TBS Master Interrupt Enable #3

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	Reserved	0
Bit 13	R/W	RWPME[3]	0
Bit 12	R/W	RPPME[3]	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	RW8DE[3]	0
Bit 9	R/W	RP8DE[3]	0
Bit 8	R/W	RA8DE/RAPME[3]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	TWDEE[3]	0
Bit 3	R/W	TPDEE[3]	0
Bit 2	R/W	TADEE[3]	0
Bit 1	R/W	ITPPE[3]	0
Bit 0	R/W	Reserved	0

This register enables interrupts originating from the ITPP #3, TADE #3, TPDE #3, TWDE #3, RA8D #3, RP8D #3, RW8D #3, RAPM #3, RPPM #3, RWPM #3 blocks in the TBS.

ITPPE[3]

The ITPP #3 interrupt enable bit (ITPPE[3]) enables the block ITPP #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in ITPP #3 to determine the event causing the interrupt and to clear the interrupt. The ITPPE[3] bit will not affect interrupts disabled at ITPP #3.

TADEE[3]

The TADE #3 interrupt enable bit (TADEE[3]) enables the block TADE #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TADE #3 to determine the event causing the interrupt and to clear the interrupt. The TADEE[3] bit will not affect interrupts disabled at TADE #3.

TPDEE[3]

The TPDE #3 interrupt enable bit (TPDEE[3]) enables the block TPDE #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TPDE #3 to determine the event causing the interrupt and to clear the interrupt. The TPDEE[3] bit will not affect interrupts disabled at TPDE #3.

TWDEE[3]

The TWDE #3 interrupt enable bit (TWDEE[3]) enables the block TWDE #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TWDE #3 to determine the event causing the interrupt and to clear the interrupt. The TWDEE[3] bit will not affect interrupts disabled at TWDE #3.

RA8DE/RAPME[3]

The RA8D #3 and RAPM #3 interrupt enable bit (RA8DE/RAPME[3]) enables the blocks RA8D #3 and RAPM #3 as the sources of a pending interrupt. It is necessary to read the various interrupt enable registers in RA8D #3 and RAPM #3 to determine the event causing the interrupt and to clear the interrupt. The RA8DE/RAPME[3] bit will not affect interrupts disabled at RA8D #3 and RAPM #3.

RP8DE[3]

The RP8D #3 interrupt enable bit (RP8DE[3]) enables the block RP8D #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RP8D #3 to determine the event causing the interrupt and to clear the interrupt. The RP8DE[3] bit will not affect interrupts disabled at RP8D #3.

RW8DE[3]

The RW8D #3 interrupt enable bit (RW8DE[3]) enables the block RW8D #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RW8D #3 to determine the event causing the interrupt and to clear the interrupt. The RW8DE[3] bit will not affect interrupts disabled at RW8D #3.

RPPME[3]

The RPPM #3 interrupt enable bit (RPPME[3]) enables the block RPPM #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RPPM #3 to determine the event causing the interrupt and to clear the interrupt. The RPPME[3] bit will not affect interrupts disabled at RPPM #3.

RWPME[3]

The RWPM #3 interrupt enable bit (RWPME[3]) enables the block RWPM #3 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RWPM #3 to determine the event causing the interrupt and to clear the interrupt. The RWPME[3] bit will not affect interrupts disabled at RWPM #3.

Reserved

The reserved bits (RESERVED) must be set to set low for correct operation of the TBS.

Register 00BH TBS Master Interrupt Enable #4

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R/W	Reserved	0
Bit 13	R/W	RWPME[4]	0
Bit 12	R/W	RPPME[4]	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	RW8DE[4]	0
Bit 9	R/W	RP8DE[4]	0
Bit 8	R/W	RA8DE/RAPME[4]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	TWDEE[4]	0
Bit 3	R/W	TPDEE[4]	0
Bit 2	R/W	TADEE[4]	0
Bit 1	R/W	ITPPE[4]	0
Bit 0	R/W	Reserved	0

This register enables interrupts originating from the ITPP #4, TADE #4, TPDE #4, TWDE #4, RA8D #4, RP8D #4, RW8D #4, RAPM #4, RPPM #4, RWPM #4 blocks in the TBS.

ITPPE[4]

The ITPP #4 interrupt enable bit (ITPPE[4]) enables the block ITPP #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in ITPP #4 to determine the event causing the interrupt and to clear the interrupt. The ITPPE[4] bit will not affect interrupts disabled at ITPP #4.

TADEE[4]

The TADE #4 interrupt enable bit (TADEE[4]) enables the block TADE #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TADE #4 to determine the event causing the interrupt and to clear the interrupt. The TADEE[4] bit will not affect interrupts disabled at TADE #4.

TPDEE[4]

The TPDE #4 interrupt enable bit (TPDEE[4]) enables the block TPDE #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TPDE #4 to determine the event causing the interrupt and to clear the interrupt. The TPDEE[4] bit will not affect interrupts disabled at TPDE #4.

TWDEE[4]

The TWDE #4 interrupt enable bit (TWDEE[4]) enables the block TWDE #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TWDE #4 to determine the event causing the interrupt and to clear the interrupt. The TWDEE[4] bit will not affect interrupts disabled at TWDE #4.

RA8DE/RAPME[4]

The RA8D #4 and RAPM #4 interrupt enable bit (RA8DE/RAPME[4]) enables the blocks RA8D #4 and RAPM #4 as the sources of a pending interrupt. It is necessary to read the various interrupt enable registers in RA8D #4 and RAPM #4 to determine the event causing the interrupt and to clear the interrupt. The RA8DE/RAPME[4] bit will not affect interrupts disabled at RA8D #4 and RAPM #4.

RP8DE[4]

The RP8D #4 interrupt enable bit (RP8DE[4]) enables the block RP8D #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RP8D #4 to determine the event causing the interrupt and to clear the interrupt. The RP8DE[4] bit will not affect interrupts disabled at RP8D #4.

RW8DE[4]

The RW8D #4 interrupt enable bit (RW8DE[4]) enables the block RW8D #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RW8D #4 to determine the event causing the interrupt and to clear the interrupt. The RW8DE[4] bit will not affect interrupts disabled at RW8D #4.

RPPME[4]

The RPPM #4 interrupt enable bit (RPPME[4]) enables the block RPPM #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RPPM #4 to determine the event causing the interrupt and to clear the interrupt. The RPPME[4] bit will not affect interrupts disabled at RPPM #4.

RWPME[4]

The RWPM #4 interrupt enable bit (RWPME[4]) enables the block RWPM #4 as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RWPM #4 to determine the event causing the interrupt and to clear the interrupt. The RWPME[4] bit will not affect interrupts disabled at RWPM #4.

Reserved

The reserved bits (RESERVED) must be set to set low for correct operation of the TBS.

Register 00CH TBS Master TSI, DLL and CSTR Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R/W	DLLE	0
Bit 11	R/W	CSTRE	0
Bit 10	R/W	TWTIE	0
Bit 9	R/W	TPTIE	0
Bit 8	R/W	TATIE	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	RWPTIE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RATIE	0

This register enables interrupts originating from the TSI, DLL and CSTR blocks.

RATIE

The RATI interrupt enable bit (RATIE) enables the block RATI as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in RATI to determine the event causing the interrupt and to clear the interrupt. The RATIE bit will not affect interrupts disabled at RATI.

RWPTIE

The RWTI and RPTI interrupt enable bit (RWPTIE) enables the blocks RWTI and RPTI as the sources of a pending interrupt. It is necessary to read the various interrupt enable registers in RWTI and RPTI to determine the event causing the interrupt and to clear the interrupt. The RWPTIE bit will not affect interrupts disabled at RWTI and RPTI.

TATIE

The TATI interrupt enable bit (TATIE) enables the block TATI as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TATI to determine the event causing the interrupt and to clear the interrupt. The TATIE bit will not affect interrupts disabled at TATI.

TPTIE

The TPTI interrupt enable bit (TPTIE) enables the block TPTI as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TPTI to determine the event causing the interrupt and to clear the interrupt. The TPTIE bit will not affect interrupts disabled at TPTI.

TWTIE

The TWTI interrupt enable bit (TWTIE) enables the block TWTI as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in TWTI to determine the event causing the interrupt and to clear the interrupt. The TWTIE bit will not affect interrupts disabled at TWTI.

CSTRE

The CSTR interrupt enable bit (CSTRE) enables the block CSTR as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in CSTR to determine the event causing the interrupt and to clear the interrupt. The CSTRE bit will not affect interrupts disabled at CSTR.

DLLE

The DLL interrupt enable bit (DLLE) enables the block DLL as the source of a pending interrupt. It is necessary to read the various interrupt enable registers in DLL to determine the event causing the interrupt and to clear the interrupt. The DLLE bit will not affect interrupts disabled at DLL.

Register 00DH TBS Master Interrupt Status #1

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R	Reserved	0
Bit 13	R	RWPMI[1]	0
Bit 12	R	RPPMI[1]	0
Bit 11	R	RAPMI[1]	0
Bit 10	R	RW8DI[1]	0
Bit 9	R	RP8DI[1]	0
Bit 8	R	RA8DI[1]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	Reserved	0
Bit 4	R	TWDEI[1]	0
Bit 3	R	TPDEI[1]	0
Bit 2	R	TADEI[1]	0
Bit 1	R	ITPPI[1]	0
Bit 0	R	Reserved	0

This register reports the interrupt status of the ITPP #1, TADE #1, TPDE #1, TWDE #1, RA8D #1, RP8D #1, RW8D #1, RAPM #1, RPPM #1, RWPM #1 blocks in the TBS.

ITPPI[1]

The ITPP #1 interrupt status bit (ITPPI[1]) identifies the block ITPP #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in ITPP #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at ITPP #1 will not be reported by the ITPPI[1] bit.

TADEI[1]

The TADE #1 interrupt status bit (TADEI[1]) identifies the block TADE #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TADE #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TADE #1 will not be reported by the TADEI[1] bit.

TPDEI[1]

The TPDE #1 interrupt status bit (TPDEI[1]) identifies the block TPDE #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TPDE #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TPDE #1 will not be reported by the TPDEI[1] bit.

TWDEI[1]

The TWDE #1 interrupt status bit (TWDEI[1]) identifies the block TWDE #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TWDE #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TWDE #1 will not be reported by the TWDEI[1] bit.

RA8DI[1]

The RA8D #1 interrupt status bit (RA8DI[1]) identifies the block RA8D #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RA8D #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RA8D #1 will not be reported by the RA8DI[1] bit.

RP8DI[1]

The RP8D #1 interrupt status bit (RP8DI[1]) identifies the block RP8D #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RP8D #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RP8D #1 will not be reported by the RP8DI[1] bit.

RW8DI[1]

The RW8D #1 interrupt status bit (RW8DI[1]) identifies the block RW8D #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RW8D #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RW8D #1 will not be reported by the RW8DI[1] bit.

RAPMI[1]

The RAPM #1 interrupt status bit (RAPMI[1]) identifies the block RAPM #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RAPM #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RAPM #1 will not be reported by the RAPMI[1] bit.

RPPMI[1]

The RPPM #1 interrupt status bit (RPPMI[1]) identifies the block RPPM #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RPPM #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RPPM #1 will not be reported by the RPPMI[1] bit. Note that though the RPPM shares logic with the OTPG, this interrupt can only be generated by the RPPM.

RWPMI[1]

The RWPM #1 interrupt status bit (RWPMI[1]) identifies the block RWPM #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RWPM #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RWPM #1 will not be reported by the RWPMI[1] bit.

Reserved

The reserved bits are read only and should be ignored by users.

Register 00EH TBS Master Interrupt Status #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R	Reserved	0
Bit 13	R	RWPMI[2]	0
Bit 12	R	RPPMI[2]	0
Bit 11	R	RAPMI[2]	0
Bit 10	R	RW8DI[2]	0
Bit 9	R	RP8DI[2]	0
Bit 8	R	RA8DI[2]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	Reserved	0
Bit 4	R	TWDEI[2]	0
Bit 3	R	TPDEI[2]	0
Bit 2	R	TADEI[2]	0
Bit 1	R	ITPPI[2]	0
Bit 0	R	Reserved	0

This register reports the interrupt status of the ITPP #2, TADE #2, TPDE #2, TWDE #2, RA8D #2, RP8D #2, RW8D #2, RAPM #2, RPPM #2, RWPM #2 blocks in the TBS.

ITPPI[2]

The ITPP #2 interrupt status bit (ITPPI[2]) identifies the block ITPP #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in ITPP #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at ITPP #2 will not be reported by the ITPPI[2] bit.

TADEI[2]

The TADE #2 interrupt status bit (TADEI[2]) identifies the block TADE #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TADE #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TADE #2 will not be reported by the TADEI[2] bit.

TPDEI[2]

The TPDE #2 interrupt status bit (TPDEI[2]) identifies the block TPDE #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TPDE #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TPDE #2 will not be reported by the TPDEI[2] bit.

TWDEI[2]

The TWDE #2 interrupt status bit (TWDEI[2]) identifies the block TWDE #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TWDE #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TWDE #2 will not be reported by the TWDEI[2] bit.

RA8DI[2]

The RA8D #2 interrupt status bit (RA8DI[2]) identifies the block RA8D #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RA8D #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RA8D #2 will not be reported by the RA8DI[2] bit.

RP8DI[2]

The RP8D #2 interrupt status bit (RP8DI[2]) identifies the block RP8D #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RP8D #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RP8D #2 will not be reported by the RP8DI[2] bit.

RW8DI[2]

The RW8D #2 interrupt status bit (RW8DI[2]) identifies the block RW8D #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RW8D #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RW8D #2 will not be reported by the RW8DI[2] bit.

RAPMI[2]

The RAPM #2 interrupt status bit (RAPMI[2]) identifies the block RAPM #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RAPM #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RAPM #2 will not be reported by the RAPMI[2] bit.

RPPMI[2]

The RPPM #2 interrupt status bit (RPPMI[2]) identifies the block RPPM #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RPPM #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RPPM #2 will not be reported by the RPPMI[2] bit. Note that though the RPPM shares logic with the OTPG, this interrupt can only be generated by the RPPM.

RWPMI[2]

The RWPM #2 interrupt status bit (RWPMI[2]) identifies the block RWPM #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RWPM #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RWPM #2 will not be reported by the RWPMI[2] bit.

Reserved

The reserved bits are read only and should be ignored by users.

Register 00FH TBS Master Interrupt Status #3

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R	Reserved	0
Bit 13	R	RWPMI[3]	0
Bit 12	R	RPPMI[3]	0
Bit 11	R	RAPMI[3]	0
Bit 10	R	RW8DI[3]	0
Bit 9	R	RP8DI[3]	0
Bit 8	R	RA8DI[3]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	Reserved	0
Bit 4	R	TWDEI[3]	0
Bit 3	R	TPDEI[3]	0
Bit 2	R	TADEI[3]	0
Bit 1	R	ITPPI[3]	0
Bit 0	R	Reserved	0

This register reports the interrupt status of the ITPP #3, TADE #3, TPDE #3, TWDE #3, RA8D #3, RP8D #3, RW8D #3, RAPM #3, RPPM #3, RWPM #3 blocks in the TBS.

ITPPI[3]

The ITPP #3 interrupt status bit (ITPPI[3]) identifies the block ITPP #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in ITPP #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at ITPP #3 will not be reported by the ITPPI[3] bit.

TADEI[3]

The TADE #3 interrupt status bit (TADEI[3]) identifies the block TADE #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TADE #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TADE #3 will not be reported by the TADEI[3] bit.

TPDEI[3]

The TPDE #3 interrupt status bit (TPDEI[3]) identifies the block TPDE #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TPDE #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TPDE #3 will not be reported by the TPDEI[3] bit.

TWDEI[3]

The TWDE #3 interrupt status bit (TWDEI[3]) identifies the block TWDE #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TWDE #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TWDE #3 will not be reported by the TWDEI[3] bit.

RA8DI[3]

The RA8D #3 interrupt status bit (RA8DI[3]) identifies the block RA8D #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RA8D #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RA8D #3 will not be reported by the RA8DI[3] bit.

RP8DI[3]

The RP8D #3 interrupt status bit (RP8DI[3]) identifies the block RP8D #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RP8D #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RP8D #3 will not be reported by the RP8DI[3] bit.

RW8DI[3]

The RW8D #3 interrupt status bit (RW8DI[3]) identifies the block RW8D #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RW8D #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RW8D #3 will not be reported by the RW8DI[3] bit.

RAPMI[3]

The RAPM #3 interrupt status bit (RAPMI[3]) identifies the block RAPM #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RAPM #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RAPM #3 will not be reported by the RAPMI[3] bit.

RPPMI[3]

The RPPM #3 interrupt status bit (RPPMI[3]) identifies the block RPPM #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RPPM #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RPPM #3 will not be reported by the RPPMI[3] bit. Note that though the RPPM shares logic with the OTPG, this interrupt can only be generated by the RPPM.

RWPMI[3]

The RWPM #3 interrupt status bit (RWPMI[3]) identifies the block RWPM #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RWPM #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RWPM #3 will not be reported by the RWPMI[3] bit.

Reserved

The reserved bits are read only and should be ignored by users.

Register 010H TBS Master Interrupt Status #4

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14	R	Reserved	0
Bit 13	R	RWPMI[4]	0
Bit 12	R	RPPMI[4]	0
Bit 11	R	RAPMI[4]	0
Bit 10	R	RW8DI[4]	0
Bit 9	R	RP8DI[4]	0
Bit 8	R	RA8DI[4]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	Reserved	0
Bit 4	R	TWDEI[4]	0
Bit 3	R	TPDEI[4]	0
Bit 2	R	TADEI[4]	0
Bit 1	R	ITPPI[4]	0
Bit 0	R	Reserved	0

This register reports the interrupt status of the ITPP #4, TADE #4, TPDE #4, TWDE #4, RA8D #4, RP8D #4, RW8D #4, RAPM #4, RPPM #4, RWPM #4 blocks in the TBS.

ITPPI[4]

The ITPP #4 interrupt status bit (ITPPI[4]) identifies the block ITPP #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in ITPP #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at ITPP #4 will not be reported by the ITPPI[4] bit.

TADEI[4]

The TADE #4 interrupt status bit (TADEI[4]) identifies the block TADE #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TADE #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TADE #4 will not be reported by the TADEI[4] bit.

TPDEI[4]

The TPDE #4 interrupt status bit (TPDEI[4]) identifies the block TPDE #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TPDE #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TPDE #4 will not be reported by the TPDEI[4] bit.

TWDEI[4]

The TWDE #4 interrupt status bit (TWDEI[4]) identifies the block TWDE #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TWDE #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at TWDE #4 will not be reported by the TWDEI[4] bit.

RA8DI[4]

The RA8D #4 interrupt status bit (RA8DI[4]) identifies the block RA8D #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RA8D #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RA8D #4 will not be reported by the RA8DI[4] bit.

RP8DI[4]

The RP8D #4 interrupt status bit (RP8DI[4]) identifies the block RP8D #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RP8D #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RP8D #4 will not be reported by the RP8DI[4] bit.

RW8DI[4]

The RW8D #4 interrupt status bit (RW8DI[4]) identifies the block RW8D #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RW8D #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RW8D #4 will not be reported by the RW8DI[4] bit.

RAPMI[4]

The RAPM #4 interrupt status bit (RAPMI[4]) identifies the block RAPM #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RAPM #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RAPM #4 will not be reported by the RAPMI[4] bit.

RPPMI[4]

The RPPM #4 interrupt status bit (RPPMI[4]) identifies the block RPPM #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RPPM #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RPPM #4 will not be reported by the RPPMI[4] bit. Note that though the RPPM shares logic with the OTPG, this interrupt can only be generated by the RPPM.

RWPMI[4]

The RWPM #4 interrupt status bit (RWPMI[4]) identifies the block RWPM #4 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RWPM #4 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at RWPM #4 will not be reported by the RWPMI[4] bit.

Reserved

The reserved bits are read only and should be ignored by users.

Register 011H TBS Master TSI, DLL and CSTR Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	DLLI	0
Bit 11	R	CSTRI	0
Bit 10	R	TWTII	0
Bit 9	R	TPTII	0
Bit 8	R	TATII	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RWTII	0
Bit 1	R	RPTII	0
Bit 0	R	RATII	0

This register reports the interrupt status of the TSI, DLL and CSTR blocks.

RATII

The RATI interrupt status bit (RATII) identifies the block RATI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RATI to determine the event causing the interrupt and to clear the interrupt. The RATII bit will not report interrupts disabled at RATI.

RPTII

The RPTI interrupt status bit (RPTII) identifies the block RPTI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RPTI to determine the event causing the interrupt and to clear the interrupt. The RPTII bit will not report interrupts disabled at RPTI.

RWTII

The RWTI interrupt status bit (RWTII) identifies the block RWTI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in RWTI to determine the event causing the interrupt and to clear the interrupt. The RWTII bit will not report interrupts disabled at RWTI.

TATII

The TATI interrupt status bit (TATII) identifies the block TATI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TATI to determine the event causing the interrupt and to clear the interrupt. The TATII bit will not report interrupts disabled at TATI.

TPTII

The TPTI interrupt status bit (TPTII) identifies the block TPTI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TPTI to determine the event causing the interrupt and to clear the interrupt. The TPTII bit will not report interrupts disabled at TPTI.

TWTII

The TWTI interrupt status bit (TWTII) identifies the block TWTI as the source of a pending interrupt. It is necessary to read the various interrupt status registers in TWTI to determine the event causing the interrupt and to clear the interrupt. The TWTII bit will not report interrupts disabled at TWTI.

CSTRI

The CSTR interrupt status bit (CSTRI) identifies the block CSTR as the source of a pending interrupt. It is necessary to read the various interrupt status registers in CSTR to determine the event causing the interrupt and to clear the interrupt. The CSTRI bit will not report interrupts disabled at CSTR.

DLLI

The DLL interrupt status bit (DLLI) identifies the block DLL as the source of a pending interrupt. It is necessary to read the various interrupt status registers in DLL to determine the event causing the interrupt and to clear the interrupt. The DLLI bit will not report interrupts disabled at DLL.

Register 012H TBS Version/Part Number

Bit	Type	Function	Default
Bit 15	R	VERSION[3]	0
Bit 14	R	VERSION[2]	0
Bit 13	R	VERSION[1]	0
Bit 12	R	VERSION[0]	1
Bit 11	R	PART NUMBER[15]	0
Bit 10	R	PART NUMBER[14]	1
Bit 9	R	PART NUMBER[13]	0
Bit 8	R	PART NUMBER[12]	1
Bit 7	R	PART NUMBER[11]	0
Bit 6	R	PART NUMBER[10]	0
Bit 5	R	PART NUMBER[9]	1
Bit 4	R	PART NUMBER[8]	1
Bit 3	R	PART NUMBER[7]	0
Bit 2	R	PART NUMBER[6]	0
Bit 1	R	PART NUMBER[5]	0
Bit 0	R	PART NUMBER[4]	1

This register reports the version number and the 12 most significant bits of the part number for the TBS.

PART NUMBER

The PART NUMBER[15:4] bits represent the 12 most significant bits of the part number of the TBS device.

VERSION

The VERSION[3:0] bits report the revision of the TBS silicon.

Register 013H TBS Part Number/Manufacturer ID

Bit	Type	Function	Default
Bit 15	R	PART NUMBER[3]	0
Bit 14	R	PART NUMBER[2]	0
Bit 13	R	PART NUMBER[1]	0
Bit 12	R	PART NUMBER[0]	0
Bit 11	R	MANUFACTURER ID[10]	0
Bit 10	R	MANUFACTURER ID[9]	0
Bit 9	R	MANUFACTURER ID[8]	0
Bit 8	R	MANUFACTURER ID[7]	0
Bit 7	R	MANUFACTURER ID[6]	1
Bit 6	R	MANUFACTURER ID[5]	1
Bit 5	R	MANUFACTURER ID[4]	0
Bit 4	R	MANUFACTURER ID[3]	0
Bit 3	R	MANUFACTURER ID[2]	1
Bit 2	R	MANUFACTURER ID[1]	1
Bit 1	R	MANUFACTURER ID[0]	0
Bit 0	R	Unused	1

This register reports the 4 least significant bits of the part number for the TBS as well as the 11 bit manufacturer's ID code.

MANUFACTURER ID

The MANUFACTURER ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code. For more information on JTAG Boundary Scan, refer to section 14.1.

PART NUMBER

The PART NUMBER[3:0] bits represent the 4 least significant bits of the part number of the TBS device.

Register 020H TWTI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	IWDTSEL[3]	0
Bit 6	R/W	IWDTSEL[2]	0
Bit 5	R/W	IWDTSEL[1]	0
Bit 4	R/W	IWDTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IWDSEL[1]	0
Bit 0	R/W	IWDSEL[0]	0

This register provides the incoming working data stream number, the time-slot number, and the page number used to access the connection memory pages in the TWTI block. Writing to this register triggers an indirect register access.

IWDSEL[1:0]

The incoming working data stream selection bits (IWDSEL[1:0]) select which incoming working data stream is accessed by the current indirect transfer. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IWDTSEL[3:0] of the internal data stream IWDSEL[1:0].

IWDSEL[1:0]	Incoming Working Data Stream
00	IWD[1][7:0]
01	IWD[2][7:0]
10	IWD[3][7:0]
11	IWD[4][7:0]

IWDTSEL[3:0]

The indirect incoming working data stream time-slot select bits (IWDTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the incoming working data stream selected by IWDSEL[1:0] that is accessed in the current indirect access. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IWDTSEL[3:0] of the internal working data stream IWDSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

IWDTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the TWTI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the TWTI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the TWTI Indirect Data Register or when another write access can be initiated.

Register 021H TWTI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	CHARACTER OVERWRITE[1]	0
Bit 12	R/W	CHARACTER OVERWRITE[0]	0
Bit 11	R/W	IP8ESEL	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IC[9]	0
Bit 8	R/W	IC[8]	0
Bit 7	R/W	IDTSEL[3]/IC[7]	0
Bit 6	R/W	IDTSEL[2]/IC[6]	0
Bit 5	R/W	IDTSEL[1]/IC[5]	0
Bit 4	R/W	IDTSEL[0]/IC[4]	0
Bit 3	R/W	IC[3]	0
Bit 2	R/W	IC[2]	0
Bit 1	R/W	IDSEL[1]/IC[1]	0
Bit 0	R/W	IDSEL[0]/IC[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the data to be written to the connection memory pages in an indirect write operation to the TWTI block.

IDSEL[1:0]

The Incoming TelecomBus stream select bits (IDSEL[1:0]) report the data stream number read after an indirect read operation has completed. The data stream number to be written to the connect memory pages must be set up in this register before triggering a write. IDSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IWDTSEL[3:0] of the incoming working data stream IWDSEL[1:0]. IDSEL[1:0] shares register bit locations with IC[1:0].

IDSEL[1:0]	Incoming TelecomBus Stream
00	ID[1][7:0]
01	ID[2][7:0]
10	ID[3][7:0]
11	ID[4][7:0]

IDTSEL[3:0]

The Incoming TelecomBus time-slot select bits (IDTSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. IDTSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IWDTSEL[3:0] of the incoming working data stream IWDSEL[1:0]. IDTSEL[3:0] shares register bit locations with IC[7:4].

IDTSEL[3:0]	Incoming TelecomBus Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

IC[9:0]

The character overwrite code bits (IC[9:0]) reports the character overwrite code read after an indirect read operation has completed. The character overwrite code to be written to the connection memory pages must be set up in this register before triggering a write. IC[9:0] reflects the last value read or written until the completion of a subsequent indirect read operation. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming working data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] overwrites the entire STS-1 data stream including overhead bytes. IC[1:0] and IC[7:4] share register bit locations with IDSEL[1:0] and IDTSEL[3:0], respectively. Note that the overwrite character should be a valid 10 bit 8B/10B character code placed in IC[9:0] in most cases. The 10 bit code for the 8 bit value 00h is 100111 0100 (RD -) or 011000 1011(RD+). The 10 bit code for FFh is 101011 0001 (RD-) or 010100 1110 (RD+) where RD stands for running disparity.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS.

IP8ESEL

The Incoming PRBS 8B/10B Encoding Select bit (IP8ESEL) reports the data stream selection read after an indirect read operation has completed. The data stream selection to be written to the connection memory pages must be set up in this register before triggering a write. IP8ESEL reflects the last value read or written until the completion of a subsequent indirect read operation. The IP8ESEL bit selects the source of the internal incoming data stream. When IP8ESEL is set to 1 the PRBS data stream from the appropriate IP8E is selected. When the bit is set to 0 the non-PRBS data stream from the ID8E is selected.

CHARACTER OVERWRITE[1:0]

The character overwrite data insertion control bits (CHARACTER OVERWRITE[1:0]) report the value of character overwrite control bits read after an indirect read operation has completed. The value of the CHARACTER OVERWRITE[1:0] bits to be written to the connection memory pages must be set up in this register before triggering a write. CHARACTER OVERWRITE[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation CHARACTER OVERWRITE[1:0] control the source of the data on the internal output data streams. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming working data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] is placed on the internal output data stream. Control values of ‘b01 and ‘b10 are invalid.

Register 022H TWTI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	COAPE	0

This register configures the operation of the TWTI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the TWTI. When the COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

CMPSEL

The connection memory page select bit (CMPSEL) provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the TCMP input signal to determine which connection memory page is currently active.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the TWTI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 023H TWTI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the TWTI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events.

Register 030H TPTI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	IPDTSEL[3]	0
Bit 6	R/W	IPDTSEL[2]	0
Bit 5	R/W	IPDTSEL[1]	0
Bit 4	R/W	IPDTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IPDSEL[1]	0
Bit 0	R/W	IPDSEL[0]	0

This register provides the incoming protection data stream number, the time-slot number, and the page number used to access the connection memory pages in the TPTI block. Writing to this register triggers an indirect register access.

IPDSEL[1:0]

The incoming protection data stream selection bits (IPDSEL[1:0]) select which incoming protection data stream is accessed by the current indirect transfer. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IPDTSEL[3:0] of the internal data stream IPDSEL[1:0].

IPDSEL[1:0]	Incoming Protection Data Stream
00	IPD[1][7:0]
01	IPD[2][7:0]
10	IPD[3][7:0]
11	IPD[4][7:0]

IPDTSEL[3:0]

The indirect incoming protection data stream time-slot select bits (IPDTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the incoming protection data stream selected by IPDSEL[1:0] that is accessed in the current indirect access. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IPDTSEL[3:0] of the internal protection data stream IPDSEL[1:0]. Valid time-slot values are 'b0001 to 'b1100.

IPDTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the TPTI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the TPTI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the TPTI Indirect Data Register or when another write access can be initiated.

Register 031H TPTI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	CHARACTER OVERWRITE[1]	0
Bit 12	R/W	CHARACTER OVERWRITE[0]	0
Bit 11	R/W	IP8ESEL	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IC[9]	0
Bit 8	R/W	IC[8]	0
Bit 7	R/W	IDTSEL[3]/IC[7]	0
Bit 6	R/W	IDTSEL[2]/IC[6]	0
Bit 5	R/W	IDTSEL[1]/IC[5]	0
Bit 4	R/W	IDTSEL[0]/IC[4]	0
Bit 3	R/W	IC[3]	0
Bit 2	R/W	IC[2]	0
Bit 1	R/W	IDSEL[1]/IC[1]	0
Bit 0	R/W	IDSEL[0]/IC[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the to be data written to the connection memory pages in an indirect write operation to the TPTI block.

IDSEL[1:0]

The Incoming TelecomBus stream select bits (IDSEL[1:0]) report the data stream number read after an indirect read operation has completed. The data stream number to be written to the connect memory pages must be set up in this register before triggering a write. IDSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IPDTSEL[3:0] of the incoming protection data stream IPDSEL[1:0]. IDSEL[1:0] shares register bit locations with IC[1:0].

IDSEL[1:0]	Incoming TelecomBus Stream
00	ID[1][7:0]
01	ID[2][7:0]
10	ID[3][7:0]
11	ID[4][7:0]

IDTSEL[3:0]

The Incoming TelecomBus time-slot select bits (IDTSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. IDTSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IPDTSEL[3:0] of the incoming protection data stream IPDSEL[1:0]. IDTSEL[3:0] shares register bit locations with IC[7:4].

IDTSEL[3:0]	Incoming TelecomBus Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

IC[9:0]

The character overwrite code bits (IC[9:0]) reports the character overwrite code read after an indirect read operation has completed. The character overwrite code to be written to the connection memory pages must be set up in this register before triggering a write. IC[9:0] reflects the last value read or written until the completion of a subsequent indirect read operation. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming protection data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] overwrites the entire STS-1 data stream including overhead bytes. IC[1:0] and IC[7:4] share register bit locations with IDSEL[1:0] and IDTSEL[3:0], respectively. Note that the overwrite character should be a valid 10 bit 8B/10B character code placed in IC[9:0] in most cases. The 10 bit code for the 8 bit value 00h is 100111 0100 (RD -) or 011000 1011(RD+). The 10 bit code for FFh is 101011 0001 (RD-) or 010100 1110 (RD+) where RD stands for running disparity.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS

IP8ESEL

The Incoming PRBS 8B/10B Encoding Select bit (IP8ESEL) reports the data stream selection read after an indirect read operation has completed. The data stream selection to be written to the connection memory pages must be set up in this register before triggering a write. IP8ESEL reflects the last value read or written until the completion of a subsequent indirect read operation. The IP8ESEL bit selects the source of the internal incoming data stream. When IP8ESEL is set to 1 the PRBS data stream from the appropriate IP8E is selected. When the bit is set to 0 the non-PRBS data stream from the ID8E is selected.

CHARACTER OVERWRITE[1:0]

The character overwrite data insertion control bits (CHARACTER OVERWRITE[1:0]) report the value of character overwrite control bits read after an indirect read operation has completed. The value of the CHARACTER OVERWRITE[1:0] bits to be written to the connection memory pages must be set up in this register before triggering a write. CHARACTER OVERWRITE[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation CHARACTER OVERWRITE[1:0] control the source of the data on the internal output data streams. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming protection data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] is placed the internal output data stream. Control values of ‘b01 and ‘b10 are invalid.

Register 032H TPTI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	COAPE	0

This register configures the operation of the TPTI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the TPTI. When the COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

CMPSEL

The connection memory page select bit (CMPSEL) bit provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the TCMP input signal to determine which connection memory page is currently active.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the TPTI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 033H TPTI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the TPTI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events.

Register 040H TATI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	IADTSEL[3]	0
Bit 6	R/W	IADTSEL[2]	0
Bit 5	R/W	IADTSEL[1]	0
Bit 4	R/W	IADTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IADSEL[1]	0
Bit 0	R/W	IADSEL[0]	0

This register provides the incoming auxiliary data stream number, the time-slot number, and the page number used to access the connection memory pages in the TATI block. Writing to this register triggers an indirect register access.

IADSEL[1:0]

The incoming auxiliary data stream selection bits (IADSEL[1:0]) select which incoming auxiliary data stream is accessed by the current indirect transfer. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IADTSEL[3:0] of the internal data stream IADSEL[1:0].

IADSEL[1:0]	Incoming Auxiliary Data Stream
00	IAD[1][7:0]
01	IAD[2][7:0]
10	IAD[3][7:0]
11	IAD[4][7:0]

IADTSEL[3:0]

The indirect incoming auxiliary data stream time-slot select bits (IADTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the incoming auxiliary data stream selected by IADSEL[1:0] that is accessed in the current indirect access. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IADTSEL[3:0] of the internal auxiliary data stream IADSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

IADTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the TATI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the TATI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the TATI Indirect Data Register or when another write access can be initiated.

Register 041H TATI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	CHARACTER OVERWRITE[1]	0
Bit 12	R/W	CHARACTER OVERWRITE[0]	0
Bit 11	R/W	IP8ESEL	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IC[9]	0
Bit 8	R/W	IC[8]	0
Bit 7	R/W	IDTSEL[3]/IC[7]	0
Bit 6	R/W	IDTSEL[2]/IC[6]	0
Bit 5	R/W	IDTSEL[1]/IC[5]	0
Bit 4	R/W	IDTSEL[0]/IC[4]	0
Bit 3	R/W	IC[3]	0
Bit 2	R/W	IC[2]	0
Bit 1	R/W	IDSEL[1]/IC[1]	0
Bit 0	R/W	IDSEL[0]/IC[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the to be data written to the connection memory pages in an indirect write operation to the TATI block.

IDSEL[1:0]

The Incoming TelecomBus stream select bits (IDSEL[1:0]) report the data stream number read after an indirect read operation has completed. The data stream number to be written to the connect memory pages must be set up in this register before triggering a write. IDSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IADTSEL[3:0] of the incoming auxiliary data stream IADSEL[1:0]. IDSEL[1:0] shares register bit locations with IC[1:0].

IDSEL[1:0]	Incoming TelecomBus Stream
00	ID[1][7:0]
01	ID[2][7:0]
10	ID[3][7:0]
11	ID[4][7:0]

IDTSEL[3:0]

The Incoming TelecomBus time-slot select bits (IDTSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. IDTSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot IDTSEL[3:0] of Incoming TelecomBus IDSEL[1:0] is transferred to time-slot IADTSEL[3:0] of the incoming auxiliary data stream IADSEL[1:0]. IDTSEL[3:0] shares register bit locations with IC[7:4].

IDTSEL[3:0]	Incoming TelecomBus Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

IC[9:0]

The character overwrite code bits (IC[9:0]) reports the character overwrite code read after an indirect read operation has completed. The character overwrite code to be written to the connection memory pages must be set up in this register before triggering a write. IC[9:0] reflects the last value read or written until the completion of a subsequent indirect read operation. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming auxiliary data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] overwrites the entire STS-1 data stream including overhead bytes. IC[1:0] and IC[7:4] share register bit locations with IDSEL[1:0] and IDTSEL[3:0], respectively. Note that the overwrite character should be a valid 10 bit 8B/10B character code placed in IC[9:0] in most cases. The 10 bit code for the 8 bit value 00h is 100111 0100 (RD -) or 011000 1011(RD+). The 10 bit code for FFh is 101011 0001 (RD-) or 010100 1110 (RD+) where RD stands for running disparity.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS

IP8ESEL

The Incoming PRBS 8B/10B Encoding Select bit (IP8ESEL) reports the data stream selection read after an indirect read operation has completed. The data stream selection to be written to the connection memory pages must be set up in this register before triggering a write. IP8ESEL reflects the last value read or written until the completion of a subsequent indirect read operation. The IP8ESEL bit selects the source of the internal incoming data stream. When IP8ESEL is set to 1 the PRBS data stream from the appropriate IP8E is selected. When the bit is set to 0 the non-PRBS data stream from the ID8E is selected.

CHARACTER OVERWRITE[1:0]

The character overwrite data insertion control bits (CHARACTER OVERWRITE[1:0]) report the value of character overwrite control bits read after an indirect read operation has completed. The value of the CHARACTER OVERWRITE[1:0] bits to be written to the connection memory pages must be set up in this register before triggering a write. CHARACTER OVERWRITE[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation CHARACTER OVERWRITE[1:0] control the source of the data on the internal output data streams. When CHARACTER OVERWRITE[1:0] is set to ‘b00, data from the Incoming TelecomBus is re-ordered and placed on the incoming auxiliary data stream. When CHARACTER OVERWRITE[1:0] is set to ‘b11, the character overwrite code specified by IC[9:0] is placed the internal output data stream. Control values of ‘b01 and ‘b10 are invalid.

Register 042H TATI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	COAPE	0

This register configures the operation of the TATI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the TATI. When COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

CMPSEL

The connection memory page select bit (CMPSEL) bit provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the TCMP input signal to determine which connection memory page is currently active.

Reserved

The reserved bit (RESERVED) must be set to set low for correct operation of the TBS.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the TATI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 043H TATI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the TATI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events.

Register 050H DLL Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The DLL Configuration Register controls the basic operation of the DLL.

LOCK

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SYSCLK and the REFCLK signals. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates zero phase offset between the SYSCLK and the REFCLK signals for the first time.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt may be generated upon an assertion event of the ERROR register. When ERRORE is set low, changes in the ERROR status do not generate an interrupt, but the ERRORI and ERROR status bits are still valid and may be polled.

Reserved

The reserved bits (RESERVED) must be set to set low for correct operation of the TBS.

Register 052H DLL Reset

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

The DLL Reset Register is used to reset the DLL.

Writing any value to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 SYSCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0 and back to a lock position.

Reserved

The reserved bits are read only and should be ignored by the user.

Register 053H Control Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

NOTE:

1. Because the clear-on-read ERRORI bit is located in this register, polling the register to check the status of the RUN bit may inadvertently clear a pending ERRORI interrupt. Care should be taken to handle this possibility in software, perhaps by examining the ERRORI bit and responding appropriately during read accesses. Clearing the ERRORI bit will not change the status of the ERROR bit, so it is also possible to simply poll the ERROR bit and ignore ERRORI.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of REFCLK and the rising edge of SYSLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset (ECBI_RSTB) or a software reset (writing to register 2).

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate an appropriate delay that causes the rising edge of REFCLK to be aligned to the rising edge of SYSCLK. ERROR is set low when the DLL captures lock again. To recover from this condition, the DLL software reset should be activated by writing to register 052H.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the DLLI bit in register 011H will also go high when ERRORI goes high.

Reserved

The reserved bits (Reserved) are read only and should be ignored.

Register 080H RWTI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	0
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ODTSEL[3]	0
Bit 6	R/W	ODTSEL[2]	0
Bit 5	R/W	ODTSEL[1]	0
Bit 4	R/W	ODTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	ODSEL[1]	0
Bit 0	R/W	ODSEL[0]	0

This register provides the Outgoing TelecomBus data stream number, the time-slot number, and the page number used to access the connection memory pages in the RWTI block. Writing to this register triggers an indirect register access.

ODSEL[1:0]

The Outgoing TelecomBus data stream selection bits (ODSEL[1:0]) select which Outgoing TelecomBus data stream (OD[*X*][7:0]) is accessed by the current indirect transfer. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0].

ODSEL[1:0]	Outgoing TelecomBus Data Stream
00	OD[1][7:0]
01	OD[2][7:0]
10	OD[3][7:0]
11	OD[4][7:0]

ODTSEL[3:0]

The indirect Outgoing TelecomBus time-slot bits (ODTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the Outgoing TelecomBus data stream selected by IODSEL[1:0] that is accessed in the current indirect access. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

ODTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the RWTI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the RWTI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the RWTI Indirect Data Register or when another write access can be initiated.

Register 081H RWTI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	RWTSEN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	WTSEL[3]	0
Bit 6	R/W	WTSEL[2]	0
Bit 5	R/W	WTSEL[1]	0
Bit 4	R/W	WTSEL[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	WLSEL[1]	0
Bit 0	R/W	WLSEL[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the to be data written to the connection memory pages in an indirect write operation to the RWTI block.

WLSEL[1:0]

The working link select bits (WLSEL[1:0]) report the receive working serial TelecomBus link number read after an indirect read operation has completed. The receive working serial TelecomBus link number to be written to the connect memory pages must be set up in this register before triggering a write. WLSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot WTSEL[3:0] of the receive working serial TelecomBus link WLSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]

WLSEL[1:0]	Receive Working Serial TelecomBus Link
00	RPWRK[1]/RNWRK[1]
01	RPWRK[2]/RNWRK[2]
10	RPWRK[3]/RNWRK[3]
11	RPWRK[4]/RNWRK[4]

Reserved

The reserved bits (Reserved) must be set to low for correct operation of the TBS.

WTSEL[3:0]

The working time-slot select bits (WTSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. WTSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot WTSEL[3:0] of receive working serial TelecomBus link WLSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

WTSEL[3:0]	STS-1/STM-0 Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

RWTSEN

The receive working timeslot enable bit (RWTSEN) reports the timeslot enable value read after an indirect read operation has completed. The timeslot enable value to be written to the connection memory pages must be set up in this register before triggering a write. RWTSEN reflects the last value read or written until the completion of a subsequent indirect read operation. When RWTSEN is set high, the data from timeslot WTSEL[3:0] of the receive working serial TelecomBus link WLSEL[1:0] is transferred to timeslot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. For each timeslot, one and only one of RWTSEN, RPTSEN, RATSEN must be set high.

Register 082H RWTI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

This register configures the operation of the RWTI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the RWTI. When the COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering (switching) of the J0/Z0 bytes. This configuration bit only has an effect when the RWTI is in the user configured timeslot mapping mode – if the RWTI is in bypass mode then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not switched by the muxing block. When this bit is set to logic 1, normal switching of the J0/Z0 bytes is enabled.

CMPSEL

The connection memory page select bit (CMPSEL) bit provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the OCMP input signal to determine which connection memory page is currently active.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the RWTI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 083H RWTI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the RWTI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events.

Register 090H RPTI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	0
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ODTSEL[3]	0
Bit 6	R/W	ODTSEL[2]	0
Bit 5	R/W	ODTSEL[1]	0
Bit 4	R/W	ODTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	ODSEL[1]	0
Bit 0	R/W	ODSEL[0]	0

This register provides the Outgoing TelecomBus data stream number, the time-slot number, and the page number used to access the connection memory pages in the RPTI block. Writing to this register triggers an indirect register access.

ODSEL[1:0]

The Outgoing TelecomBus data stream selection bits (ODSEL[1:0]) select which Outgoing TelecomBus data stream (OD[*X*][7:0]) is accessed by the current indirect transfer. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0].

ODSEL[1:0]	Outgoing TelecomBus Data Stream
00	OD[1][7:0]
01	OD[2][7:0]
10	OD[3][7:0]
11	OD[4][7:0]

ODTSEL[3:0]

The indirect Outgoing TelecomBus time-slot bits (ODTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the Outgoing TelecomBus data stream selected by IODSEL[1:0] that is accessed in the current indirect access. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

ODTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the RPTI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the RPTI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the RPTI Indirect Data Register or when another write access can be initiated.

Register 091H RPTI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	RPTSEN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	PTSEL[3]	0
Bit 6	R/W	PTSEL[2]	0
Bit 5	R/W	PTSEL[1]	0
Bit 4	R/W	PTSEL[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	PLSEL[1]	0
Bit 0	R/W	PLSEL[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the to be data written to the connection memory pages in an indirect write operation to the RPTI block.

PLSEL[1:0]

The protection link select bits (PLSEL[1:0]) report the receive protection serial TelecomBus link number read after an indirect read operation has completed. The receive protection serial TelecomBus link number to be written to the connect memory pages must be set up in this register before triggering a write. PLSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot PTSEL[3:0] of the receive protection serial TelecomBus link PLSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]

PLSEL[1:0]	Receive Protection Serial TelecomBus Link
00	RPPROT[1]/RNPROT[1]
01	RPPROT[2]/RNPROT[2]
10	RPPROT[3]/RNPROT[3]
11	RPPROT[4]/RNPROT[4]

Reserved

The reserved bits (Reserved) must be set to low for correct operation of the TBS.

PTSEL[3:0]

The protection time-slot select bits (PTSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. PTSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot PTSEL[3:0] of receive protection serial TelecomBus link PLSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

PTSEL[3:0]	STS-1/STM-0 Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

RPTSEN

The receive protection timeslot enable bit (RPTSEN) reports the timeslot enable value read after an indirect read operation has completed. The timeslot enable value to be written to the connection memory pages must be set up in this register before triggering a write. RPTSEN reflects the last value read or written until the completion of a subsequent indirect read operation. When RPTSEN is set high, the data from timeslot PTSEL[3:0] of the receive protection serial TelecomBus link PLSEL[1:0] is transferred to timeslot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. For each timeslot, one and only one of RWTSEN, RPTSEN, RATSEN must be set high.

Register 092H RPTI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

This register configures the operation of the RPTI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the RPTI. When the COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering (switching) of the J0/Z0 bytes. This configuration bit only has an effect when the RPTI is in the user configured timeslot mapping mode – if the RPTI is in bypass mode then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not switched by the muxing block. When this bit is set to logic 1, normal switching of the J0/Z0 bytes is enabled.

CMPSEL

The connection memory page select bit (CMPSEL) bit provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the OCMP input signal to determine which connection memory page is currently active.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the RPTI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 093H RPTI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the RPTI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events

Register 0A0H RATI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	0
Bit 10	R/W	PAGE	0
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ODTSEL[3]	0
Bit 6	R/W	ODTSEL[2]	0
Bit 5	R/W	ODTSEL[1]	0
Bit 4	R/W	ODTSEL[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	ODSEL[1]	0
Bit 0	R/W	ODSEL[0]	0

This register provides the Outgoing TelecomBus data stream number, the time-slot number, and the page number used to access the connection memory pages in the RATI block. Writing to this register triggers an indirect register access.

ODSEL[1:0]

The Outgoing TelecomBus data stream selection bits (ODSEL[1:0]) select which Outgoing TelecomBus data stream (OD[*X*][7:0]) is accessed by the current indirect transfer. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0].

ODSEL[1:0]	Outgoing TelecomBus Data Stream
00	OD[1][7:0]
01	OD[2][7:0]
10	OD[3][7:0]
11	OD[4][7:0]

ODTSEL[3:0]

The indirect Outgoing TelecomBus time-slot bits (ODTSEL[3:0]) indicate the STS-1/STM-0 time-slot within the Outgoing TelecomBus data stream selected by IODSEL[1:0] that is accessed in the current indirect access. Data from time-slot IODTSEL[3:0] of internal outgoing data stream IODSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are 'b0001 to 'b1100.

ODTSEL[3:0]	STS-1/STM-0 time-slot #
0000	Invalid time-slot
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid time-slot

PAGE

The connection memory page select bit (PAGE) selects the connection memory page to be accessed in the current indirect transfer. When PAGE is set high, page 1 is selected. When Page is set low, PAGE 0 is selected.

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the RATI Indirect Data register. Writing a logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the RATI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the RATI Indirect Data Register or when another write access can be initiated.

Register 0A1H RATI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	RATSEN	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	ATSEL[3]	0
Bit 6	R/W	ATSEL[2]	0
Bit 5	R/W	ATSEL[1]	0
Bit 4	R/W	ATSEL[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ALSEL[1]	0
Bit 0	R/W	ALSEL[0]	0

This register contains the data read from the connection memory pages after an indirect read operation or the to be data written to the connection memory pages in an indirect write operation to the RPTI block.

ALSEL[1:0]

The auxiliary link select bits (ALSEL[1:0]) report the receive auxiliary serial TelecomBus link number read after an indirect read operation has completed. The receive auxiliary serial TelecomBus link number to be written to the connect memory pages must be set up in this register before triggering a write. ALSEL[1:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot ATSEL[3:0] of the receive auxiliary serial TelecomBus link ALSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]

ALSEL[1:0]	Receive Auxiliary Serial TelecomBus Link
00	RPAUX[1]/RNAUX[1]
01	RPAUX[2]/RNAUX[2]
10	RPAUX[3]/RNAUX[3]
11	RPAUX[4]/RNAUX[4]

Reserved

The reserved bits (Reserved) must be set to low for correct operation of the TBS.

ATSEL[3:0]

The auxiliary time-slot select bits (ATSEL[3:0]) report the time-slot number read after an indirect read operation has completed. The time-slot number to be written to the control pages must be set up in this register before triggering a write. ATSEL[3:0] reflects the last value read or written until the completion of a subsequent indirect read operation. Data from time-slot ATSEL[3:0] of receive auxiliary serial TelecomBus link ALSEL[1:0] is transferred to time-slot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. Valid time-slot values are ‘b0001 to ‘b1100.

ATSEL[3:0]	STS-1/STM-0 Time-slot #
0000	Invalid
0001-1100	Time-slot #1 to time-slot #12
1101-1111	Invalid

RATSEN

The receive auxiliary timeslot enable bit (RATSEN) reports the timeslot enable value read after an indirect read operation has completed. The timeslot enable value to be written to the connection memory pages must be set up in this register before triggering a write. RATSEN reflects the last value read or written until the completion of a subsequent indirect read operation. When RATSEN is set high, the data from timeslot ATSEL[3:0] of the receive auxiliary serial TelecomBus link ALSEL[1:0] is transferred to timeslot ODTSEL[3:0] of Outgoing TelecomBus data stream ODSEL[1:0]. For each timeslot, one and only one of RWTSEN, RPTSEN, RATSEN must be set high.

Register 0A2H RATI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ACTIVE	X
Bit 2	R/W	CMPSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

This register configures the operation of the RATI block.

COAPE

The change of active connection memory page interrupt enable bit (COAPE) controls the assertion of the change of active connection memory page interrupts by the RATI. When the COAPE bit is high, an interrupt is generated when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. Interrupts due to changes in active connection memory page are masked when COAPE is set low.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering (switching) of the J0/Z0 bytes. This configuration bit only has an effect when the RATI is in the user configured timeslot mapping mode – if the RATI is in bypass mode then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not switched by the muxing block. When this bit is set to logic 1, normal switching of the J0/Z0 bytes is enabled.

CMPSEL

The connection memory page select bit (CMPSEL) bit provides software control of the active connection memory page. CMPSEL is exclusive-ORed with the OCMP input signal to determine which connection memory page is currently active.

ACTIVE

The active connection memory page status bit (ACTIVE) indicates which connection memory page is currently active in the RATI. ACTIVE is set low when page 0 is active. ACTIVE is set high when page 1 is active.

Register 0A3H RATI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COAPI	X

This register is used to report and acknowledge the status of the change of active connection memory page interrupts in the RATI block.

COAPI

The change of active connection memory page interrupt status bit (COAPI) report the status of the change of active page interrupts. COAPI is set high when the active connection memory page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register. COAPI remains valid when interrupts are not enabled (COAPE set low) and may be polled to detect change of active connection memory page events.

Register 100h ITPP #1 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the ITPP #1 block. Writing to this register triggers an indirect register access.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = '0') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page
0011	B1/E1 value page
0100	Monitor error count page
0101	Received B1 and E1

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	B1/E1 value page

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 101h ITPP #1 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 101h (IADDR = 0h) ITPP #1 Monitor STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 100h).

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 100h (ITPP #1 Indirect Address). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

Reserved

The reserved bit must be set low for correct operation of the TBS.

INV_PRBS

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master ITPP only.

B1E1_ENA

When high this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored and the latest B1 and E1 bytes are stored in the Monitor Received B1/E1 bytes register.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Register 101h (IADDR = 1h) ITPP #1 Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 100h).

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 101h (IADDR = 2h) ITPP #1 Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 100h).

PRBS[7:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 101h (IADDR = 3h) ITPP #1 Monitor B1/E1 Expected value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 3h (IADDR[3:0] is “3h” in register 100h).

B1[7:0]

When enabled, the monitoring of the B1 byte in the incoming SONET/SDH frame is a simple comparison to the value in the B1[7:0] register. The complement of this value is used for the monitoring of the E1 byte.

Register 101h (IADDR = 4h) ITPP #1 Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 100h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by a write to register 0x10C or by writing to register 0x002. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value. Note that the monitor requires 3 byte errors before it loses synchronization. Once synchronization is lost, errors cease to be counted. Up to 2 extra byte errors may be counted however if these errors are already in the monitor’s pipeline when the monitor declares a loss of synchronization.

Register 101h (IADDR = 5h) ITPP #1 Monitor Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 5h (IADDR[3:0] is “5h” in register 100h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time an E1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

Register 101h (IADDR = 8h) ITPP #1 Generator STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	IP8E_PRBS_ENA	0
Bit 12	R/W	ID8E_PRBS_ENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	X
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 100h).

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

B1E1_ENA

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are replaced in the frame, else they go through the ITPP unaltered.

NOTE:

1. B1/E1 byte insertion is independent of PRBS insertion for the ID8E path but not for the IP8E path. B1/E1 insertion will only occur on the IP8E path if B1E1_ENA and IP8E_PRBS_ENA are both set to 1. For the ID8E path, B1/E1 insertion will occur when B1E1_ENA is set to 1, regardless of the ID8E_PRBS_ENA setting.

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

Reserved

The reserved bits (Reserved) must be set low for correct operation of the TBS.

ID8E_PRBS_ENA

This bit specifies if PRBS is to be inserted in the path through ID8E #1. If ID8E_PRBS_ENA is high patterns are generated in the SONET/SDH frame to ID8E #1, else no pattern is generated and the unmodified SONET/SDH input frame is passed to ID8E #1. Under normal operation, ID8E_PRBS_ENA should always be set to 0.

IP8E_PRBS_ENA

This bit specifies if PRBS is to be inserted in the path through IP8E #1. If IP8E_PRBS_ENA is high patterns are generated in the SONET/SDH frame to IP8E #1, else no pattern is generated and the unmodified SONET/SDH input frame is passed to IP8E #1. Under normal operation where PRBS is being inserted into STS/SDH payloads, IP8E_PRBS_ENA will be set to 1.

Register 101h (IADDR = 9h) ITPP #1 Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 100h).

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 101h (IADDR = Ah) ITPP #1 Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 100h).

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 101h (IADDR = Bh): ITPP #1 Generator B1/E1 Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the ITPP #1 Indirect Data register (Register 101h) when accessing Indirect Address Bh (IADDR[3:0] is “Bh” in register 100h).

B1[7:0]

When enabled, the value in this register is inserted in the B1byte position in the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register 102h ITPP #1 Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS generator section.

GEN_STS3C[0]

The STS-3c/VC-4 payload configuration (GEN_STS3C[0]) bit selects the payload configuration. When GEN_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[0] register bit.

GEN_STS3C[1]

The STS-3c/VC-4 payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[1] register bit.

GEN_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[2] register bit.

GEN_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[3] register bit.

GEN_MSSLEN [1:0]

The generator master/slave configuration (GEN_MSSLEN [1:0]) bits selects the payload configuration to be processed by ITPP #1 in conjunction with other ITPP blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	ITPP Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

Reserved

The Reserved bit must be set low for correct operation of the TBS.

GEN_STS12C

The STS-12c/VC-4-4c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[3:0] register bit. The GEN_STS12C register bit has precedence over the GEN_STS3C[3:0] register bit.

GEN_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenated master payload.

Table 6 Register configuration to select payload type for ITPP Generator and Monitor

Mode	Payload	GEN/MON STS12C	GEN/MON STS12CSL	GEN/MON MSSLEN[1:0]
Master	Rates lower than STS-12c (specified with STS3C[3:0])	0	0	00
Master	STS-12c	1	0	00
Master	STS-24c	1	0	01
	STS-36c	1	0	10
	STS-48c	1	0	11
Slave	STS-24c	1	1	01
	STS-36c	1	1	10
	STS-48c	1	1	11

All other configurations are invalid.

Register 103h ITPP #1 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

MON_MSSLEN [1:0]

The monitor master/slave configuration (MON_MSSLEN [1:0]) bits selects the payload configuration to be processed by ITPP #1 in conjunction with other ITPP blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	ITPP Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

MON_MSSLEN[1:0] must be set to “00” for rates STS-12c and below.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

For details on Configuration registers see Table 6.

Register 104h ITPP #1 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI bit is set high when the monitor is in the synchronized state and an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE and is cleared after being read.

Register 105h ITPP #1 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt.

Register 106h ITPP #1 Monitor B1/E1 Byte Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

This register reports B1/E1 byte mismatch interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_B1E1I

The Monitor B1/E1Byte Mismatch Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when a mismatch has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor detects a mismatch on either the B1 or E1 bytes in the STS-1 path **x**. This bit is independent of MON**x**_B1E1E, and is cleared after it has been read, but if the mismatch condition persists the bit will be set high again at the next comparison.

Register 107h ITPP#1 Monitor B1/E1 Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

This register enables the assertion of B1/E1 byte monitor mismatch status interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_B1E1E

The Monitor B1/E1 Byte Mismatch Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high it allows the B1/E1 Byte Mismatch Interrupt to generate an external interrupt.

Register 109h ITPP#1 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in the PRBS monitor will set MONxSYNCI high. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 10Ah ITPP#1 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high a change in the synchronization state of the monitor in STS-1 path **x** will generate an interrupt.

Register 10Bh ITPP#1 Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high and the monitor is enabled, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low and the monitor is enabled, the monitor is NOT in synchronization for the STS-1 Path **x**. If the monitor is disabled, the MON**x**_SYNCV bits will retain their present values, regardless of the state of received PRBS streams, until the monitor is re-enabled. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 10Ch ITPP #1 Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 112H ID8E #1 Time-slot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the ID8E #1 block.

TMODE1[1:0] –TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the ID8E #1 block. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[1][7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST Mode
0	1	HPT Mode
1	0	Reserved
1	1	Reserved

Register 113H ID8E #1 Time-slot Configuration #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the ID8E #1 block.

TMODE9[1:0] –TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the ID8E #1 block. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[1][7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST Mode
0	1	HPT Mode
1	0	Reserved
1	1	Reserved

Register 122H IP8E #1 Time-slot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the IP8E #1 block.

TMODE1[1:0] –TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the IP8E #1 block. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[1][7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST Mode
0	1	HPT Mode
1	0	Reserved
1	1	Reserved

Register 123H IP8E #1 Time-slot Configuration #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the IP8E #1 block.

TMODE9[1:0] –TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the IP8E #1 block. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[1][7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST Mode
0	1	HPT Mode
1	0	Reserved
1	1	Reserved

Register 130H TWDE #1 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TWDE #1 block.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the working transmit serial data stream #1 (TPWRK[1]/TNWRK[1]). When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to a logic low or a logic high when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the working transmit serial data stream #1 (TPWRK[1]/TNWRK[1]) for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used as the transmitted character. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event when FIFOERRE is set high. No interrupt is generated when FIFOERRE is set low.

Reserved

The reserved bits (Reserved) must be set low for the correct operation of the TBS.

Register 131H TWDE #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports and acknowledges interrupts in the TWDE #1 block.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set high on a FIFO overrun/underrun error. FIFOERRI is set low following a read access to this register. Note: the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

Register 134H TWDE #1 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the transmit serial data stream serviced by the TWDE #1 block.

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is inserted into the working transmit serial data stream #1 (TPWRK[1]/TNWRK[1]) when the TPINS bit is set high. ALL transmitted characters are replaced by the test pattern stored in TP[9:0]. TP[9:0] has no effect when TPINS is set low.

Register 135H TWDE #1 Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Register 135H controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the TXLV_ENB and the PISO_ENB bits should both be set high.

PISO_ENB

Driving this bit high will disable the PISO circuitry.

TXLV_ENB

Driving this bit high will disable the analog transmitter circuitry.

Reserved

The reserved bits should not be altered.

Register 140H TPDE #1 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TPDE #1 block.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the protection transmit serial data stream #1 (TPPROT[1]/TNPROT[1]). When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to a logic low or a logic high when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the protection transmit serial data stream #1 (TPPROT[1]/TNPROT[1]) for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to transmitted characters. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event when FIFOERRE is set high. No interrupt is generated when FIFOERRE is set low.

Reserved

The reserved bits (Reserved) must be set low for the correct operation of the TBS.

Register 141H TPDE #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports and acknowledges interrupts in the TPDE #1 block.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set high on a FIFO overrun/underrun error. FIFOERRI is set low following a read access to this register. Note: the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

Register 144H TPDE #1 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the transmit serial data stream serviced by the TPDE #1 block.

TP[9:0]:

The Test Pattern registers (TP[9:0]) contains the test pattern that is inserted into the protection transmit serial data stream #1 (TPPROT[1]/TNPROT[1]) when TPINS bit is set high. ALL transmitted characters are replaced by the test pattern stored in TP[9:0]. TP[9:0] has no effect when TPINS is set low.

Register 145H TPDE #1 Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Register 145H controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the TXLV_ENB and the PISO_ENB bits should both be set high.

PISO_ENB

Driving this bit high will disable the PISO circuitry.

TXLV_ENB

Driving this bit high will disable the analog transmitter circuitry.

Reserved

The reserved bits should not be altered.

Register 150H TADE #1 Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TADE #1 block.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the auxiliary transmit serial data stream #1 (TPAUX[1]/TNAUX[1]). When this bit is set high, the encoded data is continuously inverted to generate line code violations. The inverted data will represent both valid and invalid 8B/10B characters as not all 8B/10B characters have positive running disparity and negative running disparity characters simply the inverse of each other. Note that TelecomBus control characters are not affected by the DLCV bit but are passed unaltered.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to a logic low or a logic high when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the auxiliary transmit serial data stream #1 (TPAUX[1]/TNAUX[1]) for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to transmitted characters. When TPINS is set low, no test patterns are generated.

FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event when FIFOERRE is set high. No interrupt is generated when FIFOERRE is set low.

Reserved

The reserved bits (Reserved) must be set low for the correct operation of the TBS.

Register 151H TADE #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports and acknowledges interrupts in the TADE #1 block.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set high on a FIFO overrun/underrun error. FIFOERRI is set low following a read access to this register. Note: the default value would only be seen immediately after a digital reset performed while the CSU is running and locked. If the CSU is disabled, or is in the process of locking, FIFO errors will be generated continually and a “1” value will appear in FIFOERRI bit almost immediately.

Register 154H TADE #1 Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the transmit serial data stream serviced by the TADE #1 block.

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is inserted into the auxiliary transmit serial data stream #1 (TPAUX[1]/TNAUX[1]) when TPINS bit is set high. ALL transmitted characters are replaced by the test pattern stored in TP[9:0]. TP[9:0] has no effect when TPINS is set low.

Register 155H TADE #1 Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

Register 155H controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the TXLV_ENB and the PISO_ENB bits should both be set high.

PISO_ENB

Driving this bit high will disable the PISO circuitry.

TXLV_ENB

Driving this bit high will disable the analog transmitter circuitry.

Reserved

The reserved bits should not be altered.

Register 160H RW8D #1 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	0
Bit 2	R	OCAV	0
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RW8D #1 block.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUOE is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set to logic 1 to force high-order AIS signals in the data-stream, when the RW8D is in the out-of-frame-alignment state. No insertion into the data stream is done when OFAAIS is set to logic 0.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

Register 161H RW8D #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	0
Bit 0		Unused	0

This register reports interrupt status due to changes of character alignment state, changes of frame alignment state, detect line code violations, and FIFO error events in the RW8D #1 block.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the datastream. LCVI is set high when a line code violation event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events. Note that an uninterrupted stream of line code violations will produce a single LCVI event as it is the receipt of an invalid character following a valid character that produces the interrupt.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events. Note that the FUOI provides no information about framing. Framing information is contained in the OFAV bit only.

Register 162H RW8D #1 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	0
Bit 14	R	LCV[14]	0
Bit 13	R	LCV[13]	0
Bit 12	R	LCV[12]	0
Bit 11	R	LCV[11]	0
Bit 10	R	LCV[10]	0
Bit 9	R	LCV[9]	0
Bit 8	R	LCV[8]	0
Bit 7	R	LCV[7]	0
Bit 6	R	LCV[6]	0
Bit 5	R	LCV[5]	0
Bit 4	R	LCV[4]	0
Bit 3	R	LCV[3]	0
Bit 2	R	LCV[2]	0
Bit 1	R	LCV[1]	0
Bit 0	R	LCV[0]	0

This register reports the number of line code violations in the previous accumulation period in the RW8D #1 block.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing to TBS Master Input Signal Activity, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 100 ns and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 163H RW8D #1 Analog Control #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the DRU_ENB and the RX_ENB bits should both be set high.

NOTE:

1. THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE ANALOG CIRCUITRY. FOR DISABLING THIS RECEIVER, THE REGISTER SHOULD BE SET TO FC34H.

DRU_ENB

Setting the DRU_ENB bit high disables the DRU.

RX_ENB

Setting the RX_ENB bit disables the LVDS receiver.

Reserved

The reserved bits (Reserved) should not be altered unless this is specifically advised.

Register 170H RP8D #1 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	0
Bit 2	R	OCAV	0
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RP8D #1 block.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUOE is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set to logic 1 to force high-order AIS signals in the data-stream, when the RP8D is in the out-of-frame-alignment state. No insertion into the data stream is done when OFAAIS is set to logic 0.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

Register 171H RP8D #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	0
Bit 0		Unused	X

This register reports interrupt status due to changes of character alignment state, changes of frame alignment state, detect line code violations, and FIFO error events in the RP8D #1 block.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events. Note that an uninterrupted stream of line code violations will produce a single LCVI event as it is the receipt of an invalid character following a valid character that produces the interrupt.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events. Note that the FUOI provides no information about framing. Framing information is contained in the OFAV bit only.

Register 172H RP8D #1 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	0
Bit 14	R	LCV[14]	0
Bit 13	R	LCV[13]	0
Bit 12	R	LCV[12]	0
Bit 11	R	LCV[11]	0
Bit 10	R	LCV[10]	0
Bit 9	R	LCV[9]	0
Bit 8	R	LCV[8]	0
Bit 7	R	LCV[7]	0
Bit 6	R	LCV[6]	0
Bit 5	R	LCV[5]	0
Bit 4	R	LCV[4]	0
Bit 3	R	LCV[3]	0
Bit 2	R	LCV[2]	0
Bit 1	R	LCV[1]	0
Bit 0	R	LCV[0]	0

This register reports the number of line code violations in the previous accumulation period in the RP8D #1 block.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing to TBS Master Input Signal Activity, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 100 ns and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 173H RP8D #1 Analog Control #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the DRU_ENB and the RX_ENB bits should both be set high.

NOTE:

1. THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE ANALOG CIRCUITRY. FOR DISABLING THIS RECEIVER, THE REGISTER SHOULD BE SET TO FC34H.

DRU_ENB

Setting the DRU_ENB bit high disables the DRU.

RX_ENB

Setting the RX_ENB bit disables the LVDS receiver.

Reserved

The reserved bits (Reserved) should not be altered unless this is specifically advised.

Register 180H RA8D #1 Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	0
Bit 2	R	OCAV	0
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RA8D #1 block.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUOE is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set to logic 1 to force high-order AIS signals in the datastream, when the RA8D is in the out-of-frame-alignment state. No insertion into the data stream is done when OFAAIS is set to logic 0.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

Register 181H RA8D #1 Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	0
Bit 0		Unused	X

This register reports interrupt status due to changes of character alignment state, changes of frame alignment state, detect line code violations, and FIFO error events in the RA8D #1 block.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events. Note that an uninterrupted stream of line code violations will produce a single LCVI event as it is the receipt of an invalid character following a valid character that produces the interrupt.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events. Note that the FUOI provides no information about framing. Framing information is contained in the OFAV bit only.

Register 182H RA8D #1 Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	0
Bit 14	R	LCV[14]	0
Bit 13	R	LCV[13]	0
Bit 12	R	LCV[12]	0
Bit 11	R	LCV[11]	0
Bit 10	R	LCV[10]	0
Bit 9	R	LCV[9]	0
Bit 8	R	LCV[8]	0
Bit 7	R	LCV[7]	0
Bit 6	R	LCV[6]	0
Bit 5	R	LCV[5]	0
Bit 4	R	LCV[4]	0
Bit 3	R	LCV[3]	0
Bit 2	R	LCV[2]	0
Bit 1	R	LCV[1]	0
Bit 0	R	LCV[0]	0

This register reports the number of line code violations in the previous accumulation period in the RA8D #1 block.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing to TBS Master Input Signal Activity, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 100 ns and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 183H RA8D #1 Analog Control #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls analog circuitry. Normally users should not alter the contents of this register except when it is desirable to disable an unused analog link for power saving purposes. In that case, the DRU_ENB and the RX_ENB bits should both be set high.

NOTE:

1. THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE ANALOG CIRCUITRY. FOR DISABLING THIS RECEIVER, THE REGISTER SHOULD BE SET TO FC34H.

DRU_ENB

Setting the DRU_ENB bit high disables the DRU.

RX_ENB

Setting the RX_ENB bit disables the LVDS receiver.

Reserved

The reserved bits (Reserved) should not be altered unless this is specifically advised.

Register 190h RWPM #1 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the RWPM #1 block. Writing to this register triggers an indirect register access.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page
0011	B1/E1 value page
0100	Monitor error count page
0101	Received B1 and E1

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 191h RWPM #1 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transferred to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 191h (IADDR = 0h) RWPM #1 STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 190h).

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 0h (PRGM Indirect Addressing). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

Reserved

This bit must be set to 0 for correct operation of the TBS.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master PRGM only.

B1E1_ENA

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored and the latest B1 and E1 bytes are stored in the Monitor Received B1/E1 bytes register.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Register 191h (IADDR = 1h) RWPM #1 PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 190h).

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 191h (IADDR = 2h) RWPM #1 PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 190h).

PRBS[7:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 191h (IADDR = 3h) RWPM #1 B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 3h (IADDR[3:0] is “3h” in register 190h).

B1[7:0]

When enabled, the monitoring of the B1 byte in the incoming SONET/SDH frame is a simple comparison to the value in the B1[7:0] register. The complement of this value is used for the monitoring of the E1 byte.

Register 191h (IADDR = 4h) RWPM #1 Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 4h (IADDR[3:0] is "4h" in register 190h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by a write to register 0x19C or by writing to register 0x002. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value. Note that the monitor requires 3 byte errors before it loses synchronization. Once synchronization is lost, errors cease to be counted. Up to 2 extra byte errors may be counted however if these errors are already in the monitor's pipeline when the monitor declares a loss of synchronization.

Register 191h (IADDR = 5h) RWPM #1 Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

This register contains the definition of the RWPM #1 Indirect Data register (Register 191h) when accessing Indirect Address 5h (IADDR[3:0] is “5h” in register 190h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time an E1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

Register 193h RWPM #1 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

MON_MSSLEN [1:0]

The monitor master/slave configuration (MON_MSSLEN [1:0]) bits selects the payload configuration to be processed by RWPM #1 in conjunction with other RWPM blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	RWPM Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

MON_MSSLEN[1:0] must be set to “00” for rates STS-12c and below.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

For details on Configuration registers see Table 6.

Register 194h RWPM #1 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE, and is cleared after being read.

Register 195h RWPM #1 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

Register 196h RWPM #1 Monitor B1/E1 Byte Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

This register reports B1/E1 byte mismatch interrupts for all the time-slots received on the first receive working serial data link (RPWRK[1]/RNWRK[1])..

MON**x**_B1E1I

The Monitor B1/E1Byte Mismatch Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when a mismatch has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor detects a mismatch on either the B1 or E1 bytes in the STS-1 path **x**. This bit is independent of MON**x**_B1E1E, and is cleared after it has been read, but if the mismatch condition persists the bit will be set high again at the next comparison.

Register 197h RWPM#1 Monitor B1/E1 Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

This register enables the assertion of B1/E1 byte monitor mismatch status interrupts for all the time-slots received on the first receive working serial data link (RPWRK[1]/RNWRK[1]).

MON**x**_B1E1E

The Monitor B1/E1 Byte Mismatch Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high it allows the B1/E1 Byte Mismatch Interrupt to generate an external interrupt.

Register 199h RWPM#1 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in the PRBS monitor will set MONxSYNCI high. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 19Ah RWPM#1 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. Whenever a change occurs in the synchronization state of the monitor on the STS-1 path **x**, and MON**x**_SYNCE is set high, an interrupt is generated on INT.

Register 19Bh RWPM#1 Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high and the monitor is enabled, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low and the monitor is enabled, the monitor is NOT in synchronization for the STS-1 Path **x**. If the monitor is disabled, the MON**x**_SYNCV bits will retain their present values, regardless of the state of received PRBS streams, until the monitor is re-enabled. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 19Ch RWPM #1 Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 1A0h RPPM #1 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the RPPM #1 block. Writing to this register triggers an indirect register access.

Note: Addresses 1A0 – 1AF and addresses 1C0 – 1CF map to the same physical registers. Values written to address 1A0 will also appear at address 1C0 etc. Indirect accesses in either the 1A0/1A1 or 1C0/1C1 address range must be completed before beginning another indirect access in either the 1A0/1A1 or 1C0/1C1 address range.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page
0011	B1/E1 value page
0100	Monitor error count page
0101	Received B1 and E1

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register. Note that because of common logic, an indirect access to the RPPM #1 or the OTPG #1 will cause this busy bit to go high.

Register 1A1h RPPM #1 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

Note: Addresses 1A0 – 1AF and addresses 1C0 – 1CF map to the same physical registers. Values written to address 1A0 will also appear at address 1C0 etc. Indirect accesses in either the 1A0/1A1 or 1C0/1C1 address range must be completed before beginning another indirect access in either the 1A0/1A1 or 1C0/1C1 address range.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 1A1h (IADDR = 0h) RPPM #1 STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 0h (IADDR[3:0] is "0h" in Register 1A0h).

MON_ENA

Monitor Enable register bit enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 0h (PRGM Indirect Addressing). If MON_ENA is set to '1', a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

Reserved

This bit must be set to 0 for proper operation of the TBS.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master PRGM only.

B1E1_ENA

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored and the latest B1 and E1 bytes are stored in the Monitor Received B1/E1 bytes register.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Register 1A1h (IADDR = 1h) RPPM #1 PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in Register 1A0h).

PRBS[22:7]

The PRBS[22:7] registers are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1A1h (IADDR = 2h) RPPM #1 PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in Register 1A0h).

PRBS[7:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1A1h (IADDR = 3h) RPPM #1 B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 3h (IADDR[3:0] is "3h" in Register 1A0h).

B1[7:0]

When enabled the monitoring of the B1 byte in the incoming SONET/SDH frame is a simple comparison to the value in the B1[7:0] register. The complement of this value is used for the monitoring of the E1 byte.

Register 1A1h (IADDR = 4h) RPPM #1 Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 4h (IADDR[3:0] is "4h" in Register 1A0h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by a write to register 0x1AC or by writing to register 0x002. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value. Note that the monitor requires 3 byte errors before it loses synchronization. Once synchronization is lost, errors cease to be counted. Up to 2 extra byte errors may be counted however if these errors are already in the monitor's pipeline when the monitor declares a loss of synchronization.

Register 1A1h (IADDR = 5h) RPPM #1 Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

This register contains the definition of the RPPM #1 Indirect Data register (Register 1A1h) when accessing Indirect Address 5h (IADDR[3:0] is "5h" in Register 1A0h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time an E1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

Register 1A3h RPPM #1 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

MON_MSSLEN [1:0]

The monitor master/slave configuration (MON_MSSLEN [1:0]) bits selects the payload configuration to be processed by RPPM #1 in conjunction with other RPPM blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	RPPM Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

MON_MSSLEN[1:0] must be set to “00” for rates STS-12c and below.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

For details on Configuration registers see Table 6.

Register 1A4h RPPM #1 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE and is cleared after being read.

Register 1A5h RPPM #1 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

Register 1A6h RPPM #1 Monitor B1/E1 Byte Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

This register reports B1/E1 byte mismatch interrupts for all the time-slots in the received on the first receive protection serial data link (RPPROT[1]/RNPROT[1]).

MON**x**_B1E1I

The Monitor B1/E1Byte Mismatch Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when a mismatch has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor detects a mismatch on either the B1 or E1 bytes in the STS-1 path **x**. This bit is independent of MON**x**_B1E1E, and is cleared after it has been read, but if the mismatch condition persists the bit will be set high again at the next comparison.

Register 1A7h RPPM#1 Monitor B1/E1 Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

This register enables the assertion of B1/E1 byte monitor mismatch status interrupts for all the time-slots received on the first receive protection serial data link (RPPROT[1]/RNPROT[1]).

MON**x**_B1E1E

The Monitor B1/E1 Byte Mismatch Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high it allows the B1/E1 Byte Mismatch Interrupt to generate an external interrupt.

Register 1A9h RPPM#1 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in the PRBS monitor will set MONxSYNCI high. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 1AAh RPPM#1 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1 path **x**, generates an interrupt on INT.

Register 1ABh RPPM#1 Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high and the monitor is enabled, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low and the monitor is enabled, the monitor is NOT in synchronization for the STS-1 Path **x**. If the monitor is disabled, the MON**x**_SYNCV bits will retain their present values, regardless of the state of received PRBS streams, until the monitor is re-enabled. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 1ACh RPPM #1 Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 1B0h RAPM #1 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the RAPM #1 block. Writing to this register triggers an indirect register access.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page
0011	B1/E1 value page
0100	Monitor error count page
0101	Received B1 and E1

Reserved

The Reserved bit must be set to logic 0 to access the RAPM indirect registers.

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

Register 1B1h RAPM #1 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 1B1h (IADDR = 0h) RAPM #1 STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in Register 1B0h).

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 0h (PRGM Indirect Addressing). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

Reserved

This register must be set to 0 for proper operation of the TBS.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When set high the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master PRGM only.

B1E1_ENA

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored and the latest B1 and E1 bytes are stored in the Monitor Received B1/E1 bytes register.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Register 1B1h (IADDR = 1h) RAPM #1 PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in Register 1B0h).

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1B1h (IADDR = 2h) RAPM #1 PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in Register 1B0h).

PRBS[7:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1B1h (IADDR = 3h) RAPM #1 B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 3h (IADDR[3:0] is "3h" in Register 1B0h).

B1[7:0]

When enabled, the monitoring of the B1 byte in the incoming SONET/SDH frame is a simple comparison to the value in the B1[7:0] register. The complement of this value is used for the monitoring of the E1 byte.

Register 1B1h (IADDR = 4h) RAPM #1 Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 4h (IADDR[3:0] is "4h" in Register 1B0h).

ERR_CNT[15:0]

The ERR_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by a write to register 0x1BC or by writing to register 0x002. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value. Note that the monitor requires 3 byte errors before it loses synchronization. Once synchronization is lost, errors cease to be counted. Up to 2 extra byte errors may be counted however if these errors are already in the monitor's pipeline when the monitor declares a loss of synchronization.

Register 1B1h (IADDR = 5h) RAPM #1 Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

This register contains the definition of the RAPM #1 Indirect Data register (Register 1B1h) when accessing Indirect Address 5h (IADDR[3:0] is "5h" in Register 1B0h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time an E1 byte is received, it is copied in this register when B1E1 monitoring is enabled.

Register 1B3h RAPM #1 Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS monitor section.

MON_STS3C[0]

The STS-3c/VC-4 payload configuration (MON_STS3C[0]) bit selects the payload configuration. When MON_STS3C[0] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[0] register bit.

MON_STS3C[1]

The STS-3c/VC-4 payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[1] register bit.

MON_STS3C[2]

The STS-3c/VC-4 payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The MON_STS12C register bit has precedence over the MON_STS3C[2] register bit.

MON_STS3C[4]

The STS-3c/VC-4 payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The MON_STS12C register bit has precedence over the MON_STS3C[3] register bit.

Reserved

The Reserved bits must be set low for correct operation of the TBS.

MON_MSSLEN [1:0]

The monitor master/slave configuration (MON_MSSLEN [1:0]) bits selects the payload configuration to be processed by RAPM #1 in conjunction with other RAPM blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	RAPM Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

MON_MSSLEN[1:0] must be set to “00” for rates STS-12c and below.

MON_STS12C

The STS-12c/VC-4-4c payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit. The MON_STS12C register bit has precedence over the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenate master payload.

For details on Configuration registers see Table 6.

Register 1B4h RAPM #1 Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE and is cleared after being read.

Register 1B5h RAPM #1 Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

Register 1B6h RAPM #1 Monitor B1/E1 Byte Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

This register reports B1/E1 byte mismatch interrupts for all the time-slots received on the first receive auxiliary serial data link (RPAUX[1]/RNAUX[1]).

MON**x**_B1E1I

The Monitor B1/E1Byte Mismatch Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when a mismatch has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor detects a mismatch on either the B1 or E1 bytes in the STS-1 path **x**. This bit is independent of MON**x**_B1E1E, and is cleared after it has been read, but if the mismatch condition persists the bit will be set high again at the next comparison.

Register 1B7h RAPM#1 Monitor B1/E1 Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

This register enables the assertion of B1/E1 byte monitor mismatch status interrupts for all the time-slots received on the first receive auxiliary serial data link (RPAUX[1]/RNAUX[1]).

MON**x**_B1E1E

The Monitor B1/E1 Byte Mismatch Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high it allows the B1/E1 Byte Mismatch Interrupt to generate an external interrupt.

Register 1B9h RAPM#1 Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE and is cleared after it's been read. For concatenated payloads, only the STS-1 path state machine that first detects the change in Synchronization Status in the PRBS monitor will set MONxSYNCI high. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 1BAh RAPM#1 Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. Whenever a change occurs in the synchronization state of the monitor on the STS-1 path **x**, and MON**x**_SYNCE is set high, an interrupt is generated on INT.

Register 1BBh RAPM#1 Monitor Synchronization State

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Incoming TelecomBus ID[1][7:0].

MON**x**_SYNCV

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high and the monitor is enabled, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low and the monitor is enabled, the monitor is NOT in synchronization for the STS-1 Path **x**. If the monitor is disabled, the MON**x**_SYNCV bits will retain their present values, regardless of the state of received PRBS streams, until the monitor is re-enabled. It is important to note that the monitor can falsely synchronize to an all zero data pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 data pattern. It is therefore recommended that users poll the monitor's PRBS accumulator's value after synchronization has been declared, to confirm that the value is neither all 1s nor all 0s.

Register 1BCh RAPM #1 Performance Counters Transfer Trigger

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

TIP

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 1C0h OTPG #1 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the OTPG #1 block. Writing to this register triggers an indirect register access.

Note: Addresses 1A0 – 1AF and addresses 1C0 – 1CF map to the same physical registers. Values written to address 1A0 will also appear at address 1C0 etc. Indirect accesses in either the 1A0/1A1 or 1C0/1C1 address range must be completed before beginning another indirect access in either the 1A0/1A1 or 1C0/1C1 address range.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

IADDR[3:0]

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Four pages are defined for the generator: the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	B1/E1 value page

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register. Note that because of common logic, an indirect access to the RPPM #1 or the OTPG #1 will cause this busy bit to go high.

Register 1C1h OTPG #1 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

Note: Addresses 1A0 – 1AF and addresses 1C0 – 1CF map to the same physical registers. Values written to address 1A0 will also appear at address 1C0 etc. Indirect accesses in either the 1A0/1A1 or 1C0/1C1 address range must be completed before beginning another indirect access in either the 1A0/1A1 or 1C0/1C1 address range.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

Register 1C1h (IADDR = 8h) OTPG #1 STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Reserved	X
Bit 12	R/W	PRBS_ENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OCOUT[1]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

This register contains the definition of the OTPG #1 Indirect Data register (Register 1C1h) when accessing Indirect Address 0h (IADDR[3:0] is "8h" in Register 1C0h).

Reserved

The reserved bits must be set to 0 for proper operation of the TBS.

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete. A read operation will always result in a logic '0'.

B1E1_ENA

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are replaced in the frame, else they go through the PRGM unaltered. The B1/E1 byte insertion is independent of PRBS insertion (PRBS_ENA).

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

OCOUT[1]

The General Purpose Output signal is a user programmable value on a per STS-1 basis, that is output at the beginning of all generated frame (first A1 byte of the STS-N frame). It stays stable over the frame, and if a new value is programmed, it will be output on the next A1 byte.

PRBS_ENA

This bit specifies if PRBS is to be inserted in the outgoing TelecomBus channel #1. If PRBS_ENA is high, patterns are generated and inserted into the SONET/SDH frame in channel #1 of the outgoing TelecomBus, else no pattern is generated and the unmodified SONET/SDH input frame is transmitted on outgoing TelecomBus channel #1.

Register 1C1h (IADDR = 9h) OTPG #1 PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the OTPG #1 Indirect Data register (Register 1C1h) when accessing Indirect Address 1h (IADDR[3:0] is “9h” in Register 1C0h).

PRBS[22:7]

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1C1h (IADDR = Ah) OTPG #1 PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the OTPG #1 Indirect Data register (Register 1C1h) when accessing Indirect Address 2h (IADDR[3:0] is “Ah” in Register 1C0h).

PRBS[6:0]

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Register 1C1h (IADDR = Bh) OTPG #1 B1/E1 Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

This register contains the definition of the OTPG #1 Indirect Data register (Register 1C1h) when accessing Indirect Address 3h (IADDR[3:0] is “Bh” in Register 1C0h).

B1[7:0]

When enabled the value in this register is inserted in the B1byte position in the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register 1C2h OTPG #1 Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming TelecomBus ID[1][7:0] for processing by the PRBS generator section.

GEN_STS3C[0]

The STS-3c/VC-4 payload configuration (GEN_STS3C[0]) bit selects the payload configuration. When GEN_STS3C[0] is set to logic 1, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN_STS3C[0] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[0] register bit.

GEN_STS3C[1]

The STS-3c/VC-4 payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[1] register bit.

GEN_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[2] register bit.

GEN_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1/VC-3 payloads. The GEN_STS12C register bit has precedence over the GEN_STS3C[3] register bit.

GEN_MSSLEN [1:0]

The generator master/slave configuration (GEN_MSSLEN [1:0]) bits selects the payload configuration to be processed by OTPG #1 in conjunction with other OTPG blocks in the TBS.

GEN_MSSLEN [1:0]	Payload Configuration	OTPG Used
00	STS-12c/VC-4-4c and below	#1
01	STS-24c/VC-4-8c	#1, #2
10	STS-36c/VC-4-12c	#1, #2, #3
11	STS-48c/VC-4-16c	#1, #2, #3, #4

Reserved

The Reserved bit must be set low for correct operation of the TBS.

GEN_STS12C

The STS-12c/VC-4-4c payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[3:0] register bit. The GEN_STS12C register bit has precedence over the GEN_STS3C[3:0] register bit.

GEN_STS12CSL

The slave STS-12c/VC-4-4c payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the timeslots #1 to #12 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the timeslots #1 to # 12 are part of a concatenated master payload.

Table 7 Register configuration to select payload type for OTPG Generator

Mode	Payload	GEN STS12C	GEN STS12CSL	GEN MSSLEN[1:0]
Master	Rates lower than STS-12c (specified with STS3C[3:0])	0	0	00
Master	STS-12c	1	0	00
Master	STS-24c	1	0	01
	STS-36c	1	0	10
	STS-48c	1	0	11
Slave	STS-24c	1	1	01
	STS-36c	1	1	10
	STS-48c	1	1	11

All other configurations are invalid.

Register 200h, 300h, 400h: ITPP #2, #3, #4 Indirect Address

Refer to register 100h for the definition of these registers.

Register 201h, 301h, 401h: ITPP #2, #3, #4 Indirect Data

Refer to register 101h for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 1h): ITPP #2, #3, #4 Monitor PRBS[22:7] Accumulator

Refer to register 101h (IADDR = 1h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 2h): ITPP #2, #3, #4 Monitor PRBS[6:0] Accumulator

Refer to register 101h(IADDR = 2h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 3h): ITPP #2, #3, #4 Monitor B1/E1 value

Refer to register 101h (IADDR = 3h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 4h): ITPP #2, #3, #4 Monitor Error count

Refer to register 101h (IADDR = 4h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 5h): ITPP #2, #3, #4 Monitor Received B1/E1 bytes

Refer to register 101h (IADDR = 5h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 8h): ITPP #2, #3, #4 Generator STS-1 path Configuration

Refer to register 101h (IADDR = 8h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = 9h): ITPP #2, #3, #4 Generator PRBS[22:7] Accumulator

Refer to register 101h (IADDR = 9h) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = Ah): ITPP #2, #3, #4 Generator PRBS[6:0] Accumulator

Refer to register 101h (IADDR = Ah) for the definition of these registers.

Register 201h, 301h, 401h (IADDR = Bh): ITPP #2, #3, #4 Generator B1/E1 Value

Refer to register 101h (IADDR = Bh) for the definition of these registers.

Register 202h, 302h, 402h: ITPP #2, #3, #4 Generator Payload Configuration

Refer to register 102h for the definition of these registers.

Register 203h, 303h, 403h: ITPP #2, #3, #4 Monitor Payload Configuration

Refer to register 103h for the definition of these registers.

Register 204h, 304h, 404h: ITPP #2, #3, #4 Monitor Byte Error Interrupt Status

Refer to register 104h for the definition of these registers.

Register 205h, 305h, 405h: ITPP #2, #3, #4 Monitor Byte Error Interrupt Enable

Refer to register 105h for the definition of these registers.

Register 206h, 306h, 406h: ITPP #2, #3, #4 Monitor B1/E1 Byte Mismatch Interrupt Status

Refer to register 106h for the definition of these registers.

Register 207h, 307h, 407h: ITPP #2, #3, #4 Monitor B1/E1 Mismatch Interrupt Enable

Refer to register 107h for the definition of these registers.

Register 209h, 309h, 409h: ITPP #2, #3, #4 Monitor Synchronization Interrupt Status

Refer to register 109h for the definition of these registers.

Register 20Ah, 30Ah, 40Ah: ITPP #2, #3, #4 Monitor Synchronization Interrupt Enable

Refer to register 10Ah for the definition of these registers.

Register 20Bh, 30Bh, 40Bh: ITPP #2, #3, #4 Monitor Synchronization State

Refer to register 10Bh for the definition of these registers.

Register 20Ch, 30Ch, 40Ch: ITPP #, #3, #4 Performance Counters Transfer Trigger

Refer to register 10Ch for the definition of these registers.

Register 212h, 312h, 412h: ID8E #2, #3, #4 Time-slot Configuration #1

Refer to register 112h for the definition of these registers.

Register 213h, 313h, 413h: ID8E #2, #3, #4 Time-slot Configuration #2

Refer to register 113h for the definition of these registers.

Register 222h, 322h, 422h: IP8E #2, #3, #4 Time-slot Configuration #1

Refer to register 122h for the definition of these registers.

Register 223h, 323h, 423h: IP8E #2, #3, #4 Time-slot Configuration #2

Refer to register 123h for the definition of these registers.

Register 230h, 330h, 430h: TWDE #2, #3, #4 Control and Status

Refer to register 130h for the definition of these registers.

Register 231h, 321h, 431h: TWDE #2, #3, #4 Interrupt Status

Refer to register 131h for the definition of these registers.

Register 234h, 334h, 434h: TWDE #2, #3, #4 Test Pattern

Refer to register 134h for the definition of these registers.

Register 240h, 340h, 440h: TPDE #2, #3, #4 Control and Status

Refer to register 140h for the definition of these registers.

Register 241h, 341h, 441h: TPDE #2, #3, #4 Interrupt Status

Refer to register 141h for the definition of these registers.

Register 244h, 344h, 444h: TPDE #2, #3, #4 Test Pattern

Refer to register 144h for the definition of these registers.

Register 250h 350h, 450h: TADE #2, #3, #4 Control and Status

Refer to register 150h for the definition of these registers.

Register 251h, 351h, 451h: TADE #2, #3, #4 Interrupt Status

Refer to register 151h for the definition of these registers.

Register 254h, 354h, 454h: TADE #2, #3, #4 Test Pattern

Refer to register 154h for the definition of these registers.

Register 260h, 360h, 460h: RW8D #2, #3, #4 Control and Status

Refer to register 160h for the definition of these registers.

Register 261h, 361h, 461h: RW8D #2, #3, #4 Interrupt Status

Refer to register 161h for the definition of these registers.

Register 262h, 362h, 462h: RW8D #2, #3, #4 Line Code Violation Count

Refer to register 162h for the definition of these registers.

Register 270h, 370h, 470h: RP8D #2, #3, #4 Control and Status

Refer to register 170h for the definition of these registers.

Register 271h, 371h, 471h: RP8D #2, #3, #4 Interrupt Status

Refer to register 171h for the definition of these registers.

Register 272h, 372h, 472h: RP8D #2, #3, #4 Line Code Violation Count

Refer to register 172h for the definition of these registers.

Register 280h, 380h, 480h: RA8D #2, #3, #4 Control and Status

Refer to register 180h for the definition of these registers.

Register 281h, 381h, 481h: RA8D #2, #3, #4 Interrupt Status

Refer to register 181h for the definition of these registers.

Register 282h, 382h, 482h: RA8D #2, #3, #4 Line Code Violation Count

Refer to register 182h for the definition of these registers.

Register 290h, 390h, 490h: RWPM #2, #3, #4 Indirect Address

Refer to register 190h for the definition of these registers.

Register 291h, 391h, 491h: RWPM #2, #3, #4 Indirect Data

Refer to register 191h for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 0h): RWPM #2, #3, #4 STS-1 path Configuration

Refer to register 191h (IADDR = 0h) for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 1h): RWPM #2, #3, #4 PRBS[22:7] Accumulator

Refer to register 191h (IADDR = 1h) for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 2h): RWPM #2, #3, #4 PRBS[6:0] Accumulator

Refer to register 191h (IADDR = 2h) for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 3h): RWPM #2, #3, #4 B1/E1 value

Refer to register 191h (IADDR = 3h) for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 4h): RWPM #2, #3, #4 Error count

Refer to register 191h (IADDR = 4h) for the definition of these registers.

Register 291h, 391h, 491h (IADDR = 5h): RWPM #2, #3, #4 Received B1/E1 bytes

Refer to register 191h (IADDR = 5h) for the definition of these registers.

Register 293h, 393h, 493h: RWPM #2, #3, #4 Monitor Payload Configuration

Refer to register 193h for the definition of these registers.

Register 294h, 394h, 494h : RWPM #2, #3, #4 Monitor Byte Error Interrupt Status

Refer to register 194h for the definition of these registers.

Register 295h, 395h, 495h: RWPM #2, #3, #4 Monitor Byte Error Interrupt Enable

Refer to register 195h for the definition of these registers.

Register 296h,396h, 496h: RWPM #2, #3, #4 Monitor B1/E1 Byte Mismatch Interrupt Status

Refer to register 196h for the definition of these registers.

Register 297h, 397h, 497h: RWPM #2, #3, #4 Monitor B1/E1 Mismatch Interrupt Enable

Refer to register 197h for the definition of these registers.

Register 299h, 399h, 499h: RWPM #2, #3, #4 Monitor Synchronization Interrupt Status

Refer to register 199h for the definition of these registers.

Register 29Ah, 39Ah, 49Ah: RWPM #2, #3, #4 Monitor Synchronization Interrupt Enable

Refer to register 19Ah for the definition of these registers.

Register 29Bh, 39Bh, 49Bh: RWPM #2, #3, #4 Monitor Synchronization State

Refer to register 19Bh for the definition of these registers.

Register 29Ch, 39Ch, 49Ch: RWPM #2, #3, #4 Performance Counters Transfer Trigger

Refer to register 19Ch for the definition of these registers.

Register 2A0h, 3A0h, 4A0h: RPPM #2, #3, #4 Indirect Address

Refer to register 1A0h for the definition of these registers.

Register 2A1h, 3A1h, 4A1h: RPPM #2, #3, #4 Indirect Data

Refer to register 1A1h for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 0h): RPPM #2, #3, #4 STS-1 path Configuration

Refer to register 1A1h (IADDR = 0h) for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 1h): RPPM #2, #3, #4 PRBS[22:7] Accumulator

Refer to register 1A1h (IADDR = 1h) for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 2h): RPPM #2, #3, #4 PRBS[6:0] Accumulator

Refer to register 1A1h (IADDR = 2h) for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 3h): RPPM #2, #3, #4 B1/E1 value

Refer to register 1A1h (IADDR = 3h) for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 4h): RPPM #2, #3, #4 Error count

Refer to register 1A1h (IADDR = 4h) for the definition of these registers.

Register 2A1h, 3A1h, 4A1h (IADDR = 5h): RPPM #2, #3, #4 Received B1/E1 bytes

Refer to register 1A1h (IADDR = 5h) for the definition of these registers.

Register 2A3h, 3A3h, 4A3h: RPPM #2, #3, #4 Monitor Payload Configuration

Refer to register 1A3h for the definition of these registers.

Register 2A4h, 3A4h, 4A4h: RPPM #2, #3, #4 Monitor Byte Error Interrupt Status

Refer to register 1A4h for the definition of these registers.

Register 2A5h, 3A5h, 4A5h: RPPM #2, #3, #4 Monitor Byte Error Interrupt Enable

Refer to register 1A5h for the definition of these registers.

Register 2A6h, 3A6h, 4A6h: RPPM #2, #3, #4 Monitor B1/E1 Byte Mismatch Interrupt Status

Refer to register 1A6h for the definition of these registers.

Register 2A7h, 3A7h, 4A7h: RPPM #2, #3, #4 Monitor B1/E1 Mismatch Interrupt Enable

Refer to register 1A7h for the definition of these registers.

Register 2A9h, 3A9h, 4A9h: RPPM #2, #3, #4 Monitor Synchronization Interrupt Status

Refer to register 1A9h for the definition of these registers.

Register 2AAh, 3AAh, 4AAh: RPPM #2, #3, #4 Monitor Synchronization Interrupt Enable

Refer to register 1AAh for the definition of these registers.

Register 2ABh, 3ABh, 4ABh: RPPM #2, #3, #4 Monitor Synchronization State

Refer to register 1ABh for the definition of these registers.

Register 2ACh 3ACh, 4ACh: RPPM #2, #3, #4 Performance Counters Transfer Trigger

Refer to register 1ACh for the definition of these registers.

Register 2B0h, 3B0h, 4B0h: RAPM #2, #3, #4 Indirect Address

Refer to register 1B0h for the definition of these registers.

Register 2B1h, 3B1h, 4B1h: RAPM #2, #3, #4 Indirect Data

Refer to register 1B1h for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 0h): RAPM #2, #3, #4 STS-1 path Configuration

Refer to register 1B1h (IADDR = 0h) for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 1h): RAPM #2, #3, #4 PRBS[22:7] Accumulator

Refer to register 1B1h (IADDR = 1h) for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 2h): RAPM #2, #3, #4 PRBS[6:0] Accumulator

Refer to register 1B1h (IADDR = 2h) for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 3h): RAPM #2, #3, #4 B1/E1 value

Refer to register 1B1h (IADDR = 3h) for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 4h): RAPM #2, #3, #4 Error count

Refer to register 1B1h (IADDR = 4h) for the definition of these registers.

Register 2B1h, 3B1h, 4B1h (IADDR = 5h): RAPM #2, #3, #4 Received B1/E1 bytes

Refer to register 1B1h (IADDR = 5h) for the definition of these registers.

Register 2B3h, 3B3h, 4B3h: RAPM #2, #3, #4 Monitor Payload Configuration

Refer to register 1B3h for the definition of these registers.

Register 2B4h, 3B4h, 4B4h: RAPM #2, #3, #4 Monitor Byte Error Interrupt Status

Refer to register 1B4h for the definition of these registers.

Register 2B5h, 3B5h, 4B5h: RAPM #2, #3, #4 Monitor Byte Error Interrupt Enable

Refer to register 1B5h for the definition of these registers.

Register 2B6h, 3B6h, 4B6h: RAPM #2, #3, #4 Monitor B1/E1 Byte Mismatch Interrupt Status

Refer to register 1B6h for the definition of these registers.

Register 2B7h, 3B7h, 4B7h: RAPM #2, #3, #4 Monitor B1/E1 Mismatch Interrupt Enable

Refer to register 1B7h for the definition of these registers.

Register 2B9h, 3B9h, 4B9h: RAPM #2, #3, #4 Monitor Synchronization Interrupt Status

Refer to register 1B9h for the definition of these registers.

Register 2BAh, 3BAh, 4BAh: RAPM #2, #3, #4 Monitor Synchronization Interrupt Enable

Refer to register 1BAh for the definition of these registers.

Register 2BBh, 3BBh, 4BBh: RAPM #2, #3, #4 Monitor Synchronization State

Refer to register 1BBh for the definition of these registers.

Register 2BCh, 3BCh, 4BCh: RAPM #2, #3, #4 Performance Counters Transfer Trigger

Refer to register 1BBh for the definition of these registers.

Register 2C0h, 3C0h, 4C0h: OTPG #2, #3, #4 Indirect Address

Refer to register 1C0h for the definition of these registers.

Register 2C1h, 3C1h, 4C1h: OTPG #2, #3, #4 Indirect Data

Refer to register 1C1h for the definition of these registers.

Register 2C1h, 3C1h, 4C1h (IADDR = 8h): OTPG #2, #3, #4 STS-1 path Configuration

Refer to register 1C1h (IADDR = 8h) for the definition of these registers.

Register 2C1h, 3C1h, 4C1h (IADDR = 9h): OTPG #2, #3, #4 PRBS[22:7] Accumulator

Refer to register 1C1h (IADDR = 9h) for the definition of these registers.

Register 2C1h, 3C1h, 4C1h (IADDR = Ah): OTPG #2, #3, #4 PRBS[6:0] Accumulator

Refer to register 1C1h (IADDR = Ah) for the definition of these registers.

Register 2C1h, 3C1h, 4C1h (IADDR = Bh): OTPG #2, #3, #4 B1/E1 Value

Refer to register 1C1h (IADDR = Bh) for the definition of these registers.

Register 2C2h, 3C2h, 4C2h: OTPG #2, #3, #4 Generator Payload Configuration

Refer to register 1C2h for the definition of these registers.

Register 500H CSTR Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits must be set to their default values for proper operation.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the CSU1250 into a reset.ENG:It is joined with the CSTR ARB signal (using an AND gate) and is then connected to the CSU ARSTB pin through a high drive . For normal operation, it is held at logic ‘1’ In order to properly reset the CSU, CSU_RSTB should be held low for at least 1 ms.

CSU_ENB

The active low CSU enable control signal (CSU_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic 1. For normal operation, it is set to logic 0.

Register 501H CSTR Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

LOCKV

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the reference clock. LOCKV is set low when the CSU has not successfully locked with the reference SYSCLK. LOCKV is set high when the CSU has locked with the reference SYSCLK.

LOCKE

The CSU lock interrupt enable bit (LOCKE) controls the assertion of CSU lock state interrupts by the CSTR. When LOCKE is high, an interrupt is generated when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

Register 502H CSTR Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOCKI	0

LOCKI

The CSU lock interrupt status bit (LOCKI) responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock, or loses its lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occurs. LOCKI register bit will be cleared when it is read. When LOCKE is set high, LOCKI is used to produce the interrupt output that is reflected in the TBS Master TSI, DLL and CSTR Interrupt Status register. Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit itself remains valid and may be polled to detect change of lock status events.

13 Test Feature Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TBS. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[11]) is high.

In addition, the TBS also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

14 Operation

14.1 Power Conservation

In order to realize power savings, any of the twelve LVDS link may be disabled regardless of the port it is on. As well, the entire working, protect or auxiliary ports can be disabled.

Consider for example, that a user wishes to disable the fourth transmit and receive LVDS links on the TBS. The transmitter would be disabled by setting bits 7 and 8 high in register 455H. The receiver is disabled by setting bits 12 and 13 high in register 483H.

Should a user wish to power down a complete port (working, protect, auxiliary) the best approach is to reset the entire port in the Master Reset Register. For example in order to power down the entire Auxiliary Port, bits 8 and 11 in register 003H should be set high.

The following formulae can be used to estimate typical power consumption for a given configuration. Note: these formulae assume full PRBS activity is used in conjunction with other device functions. Further reduction in power consumption would be possible if the PRBS generators and monitors were disabled.

Assume the following variable definitions:

Number of powered Transmit Ports = x

Number of powered Receive Ports = y

Number of powered Transmit LVDS links = n

Number of powered Receive LVDS links = m

Then, the power consumption per rail can be estimated as follows:

VDDI: 0.0179x + 0.0522y + 0.8415 W

VDDO: 0.5142 W

AVDH: 0.0355n + 0.0039m + 0.0403 W

AVDL: 0.0079n + 0.0161m + 0.4094 W

CSU_AVDH: 0.0483 W

This implies that:

Total 1.8V power: 0.0179x + 0.0522y + 0.0079n + 0.0161m + 1.2509 W

Total 3.3V power: 0.0355n + 0.0039m + 0.6027 W

and finally:

Estimated Typical Power Consumption = 0.0179x + 0.0522y + 0.0435n + 0.0200m + 1.8536 W

For a fully enabled device (x=y=3, m=n=12), we would expect:

Estimated Typical Power Consumption = 2.82W

Actual results will also depend on power supply levels and on-chip data-dependent activity.

14.2 Parallel TelecomBus Termination

It is recommended that the both "Incoming TelecomBus Stream" and "Outgoing TelecomBus Stream" signals (as defined the Pin Description section) use 65 Ohm controlled-impedance traces. In addition, when the outgoing signals are used to drive traces longer than 1 inch, it is recommended that series termination resistors of 51 Ohms be added.

14.3 LVDS Optimizations

The LVDS interface implemented on the TBS and TSE follows the IEEE 1596.3-1996 specification with some minor exceptions. The changes are implemented to customize and optimize the LVDS interface for the system and are described in detail below. Even with these differences the LVDS interface should be compatible with the physical layer of other LVDS interfaces. The differences from the IEEE specification include:

1. Faster rise/fall times (200 – 400) ps versus the specified (300 - 500) ps. Faster edge rates are commonly used with higher speed LVDS interfaces in the industry to ease interfacing. The IEEE 1596.3-1996 edge rates are optimized for data rates below 400 Mbps.

2. Hysteresis is not implemented in the receive LVDS interface. Hysteresis is used in many implementations to negate the effect of noise that may exist on unused LVDS links. Hysteresis was not implemented in the CHESS set devices to minimize circuit complexity, power, and cost. Instead, the RX interfaces and the DRUs for unused links can be disabled (powered down) through register control in order to prevent sensitivity to noise on these links.

3. The LVDS transmitter contains an on-chip 100-ohm termination. Most implementations use a single 100-ohm termination on the receiver. By implementing a double termination (on both the LVDS receiver and transmitter) better signal integrity and matching is ensured.

4. Although not a difference with the Layer 1 IEEE 1596.3-1996 specification, the Layer 2 8B/10B encoding is discussed here for completeness. 8B/10B encoding guarantees transition density as compared to scrambled encoding, which provides only a certain probability of transition density. This guaranteed transition density allows a simpler and more power-effective data recovery unit, provides a more robust serial interface (greater trace or back-plane distance achievable). It also negates the need for complete SONET framing since the A1 A2 and J0 bytes can be encoded into special escape characters of the LVDS data stream.

5. The device uses 20% resistors; not 10% as specified by the LVDS specification. They are 20% resistors since that was the highest tolerance resistor available for on-chip applications. However, because they are integrated on-chip, this LVDS interface can achieve much better signal integrity than one with off-chip terminations.

14.4 LVDS Hot Swapping

The LVDS electrical interface differs from a standard CMOS interface; there is no inherent problem in leaving the LVDS inputs floating. Note that the LVDS receiver consists of a differential amplifier with a wide common-mode range. The power dissipation is independent of the data transitions (that is, if the input is connected). There is an internal 100 Ω termination across the positive and negative input. Floating inputs will settle to an arbitrary voltage (between VDD and VSS) determined by leakage paths. Regardless of this arbitrary voltage, the input structure of the receiver will operate in its proper range and the receiver output will be logic 1 or 0 depending on internal offsets. Noise events (power supply noise, crosstalk) may induce the receiver to toggle randomly, generating "ambiguous" data.

Unused links should be disabled in software. This will ensure that the power consumption for those links will be reduced to nearly 0 mW. There is no requirement for how quickly the link should be disabled. Disabling the link simply results in lower power dissipation since the circuitry will be shut down. This action is not mandatory, but is good practice.

During a hot-swapping situation, there will be no electrical damage on the LVDS inputs provided that maximum ratings are not exceeded (see absolute maximum ratings section 16). The “hot-swap” channel can be left enabled and the device will sync up once the far end transmitter is connected. There are no effects on other channels. Hot swapping of cards is still allowed by reprogramming of the links in software.

14.5 LVDS Trace Lengths

The TBS utilizes 12 different input and output differential LVDS pairs. It is critical to match the lengths of the positive and negative traces of each differential pair to minimize skew and maximize the eye opening. However, matching one differential pair to another pair is not as important. As discussed in section 14.16 - “J0” Synchronization of the TBS in a CHESS™ System, the high-speed serial LVDS links are connected to a 24 word (10 bit words) FIFO. Of this 24 word margin, 8 words should be allocated for clock skew and wander between cards or within devices. The remaining 16 words are then available to accommodate differences in trace lengths between LVDS pairs.

The 16 word FIFO yields an allowable inter-link delay differential of 205.8 ns or 41.2m. This is calculated as follows:

16 words x 10 bits/word = 160 bits of margin in FIFO

1/(777.6 Mb/s) = 1.29 ns/bit on the serial link

160 bits x 1.29 ns/bit = 205.8 ns of margin = 16 clock cycles (at 77.76 MHz)

A transmission speed of 2/3 the speed of light, this corresponds to a trace length difference of 41.2m:

$205.8x10^{9}$s x 2/3 x $3x10^{8}$ m/s = 41.2 m

However, it is important to note that the LVDS interface itself is designed to drive 1m of backplane plus only 30cm of trace length on either side. Since this 1.6m of trace length is smaller than the maximum trace length differential computed above, the TBS' ability to tolerate trace length differential will not be a limiting factor for designs.

The total available trace length of 1.6m corresponds to 8ns of delay or a worst case difference of 0.6 clock cycles (77.76 MHz) between any two LVDS links. Low loss cable or an optical interface can be used to connect to the LVDS interface to realize greater back-plane distances, which may require more careful consideration of the inter-link delay differentials.

14.6 JTAG Test Port

The TBS JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 8 Instruction Register (Length - 3 Bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 9 Identification Register

Length	32 bits
Version Number	1H
Part Number	5310H
Manufacturer's Identification Code	0CDH
Device Identification	153100CDH

Table 10 Boundary Scan Register

Length - 246 bits

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
RJ0FP	245	IN_CELL	L	OEB_OCOUT[2]	122	OUT_CELL	-
OEB_TJ0FP	244	OUT_CELL	L	OCOUT[2]	121	OUT_CELL	-
TJ0FP	243	OUT_CELL	L	OEB_OD_2[7]	120	OUT_CELL	-
ITV5[4]	242	IN_CELL	H	OD_2[7]	119	OUT_CELL	-
ITPL[4]	241	IN_CELL	L	OEB_OD_2[6]	118	OUT_CELL	-
ITAIS[4]	240	IN_CELL	H	OD_2[6]	117	OUT_CELL	-
IPAIS[4]	239	IN_CELL	L	OEB_OD_2[5]	116	OUT_CELL	-
IDP[4]	238	IN_CELL	H	OD_2[5]	115	OUT_CELL	-
ID_4[7]	237	IN_CELL	L	OEB_OD_2[4]	114	OUT_CELL	-
ID_4[6]	236	IN_CELL	L	OD_2[4]	113	OUT_CELL	-
ID_4[5]	235	IN_CELL	H	OEB_OD_2[3]	112	OUT_CELL	-
ID_4[4]	234	IN_CELL	H	OD_2[3]	111	OUT_CELL	-
ID_4[3]	233	IN_CELL	L	OEB_OD_2[2]	110	OUT_CELL	-
ID_4[2]	232	IN_CELL	L	OD_2[2]	109	OUT_CELL	-
ID_4[1]	231	IN_CELL	L	OEB_OD_2[1]	108	OUT_CELL	-
ID_4[0]	230	IN_CELL	H	OD_2[1]	107	OUT_CELL	-
IPL[4]	229	IN_CELL	L	OEB_OD_2[0]	106	OUT_CELL	-
IJOJ1[4]	228	IN_CELL	L	OD_2[0]	105	OUT_CELL	-
OEB_OTV5[4]	227	OUT_CELL	L	OEB_OPL[2]	104	OUT_CELL	-
OTV5[4]	226	OUT_CELL	L	OPL[2]	103	OUT_CELL	-
OEB_OTPL[4]	225	OUT_CELL	L	OEB_OJ0J1[2]	102	OUT_CELL	-
OTPL[4]	224	OUT_CELL	L	OJ0J1[2]	101	OUT_CELL	-
OEB_OTAIS[4]	223	OUT_CELL	L	ITV5[1]	100	IN_CELL	-
OTAIS[4]	222	OUT_CELL	L	ITPL[1]	99	IN_CELL	-
OEB_OPAIS[4]	221	OUT_CELL	H	ITAIS[1]	98	IN_CELL	-
OPAIS[4]	220	OUT_CELL	H	IPAIS[1]	97	IN_CELL	-
OEB_ODP[4]	219	OUT_CELL	L	IDP[1]	96	IN_CELL	-
ODP[4]	218	OUT_CELL	L	ID_1[7]	95	IN_CELL	-
OEB_OCOUT[4]	217	OUT_CELL	H	ID_1[6]	94	IN_CELL	-
OCOUT[4]	216	OUT_CELL	H	ID_1[5]	93	IN_CELL	-
OEB_OD_4[7]	215	OUT_CELL	L	ID_1[4]	92	IN_CELL	-
OD_4[7]	214	OUT_CELL	H	ID_1[3]	91	IN_CELL	-
OEB_OD_4[6]	213	OUT_CELL	-	ID_1[2]	90	IN_CELL	-
OD_4[6]	212	OUT_CELL	-	ID_1[1]	89	IN_CELL	-
OEB_OD_4[5]	211	OUT_CELL	-	ID_1[0]	88	IN_CELL	-
OD_4[5]	210	OUT_CELL	-	IPL[1]	87	IN_CELL	-
OEB_OD_4[4]	209	OUT_CELL	-	IJOJ1[1]	86	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OD_4[4]	208	OUT_CELL	-	OEB_OTV5[1]	85	OUT_CELL	-
OEB_OD_4[3]	207	OUT_CELL	-	OTV5[1]	84	OUT_CELL	-
OD_4[3]	206	OUT_CELL	-	OEB_OTPL[1]	83	OUT_CELL	-
OEB_OD_4[2]	205	OUT_CELL	-	OTPL[1]	82	OUT_CELL	-
OD_4[2]	204	OUT_CELL	-	OEB_OTAIS[1]	81	OUT_CELL	-
OEB_OD_4[1]	203	OUT_CELL	-	OTAIS[1]	80	OUT_CELL	-
OD_4[1]	202	OUT_CELL	-	OEB_OPAIS[1]	79	OUT_CELL	-
OEB_OD_4[0]	201	OUT_CELL	-	OPAIS[1]	78	OUT_CELL	-
OD_4[0]	200	OUT_CELL	-	OEB_ODP[1]	77	OUT_CELL	-
SYSCLK	199	IN_CELL	-	ODP[1]	76	OUT_CELL	-
OEB_OPL[4]	198	OUT_CELL	-	OEB_OCOUT[1]	75	OUT_CELL	-
OPL[4]	197	OUT_CELL	-	OCOUT[1]	74	OUT_CELL	-
OEB_OJ0J1[4]	196	OUT_CELL	-	OEB_OD_1[7]	73	OUT_CELL	-
OJ0J1[4]	195	OUT_CELL	-	OD_1[7]	72	OUT_CELL	-
ITV5[3]	194	IN_CELL	-	OEB_OD_1[6]	71	OUT_CELL	-
ITPL[3]	193	IN_CELL	-	OD_1[6]	70	OUT_CELL	-
ITAIS[3]	192	IN_CELL	-	OEB_OD_1[5]	69	OUT_CELL	-
IPAIS[3]	191	IN_CELL	-	OD_1[5]	68	OUT_CELL	-
IDP[3]	190	IN_CELL	-	OEB_OD_1[4]	67	OUT_CELL	-
ID_3[7]	189	IN_CELL	-	OD_1[4]	66	OUT_CELL	-
ID_3[6]	188	IN_CELL	-	OEB_OD_1[3]	65	OUT_CELL	-
ID_3[5]	187	IN_CELL	-	OD_1[3]	64	OUT_CELL	-
ID_3[4]	186	IN_CELL	-	OEB_OD_1[2]	63	OUT_CELL	-
ID_3[3]	185	IN_CELL	-	OD_1[2]	62	OUT_CELL	-
ID_3[2]	184	IN_CELL	-	OEB_OD_1[1]	61	OUT_CELL	-
ID_3[1]	183	IN_CELL	-	OD_1[1]	60	OUT_CELL	-
ID_3[0]	182	IN_CELL	-	OEB_OD_1[0]	59	OUT_CELL	-
IPL[3]	181	IN_CELL	-	OD_1[0]	58	OUT_CELL	-
IJOJ1[3]	180	IN_CELL	-	OEB_OPL[1]	57	OUT_CELL	-
OEB_OTV5[3]	179	OUT_CELL	-	OPL[1]	56	OUT_CELL	-
OTV5[3]	178	OUT_CELL	-	OEB_OJ0J1[1]	55	OUT_CELL	-
OEB_OTPL[3]	177	OUT_CELL	-	OJ0J1[1]	54	OUT_CELL	-
OTPL[3]	176	OUT_CELL	-	OEB_D[15]	53	OUT_CELL	-
OEB_OTAIS[3]	175	OUT_CELL	-	D[15]	52	IO_CELL	-
OTAIS[3]	174	OUT_CELL	-	OEB_D[14]	51	OUT_CELL	-
OEB_OPAIS[3]	173	OUT_CELL	-	D[14]	50	IO_CELL	-
OPAIS[3]	172	OUT_CELL	-	OEB_D[13]	49	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_ODP[3]	171	OUT_CELL	-	D[13]	48	IO_CELL	-
ODP[3]	170	OUT_CELL	-	OEB_D[12]	47	OUT_CELL	-
OEB_OCOUT[3]	169	OUT_CELL	-	D[12]	46	IO_CELL	-
OCOUT[3]	168	OUT_CELL	-	OEB_D[11]	45	OUT_CELL	-
OEB_OD_3[7]	167	OUT_CELL	-	D[11]	44	IO_CELL	-
OD_3[7]	166	OUT_CELL	-	OEB_D[10]	43	OUT_CELL	-
OEB_OD_3[6]	165	OUT_CELL	-	D[10]	42	IO_CELL	-
OD_3[6]	164	OUT_CELL	-	OEB_D[9]	41	OUT_CELL	-
OEB_OD_3[5]	163	OUT_CELL	-	D[9]	40	IO_CELL	-
OD_3[5]	162	OUT_CELL	-	OEB_D[8]	39	OUT_CELL	-
OEB_OD_3[4]	161	OUT_CELL	-	D[8]	38	IO_CELL	-
OD_3[4]	160	OUT_CELL	-	OEB_D[7]	37	OUT_CELL	-
OEB_OD_3[3]	159	OUT_CELL	-	D[7]	36	IO_CELL	-
OD_3[3]	158	OUT_CELL	-	OEB_D[6]	35	OUT_CELL	-
OEB_OD_3[2]	157	OUT_CELL	-	D[6]	34	IO_CELL	-
OD_3[2]	156	OUT_CELL	-	OEB_D[5]	33	OUT_CELL	-
OEB_OD_3[1]	155	OUT_CELL	-	D[5]	32	IO_CELL	-
OD_3[1]	154	OUT_CELL	-	OEB_D[4]	31	OUT_CELL	-
OEB_OD_3[0]	153	OUT_CELL	-	D[4]	30	IO_CELL	-
OD_3[0]	152	OUT_CELL	-	OEB_D[3]	29	OUT_CELL	-
OEB_OPL[3]	151	OUT_CELL	-	D[3]	28	IO_CELL	-
OPL[3]	150	OUT_CELL	-	OEB_D[2]	27	OUT_CELL	-
OEB_OJ0J1[3]	149	OUT_CELL	-	D[2]	26	IO_CELL	-
OJ0J1[3]	148	OUT_CELL	-	OEB_D[1]	25	OUT_CELL	-
ITV5[2]	147	IN_CELL	-	D[1]	24	IO_CELL	-
ITPL[2]	146	IN_CELL	-	OEB_D[0]	23	OUT_CELL	-
ITAIS[2]	145	IN_CELL	-	D[0]	22	IO_CELL	-
IPAIS[2]	144	IN_CELL	-	A[11]	21	IN_CELL	-
IDP[2]	143	IN_CELL	-	A[10]	20	IN_CELL	-
ID_2[7]	142	IN_CELL	-	A[9]	19	IN_CELL	-
ID_2[6]	141	IN_CELL	-	A[8]	18	IN_CELL	-
ID_2[5]	140	IN_CELL	-	A[7]	17	IN_CELL	-
ID_2[4]	139	IN_CELL	-	A[6]	16	IN_CELL	-
ID_2[3]	138	IN_CELL	-	A[5]	15	IN_CELL	-
ID_2[2]	137	IN_CELL	-	A[4]	14	IN_CELL	-
ID_2[1]	136	IN_CELL	-	A[3]	13	IN_CELL	-
ID_2[0]	135	IN_CELL	-	A[2]	12	IN_CELL	-
IPL[2]	134	IN_CELL	-	A[1]	11	IN_CELL	-
IJOJ1[2]	133	IN_CELL	-	A[0]	10	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_OTV5[2]	132	OUT_CELL	-	ALE	9	IN_CELL	-
OTV5[2]	131	OUT_CELL	-	RDB	8	IN_CELL	-
OEB_OTPL[2]	130	OUT_CELL	-	CSB	7	IN_CELL	-
OTPL[2]	129	OUT_CELL	-	WRB	6	IN_CELL	-
OEB_OTAIS[2]	128	OUT_CELL	-	OEB_INTB	5	OUT_CELL	-
OTAIS[2]	127	OUT_CELL	-	INTB	4	OUT_CELL	-
OEB_OPAIS[2]	126	OUT_CELL	-	RSTB	3	IN_CELL	-
OPAIS[2]	125	OUT_CELL	-	RWSEL	2	IN_CELL	-
OEB_ODP[2]	124	OUT_CELL	-	OCMP	1	IN_CELL	-
ODP[2]	123	OUT_CELL	-	TCMP	0	IN_CELL	-

NOTES:

1. When set high, INTB will be set to high impedance.
2. HIZ is the active low output enable for all OUT_CELL types except D[15:0], and INTB.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexor in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 9 Input Observation Cell (IN_CELL)

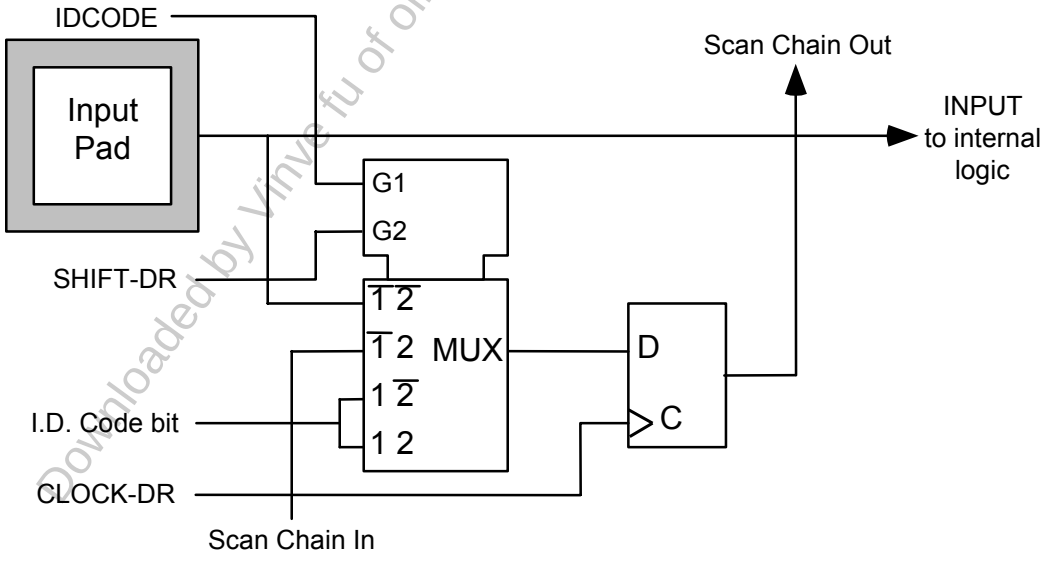


Figure 10 Output Cell (OUT_CELL)

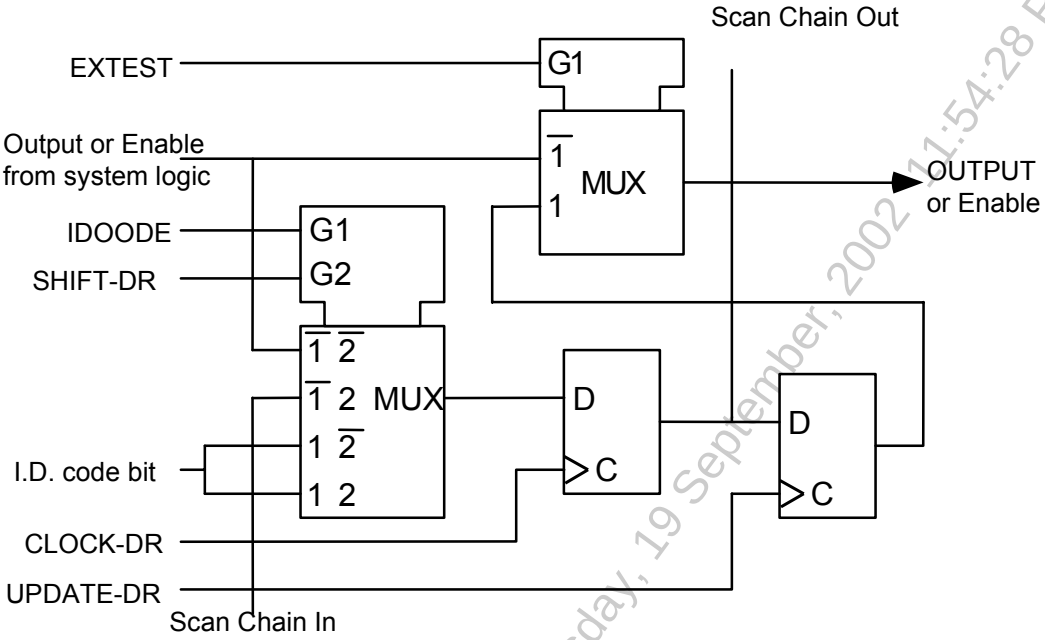


Figure 11 Bi-directional Cell (IO_CELL)

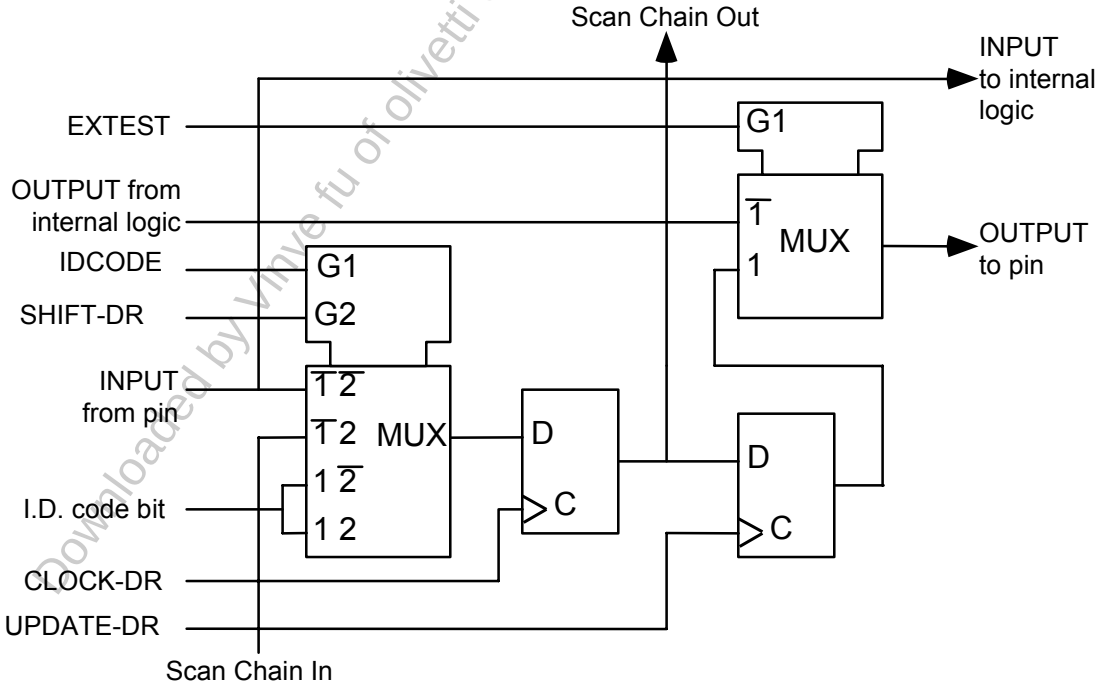
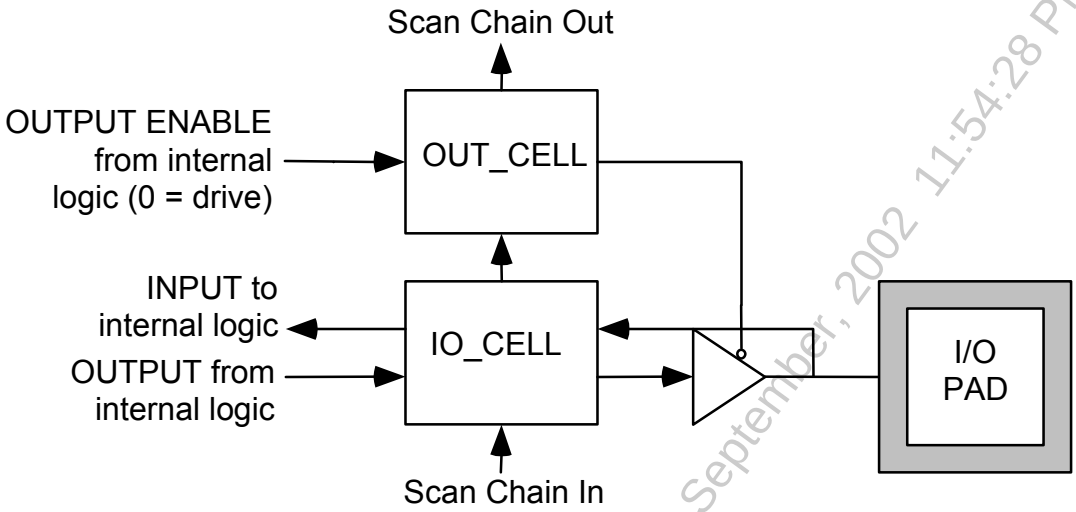


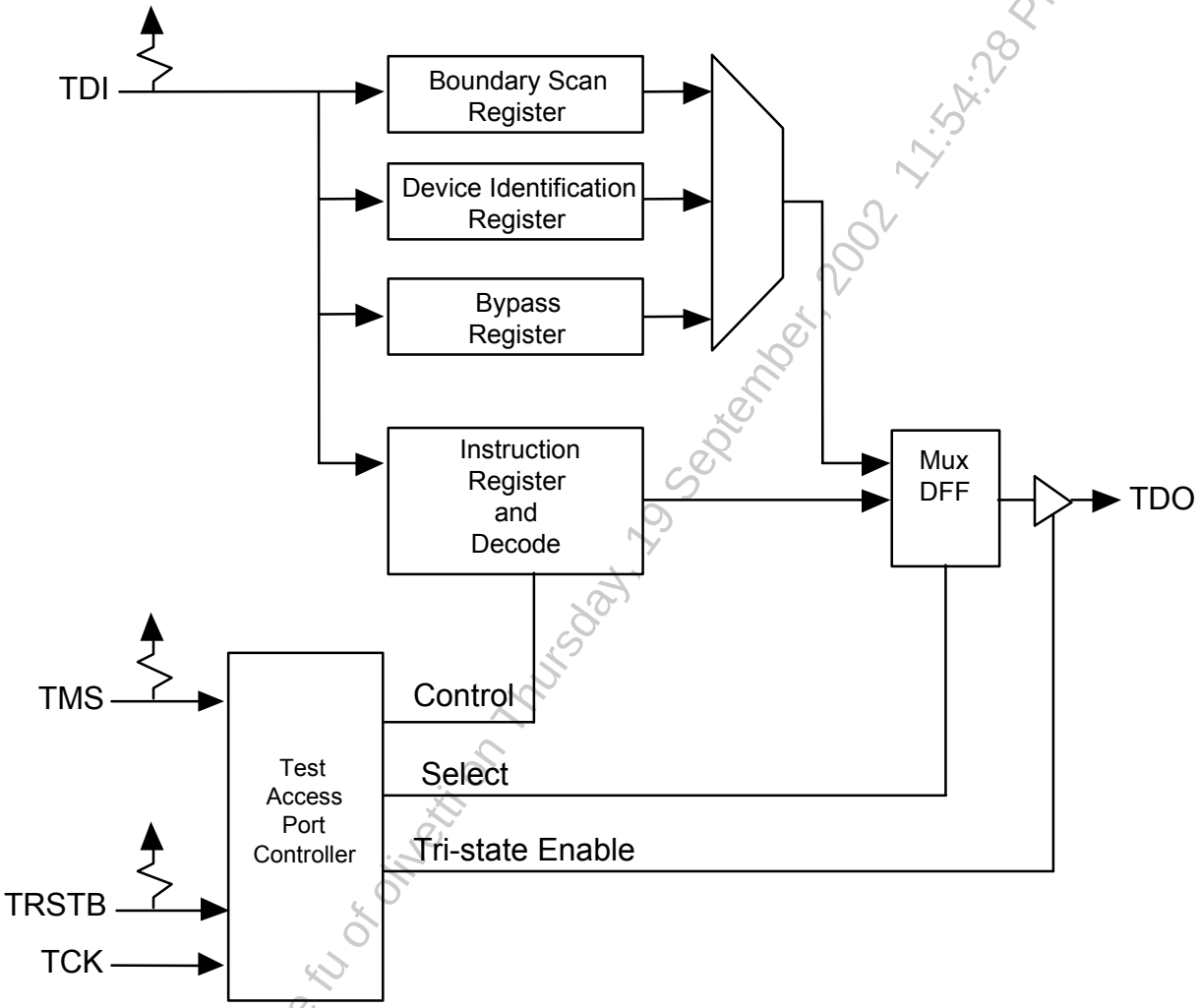
Figure 12 Layout of Output Enable and Bi-directional Cells



14.7 JTAG Support

The TBS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI, and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 13 Boundary Scan Architecture



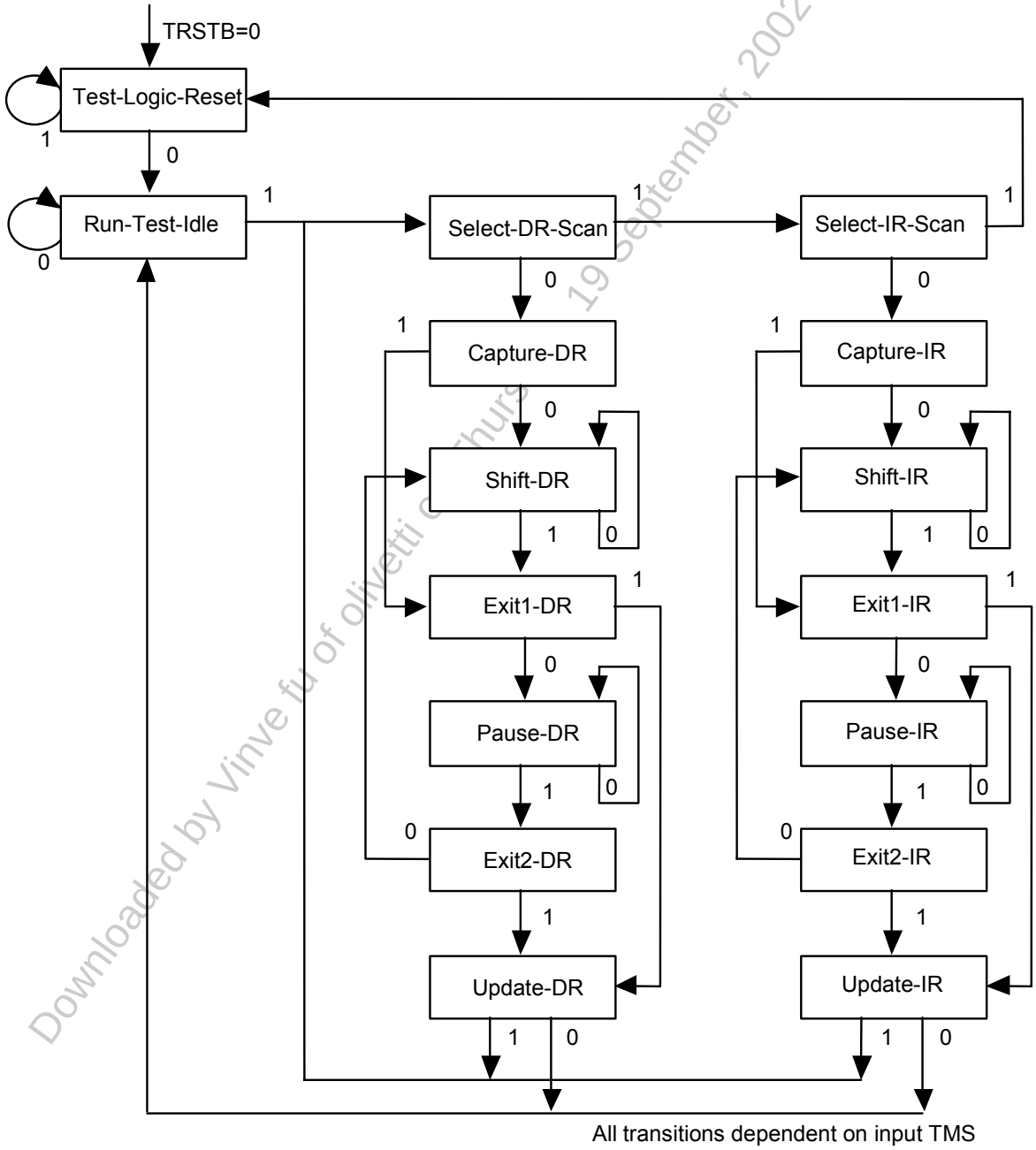
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

14.7.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 14 TAP Controller Finite State Machine



14.7.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

14.7.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14.8 Interrupt Service Routine

The TBS will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the registers 004H, 00DH, 00EH, 00FH, 010H, and 011H to find the functional block(s) which caused the interrupt.

2. Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

3. Service the interrupt(s).

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

14.9 Accessing Indirect Registers

Indirect registers are used to conserve address space in the TBS. Writing the indirect address register accesses indirect registers. The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data registers.

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data registers to find the state of the register bits for the selected channel number.

Software Design Notes:

Software should not attempt to write to indirect addresses other than those specifically mentioned in the register description. Other indirect addresses should be considered reserved.

Software should implement a timeout so that a BUSY bit which is stuck at 1 will not cause an infinite loop in the software. BUSY bits will not be stuck at 1 in normal operation, but may become stuck at 1 if an invalid access is attempted, or an access is attempted while the device is not being clocked.

The maximum amount of time software needs to wait for the BUSY bit to clear after an indirect access is triggered is shown in Table 11.

Table 11 Indirect Access Maximum BUSY Times

Register Address	Block Name	SYSCLK cycles to clear BUSY (MAX)
0020H, 0030H, 0040H	TWTI, TPTI, TATI	10
0080H, 0090H, 00A0H	RWTI, RPTI, RATI	10
0100H, 0200H, 0300H, 0400H	ITPP#1-#4	17
0190H, 0290H, 0390H, 0490H	RWPM#1-#4	17
01A0H, 02A0H, 03A0H, 04A0H	RPPM#1-#4	17
01B0H, 02B0H, 03B0H, 04B0H	RAPM#1-#4	17
01C0H, 02C0H, 03C0H, 04C0H	OTPG#1-#4	17

14.10 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled at regular intervals. The counters will saturate and not roll over if they reach their maximum value.

Writing to the TBS Master Input Signal Activity, Accumulation Trigger register (002H) causes a device update of all the counters. If this register is written to, the TIP bit in the TBS Master Accumulation Transfer and Parity Error Interrupt Status register (005H) can be polled to determine when all the counter values have been transferred and are ready to be read. Alternately, software can wait the number of cycles shown in the Table 12.

Table 12 Maximum Performance Monitor Counter Transfer Time

Trigger Register Address	Block Name	SYSCLK cycles to complete transfer (MAX)
0002H	All R8TD and PRBS Monitor Blocks	17
0162H, 0262H, 0362H, 0462H	RW8D#1-#4	6
0172H, 0272H, 0372H, 0472H	RP8D#1-#4	6
0182H, 0282H, 0382H, 0482H	RA8D#1-#4	6
010CH, 020CH, 030CH, 040CH	ITPP#1-#4	17
019CH, 029CH, 039CH, 049CH	RWPM#1-#4	17
01ACH, 02ACH, 03ACH, 04ACH	RPPM#1-#4	17
01BCH, 02BCH, 03BCH, 04BCH	RAPM#1-#4	17

14.11 Interpreting the Status of Receive Decoders

The receive decoder blocks (Rx8D) produce interrupts based on four receiver conditions or events: OCA (Out of Character Alignment), OFA (Out of Frame Alignment), FUO (FIFO Underrun/Overrun) and LCV (Line Code Violation). Understanding the relationships between these conditions can help to diagnose device status. These conditions have the following inter-relationships:

- OCA implies OFA until character alignment is re-achieved. OCA will most likely cause some LCVs but not necessarily a continual stream. Since character boundaries are not known, framing and disparity are meaningless.
- OFA, by itself, does not cause any of the other conditions.
- FUO may produce zero, one or many LCVs, depending on how the FIFO overrun/underrun occurs.
- Persistent LCVs (five or more in any sequence of 15 characters) cause OCA.

14.12 Setting up Timeslot Assignments in the RWTI, RPTI, and RATI

The receive timeslot interchange (TSI) blocks in the TBS (RWTI, RPTI, and RATI) can be used to rearrange the position of SONET/SDH timeslots. Each block buffers 48 timeslots and rearranges them as desired before outputting them. The TSI blocks allow user configuration of timeslot mappings, bypass of timeslot switching, and predefined mappings for standard TelecomBus interfaces.

The RWSEL input signal will select whether the RWTI or RPTI outputs are directed to the Outgoing TelecomBus if the RWSEL_EN register bit (register 001H) is set to logic 1. See Section 14.14 for details.

The RWTSEN register bit in RWTI Indirect Data register, the RPTSEN register bit in RPTI Indirect Data register, and the RATSEN register bit in RATI Indirect Data register enable per-STS-1 timeslot selection among the RWTI, RPTI, or RATI outputs when the RWSEL_EN register bit is set to logic 0. For each timeslot, one and only one of the RWTSEN, RPTSEN or RATSEN must be set high. See Section 14.14 for details.

14.12.1 Receive Timeslot Mapping

The standard Timeslot Map at the TBS interface is shown in Table 13. The timeslots on the left side of Table 13 are presented on OD[x] before the timeslots on the right. The following discussion references OD[x][7:0], but can also apply to their associated control signals.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by ‘x’ and the column number within the STS-3/STM-1 is given by ‘y’. With such a mapping, an STS-12c/STM-4c data stream will be transferred across one complete OD[x][7:0] bus and an STS-48/STM-16 data stream will be transferred across the 32-bit bus OD[4:1][7:0].

The mapping shown in Table 13 can also be applied to the serial TelecomBus. If the working serial TelecomBus links were selected, RPWRK[1]/RNWRK[1] would carry the timeslots shown for OD[1][7:0] in bit-serial order. RPWRK[2]/RNWRK[2] would carry the timeslots shown for OD[2][7:0] and so on.

Table 13 Standard Outgoing TelecomBus Timeslot Map

OD[1][7:0]	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
OD[2][7:0]	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
OD[3][7:0]	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
OD[4][7:0]	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

14.12.2 Custom Timeslot Mappings

If the RTSI_MODE[1:0] bits (register 001H) are set to ‘b00, then the RPTI, RWTI, and RATI blocks will be set for custom timeslot mapping. This permits the user to swap the position of or multicast any STS-1/STM-0 timeslot.

The channels must still fit into the required system-side timeslot map in a manner that is required by a channel of such a rate. For example, an STS-3c channel which occupied timeslots (S1,1, S1,2, S1,3) in Table 13 on the selected receive serial TelecomBus links can be moved to the outgoing parallel TelecomBus timeslots (S7,1, S7,2, S7,3).

The following procedure shows how the RWTI (or RPTI or RATI) block can be programmed perform such a remapping of timeslots. Page 0 of the RWTI block is configured in the example.

1. Set RTSI_MODE[1:0] equal to ‘b00.
2. Read BUSY in the RWTI Indirect Address register at 080H. If it is logic 0, proceed to step 3. Otherwise, poll BUSY until it is logic 0.
3. Write 0010H to the RWTI Indirect Data register at 081H to set WTSEL[3:0] to 1 and WLSEL[1:0] to 0. This selects the timeslot S1,1 as the input timeslot.
4. Write 0031H to the RWTI Indirect Address register at 080H to set ODTSEL[3:0] to 3 and ODSEL[1:0] to 1. This selects the position S7,1 on the output timeslot in the page 0 mapping of the RWTI.
5. Read BUSY in the RWTI Indirect Address register at 080H. If it is logic 0, proceed to step 6. Otherwise, poll BUSY until it is logic 0.
6. Write 0050H to the RWTI Indirect Data register at 081H to set WTSEL[3:0] to 5 and WLSEL[1:0] to 0. This selects the timeslot S1,2 as the input timeslot.
7. Write 0071H to the RWTI Indirect Address register at 080H to set ODTSEL[3:0] to 7 and ODSEL[1:0] to 1. This selects the position S7,2 on the output timeslot in the page 0 mapping of the RWTI.
8. Read BUSY in the RWTI Indirect Address register at 080H. If it is logic 0, proceed to step 9. Otherwise, poll BUSY until it is logic 0.
9. Write 0090H to the RWTI Indirect Data register at 081H to set WTSEL[3:0] to 9 and WLSEL[1:0] to 0. This selects the timeslot S1,3 as the input timeslot.
10. Write 00B1H to the RWTI Indirect Address register at 080H to set ODTSEL[3:0] to BH and ODSEL[1:0] to 1. This selects the position S7,3 on the output stream in the page 0 mapping of the RWTI.

14.13 Setting up Timeslot Assignments in the TWTI, TPTI, and TATI

The transmit timeslot interchange (TSI) blocks in the TBS (TWTI, TPTI, and TATI) can be used to rearrange the position of SONET/SDH timeslots prior to transmission on the serial TelecomBus links. Each block buffers 48 timeslots and rearranges them as desired before outputting them. The TSI blocks allow user configuration of timeslot mappings, basic bypass of timeslots, and predefined mappings for standard TelecomBus interfaces.

14.13.1 Transmit Timeslot Mapping

The Timeslot Mapping done by the TWTI, TPTI, and TATI is identical to that discussed in Section **Error! Reference source not found.** except there is no separation of data and control signals. The TWTI, TPTI, and TATI deal with 8B/10B encoded data so the TelecomBus control signals are inherent in the 10 bit data presented to and interchanged in these blocks. The standard incoming parallel TelecomBus timeslot mapping is shown in Table 14. The timeslots on the left side of Table 14 are presented to ID[x] before the timeslots on the right.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by ‘x’ and the column number within the STS-3/STM-1 is given by ‘y’. With such a mapping, an STS-12c/STM-4c data stream will be transferred across one complete ID[x][7:0] bus and an STS-48/STM-16 data stream will be transferred across the 32-bit bus ID[4:1][7:0].

The mapping shown in Table 14 can also be applied to the transmit serial TelecomBus. TPWRK[1]/TNWRK[1] would carry the timeslots shown for ID[1][7:0] in bit-serial order. TPWRK[2]/TNWRK[2] would carry the timeslots shown for ID[2][7:0] and so on.

Table 14 Standard Incoming TelecomBus Timeslot Map

ID[1][7:0]	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
ID[2][7:0]	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
ID[3][7:0]	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
ID[4][7:0]	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

14.13.2 Custom Timeslot Mappings

If the TTSI_MODE[1:0] bits (register 000H) are set to ‘b00, then the TWTI, TPTI, and TATI blocks will be set for custom timeslot mapping. This permits the user to swap the position of or multicast any STS-1/STM-0 timeslot.

The channels must still fit into the required system-side timeslot map in a manner that is required by a channel of such a rate. For example, an STS-3c channel which occupied timeslots (S1,1, S1,2, S1,3) in Table 14 on the selected incoming parallel TelecomBus bus can be moved to the transmit serial TelecomBus timeslots (S7,1, S7,2, S7,3). Note that this is not strictly true if in a system another TBS will be receiving this datastream. The receiving TBS has an RTSI block which could be used to further map the timeslots into their final locations.

The mapping procedure is identical to that shown in Section 14.12.2.

14.13.3 Active and Standby Pages in the TSI Blocks

The TSI (RWTI, RPTI, RATI, TWTI, TPTI, and TATI) blocks contain 2 pages of configurations: an active page, and an inactive page. Selection of the page in use in the RWTI, RPTI, and RATI is done by the OCMP input signal. Selection of the page in use in the TWTI, TPTI, and TATI is done by the TCMP input signal.

The existence of an active page and an inactive page allows the user to set up an alternate timeslot mapping on multiple devices or multiple TSI blocks before performing a global switch to the new mapping. The swapping of the page in use is done at transport frame boundaries under the control of the TCMP and OCMP input signals. The TCMP is sampled at the J0 byte location within a frame as defined by IJ0J1[1] = '1' and IPL[1] = '0'. The OCMP control signal is sampled at the J0 locations defined by RJ0FP = '1'. The actual switching of pages occurs on the second frame boundary after the TCMP or OCMP signals have been sampled.

14.14 Using RWSEL and RWTSEN, RPTSEN, and RATSEN

The RWSEL signal and RWTSEN, RPTSEN, and RATSEN register bits are used to select how the working, protection, and auxiliary receive serial TelecomBus signals (RPWRK[4:1]/RNWRK[4:1], RPPROT[4:1]/RNPROT[4:1] and RPAUX[4:1]/RNAUX[4:1]) are directed to the outgoing parallel TelecomBus interface.

The RWSEL input pin is used to perform a global switch between the working and protection serial TelecomBus. The auxiliary links are not used. RWSEL is only active when the RWSEL_EN register bit in the TBS Master Outgoing Configuration and Control register (001H) is set to logic 1. When RWSEL is logic 1, the working serial TelecomBus links are routed to the outgoing parallel TelecomBus. The protection serial TelecomBus links will only go as far as the RPPM blocks so the link integrity can be verified using PRBS patterns. When RWSEL is logic 0, the protection links will be routed to the outgoing parallel TelecomBus. The working serial TelecomBus links will only go as far as the RWPM blocks so that the link integrity can be verified using PRBS patterns.

The RWSEL is sampled when the RJ0FP signal is high. The switch between the working and protection links occurs at on the second transport frame boundary after the RWSEL is sampled as shown in Section 15.2.

The RWTSEN, RPTSEN and RATSEN register bits in the RWTI, RPTI and RATI Indirect Data registers, respectively, are used when RWSEL_EN is set to logic 0.

The RWTSEN, RPTSEN and RATSEN register bits allow selection of data from the working, protection, or auxiliary serial TelecomBus links on a per-STS-1 timeslot granularity to be routed to the outgoing TelecomBus interface. When RWTSEN is set high, the working serial TelecomBus link is selected for the corresponding timeslot. When RPTSEN is set high, the protection serial TelecomBus link is selected for the corresponding timeslot. When RATSEN is set high, the auxiliary serial TelecomBus link is selected for the corresponding timeslot. For each timeslot, one and only one of the RWTSEN, RPTSEN, and RATSEN register bit must be set high.

RWTSEN, RPTSEN and RATSEN changes take place at transport frame boundaries.

14.15 PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. With PRBS data and incrementing data patterns, the payload envelope is filled with pseudo-random/incrementing bytes with the exception of POH and fixed stuff columns. In the case of the incrementing counts, the count starts at 0 and increments to FFh before the count starts over at 0 once again. The incrementing count is free to float within the payload envelope and therefore the 0 count is not associated with any fixed location within a payload envelope. This PRBS generator and monitor is compatible with the PRBS generators and monitors in other CHESS™ Set devices. It may not be compatible with external test equipment.

The user has the option to monitor a programmable sequence in all the B1 byte positions. The complement of these values is also monitored in the E1 byte positions. This is used to check for mis-configuration of STS-1 cross-connect fabrics. If a known STS-1 originated from a particular STS-1 port, the source can be programmed to send a B1 pattern that would be monitored at the other end.

14.15.1 Mixed Payload (STS-12c, STS-3c, and STS-1)

Each PRGM is designed to process the payload of an STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1 paths) can be programmed to a granularity of an STS-1. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- three STS-1/STM-0 with three STS-3c/STM-1
- six STS-1/STM-0 with two STS-3c/STM-1
- nine STS-1/STM-0 with one STS-3c/STM-1.

The STS-1 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1). See Table 13 and Table 14 for more details.

14.15.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

In master/slave configuration of the monitor (processing STS-24c/VC-4-8c, STS-36c/VC-4-12c, STS-48c/VC-4-16c or STS-192c/VC-4-64c concatenated payloads) more bytes are needed to recover the LFSR state, because the slaves needs a few bytes to be synchronized with the J1 byte indicator.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

Out of Synchronization and Synchronized states are defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 3 consecutive bytes with errors. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization. It is important to note however that the monitor can falsely synchronize to an all zero pattern. If inverted PRBS is selected, the monitor can falsely synchronize to an all 1 pattern. It is therefore recommended that users poll the monitor's LFSR value after synchronization has been declared, to confirm that the value is neither all 1s or all 0s.

Upon detecting 3 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

14.15.3 Master/Slave Configuration for STS-48c/STM-16c Payloads

To monitor STS-48c/STM-16c payloads, a master/slave configuration is available where each monitor receives 1/4 of the concatenated stream. In the case of a STS-48c/STM-16c, 4 PRGMs are used in a master/slave configuration. Because the payload is four bytes interleaved, after a group of four consecutive bytes, a jump in the sequence takes place. The number of bytes that must be skipped can be determined using the number of PRGMs in the master/slave configuration. For example, to process an STS-48c/STM-16c, the number of sequence to skip is (4 PRGMS * 4 bytes) – 3 = 13. So, 13 sequences will be skipped after each group of four consecutive bytes.

The PRBS monitor can be re-initialize by the user by writing in a normal register of the master PRGM. Since all the slave PRGMs use the LFSR state of the previous PRGM in the chain, they will also be re-initialized.

14.15.4 Error Detection and Accumulation.

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect byte errors in the payload. A byte error is detected on a comparison mismatch of the two bytes. Only a single byte error is counted regardless of the number of erroneous bits in the byte. All byte errors are accumulated in a 16 bit byte error counter. The error counter will saturate at its maximum value of FFFFh, i.e. it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. The error counter is cleared when transferred into the registers and the accumulation restarts at zero. When reading error counts for concatenated payloads of STS-3c /STM-1c or STS-12c/STM-3c sizes, it is necessary to read the error count in all slices (all associated STS-1's). The majority of the error counts will be accumulated in the master slice when the error count transfer is initiated, but an error may be accumulated in a slave slice register if the error occurs during the transfer operation. In the case of STS-48c/STM-16c payloads, it is necessary to read the error count in all STS-1's of each PRGM in the group of 4 PRGMs associated with the STS-48c/STM-16c monitor. Since all STS-1 error counts belonging to a concatenated stream must be read for maximum accuracy, the error counts in each associated register must be totaled by software to obtain the error count for the concatenated stream. If this level of accuracy is not desired, software may choose to only read the error count for the master slice, with the risk of missing a small number of error counts on each accumulation operation. For each independent STS-1 monitored by a PRGM, the error count register for each individual STS-1 must be read.

Byte errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming the RESYNC register bit high, or once it detects 3 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated.

14.16 "J0" Synchronization of the TBS in a CHESS™ System

Any TSE/TBS fabric can be viewed as a collection of different stages. For example, a Time-Space-Time switch could be constructed with five datapath stages:

1. ingress load devices (e.g. SPECTRA-2488)
2. ingress TBS devices
3. TSE devices
4. egress TBS devices
5. egress load devices (e.g. SPECTRA-2488)

Note that in some cases, one physical device may serve in two stages, such as stages 1 and 5 or stages 2 and 4. STS-12 frames are pipelined through this fabric in a regular fashion, under control of a single clock frequency (77.76 MHz). In order to maintain valid framing for the group of STS-12 streams, the datapath devices must be coordinated with one another. The first step in this coordination is the use of a global frame synchronization pulse to mark the position of frame boundaries as they enter the fabric. However, since each device in the system datapath sees the STS-12 frames at a different latency than other devices, there must be a mechanism to account for the individual latencies at different points along the datapath.

The most significant source of delay is the cumulative latency of the devices that lie along the system datapath. To accommodate different system arrangements, a synchronization frame pulse and a programmable frame delay register are used to re-frame the STS-12 streams for each system datapath device. In the TBS, this FIFO is 24-words deep and is controlled by the RJ0FP pin along with the RJ0DLY register. This frame delay register is used to inform the TBS of the latency between a frame pulse on the RJ0FP pin and the presence of J0 characters in the FIFOs so that a re-framing mechanism can be triggered at the appropriate time. Because the J0 characters may lie at different FIFO depths, due to skew between links, this re-framing can be achieved by realigning the FIFO read pointers to match the J0 positions.

In addition to device latencies, there are other sources of delay. Furthermore, these delays may vary from link to link. For example, clock skew or differential trace lengths impose uneven delays on individual links. The 24-word depth of the FIFO allows these delays to be equalized as part of the re-framing process. When the RJ0FP-RJ0DLY trigger signals the occurrence of a frame boundary, the TBS will adjust the FIFO's read positions to realign the STS-12 streams' J0 characters with one another. As long as the J0 characters from all the STS-12 streams are indeed simultaneously present in their respective FIFOs when this occurs, the TBS will effectively re-align the streams as part of the re-framing process. The large FIFO depth allows the TBS to compensate for such differential delays as trace lengths that vary by several meters. Smaller delay variances, such as those due to clock jitter, can be absorbed automatically by the serial receive links. If they prove to be too large for such absorption, they will then be corrected through the FIFO re-framing process.

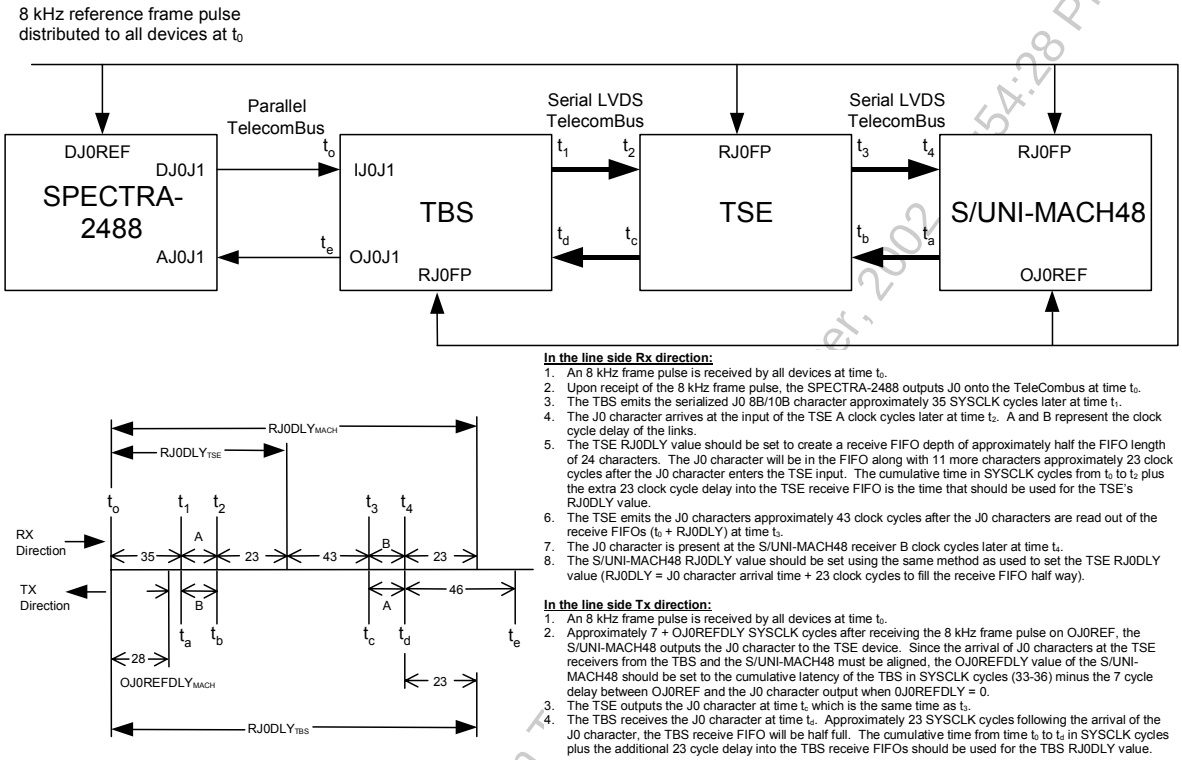
In order to guarantee that the RJ0FP-RJ0DLY trigger will happen when all streams' J0 characters are simultaneously present within the FIFOs, it is important to choose correct values for the frame delay register. The following example explains how frame delay register values are chosen for the devices of a sample system. Consider the implementation shown in Figure 15. All devices receive the global frame pulse simultaneously at time t0 (ignoring any trace length differentials). The SPECTRA-2488 emits the J0 byte onto the TelecomBus upon receiving the global frame pulse on the DJ0REF input. This action is entirely independent of receiving a J0 byte from the optical line. SPECTRA-2488 pointer adjustments will define the start of the payload envelope (the J1 byte indicates start of payload) and this payload will be output over the TelecomBus. The SPECTRA-2488 can be viewed as the master by which the synchronization of the other CHESS devices is determined. The TBS expects the four incoming eight bit 77.76 MHz TelecomBus data paths to be synchronized and upon processing emits the serialized data with J0 character approximately 35 clock cycles after receiving the J0 on the parallel TelecomBus. The J0 byte on each of the twelve independent 777.6 MHz LVDS links are not exactly simultaneous and may have a slight amount of skew relative to each other (because of presence of an 8 word FIFO on the LVDS transmitter output). The LVDS links are then mated to the TSE through a back-plane. The TSE is programmed (via indirect register access of the RJ0DLY[13:0] word) to expect the J0 byte a certain number of clock cycles after it receives the global frame pulse.

The ingress FIFOs permit a variable latency in J0 arrival of up to 16 clock cycles. That is, the largest tolerable delay between the slowest and fastest LVDS link of the 64 TSE LVDS links is 16 bytes. Consequently, the external system must ensure that the relative delays between all the 64 receive LVDS links be less than 16 bytes. The minimum value for the internal programmable delay (RJ0DLY[13:0]) is the delay to the last (slowest) J0 character plus 15 bytes. The maximum value is the delay to the first (fastest) J0 character plus 31 bytes. The actual programmed delay should be based on the delay of the "slowest" of the 64 links – the link in which J0 arrives last plus a small safety margin of 1 or 2 bytes. The magnitude of the clock cycle delay is bounded by two parameters. First, the programmed delay register RJ0DLY is 14 bits. This implies that a clock cycle delay of 214 –1 or 16,383 clock cycles can be programmed. However, the second parameter, the frame rate (125 µs), bounds the delay to one STS-12 frame or 9719 (9720 unique values but 0 is the value for no delay) clock cycles (125 µs x 77.76 MHz), after which the next SONET frame begins. The TSE, upon receiving the global frame pulse, will wait the programmed amount of time (56 clock cycles + cable length delays) before searching each of the 64 links for the location of the J0 pulse to initialize synchronization.

The number of clock cycles can be determined by simply adding the relevant device and cable length latencies. In practice, the programmed delay can be obtained by measuring the clock difference between the global 8kHz frame pulse and the presence of the J0 on the TJ0FP pin. The programmed delay is this clock cycle difference plus a few clock cycles for margin.

This synchronization mechanism is flexible enough to accommodate system paths with different cumulative device latencies. Consider a TSE that is mated to a S/UNI-MACH48 on one link and a SPECTRA-2488 feeding a TBS on the other link. The alternate data paths have different delays; the SPECTRA-2488/TBS link has a greater delay than the S/UNI-MACH48 link delay. In this case, the S/UNI-MACH-48 is programmed to emit the J0 pulse later than SPECTRA-2488 (but aligned with the TBS serial output) such that the J0 from both sources arrive at the TSE within the allowed 16-clock cycle window. The S/UNI-MACH48 programmed delay is 24 clock cycles after the receipt of the frame pulse.

Figure 15 "J0" Synchronization Control



In the line side Rx direction:

1. An 8 kHz frame pulse is received by all devices at time t_0.
2. Upon receipt of the 8 kHz frame pulse, the SPECTRA-2488 outputs J0 onto the TeleCombus at time t_0.
3. The TBS emits the serialized J0 8B/10B character approximately 35 SYSCLK cycles later at time t_1.
4. The J0 character arrives at the input of the TSE A clock cycles later at time t_2. A and B represent the clock cycle delay of the links.
5. The TSE RJ0DLY value should be set to create a receive FIFO depth of approximately half the FIFO length of 24 characters. The J0 character will be in the FIFO along with 11 more characters approximately 23 clock cycles after the J0 character enters the TSE input. The cumulative time in SYSCLK cycles from t_0 to t_2 plus the extra 23 clock cycle delay into the TSE receive FIFO is the time that should be used for the TSE's RJ0DLY value.
6. The TSE emits the J0 characters approximately 43 clock cycles after the J0 characters are read out of the receive FIFOs (t_0 + RJ0DLY) at time t_3.
7. The J0 character is present at the S/UNI-MACH48 receiver B clock cycles later at time t_4.
8. The S/UNI-MACH48 RJ0DLY value should be set using the same method as used to set the TSE RJ0DLY value (RJ0DLY = J0 character arrival time + 23 clock cycles to fill the receive FIFO half way).

In the line side Tx direction:

1. An 8 kHz frame pulse is received by all devices at time t_0.
2. Approximately 7 + OJ0REFDLY SYSCLK cycles after receiving the 8 kHz frame pulse on OJ0REF, the S/UNI-MACH48 outputs the J0 character to the TSE device. Since the arrival of J0 characters at the TSE receivers from the TBS and the S/UNI-MACH48 must be aligned, the OJ0REFDLY value of the S/UNI-MACH48 should be set to the cumulative latency of the TBS in SYSCLK cycles (33-36) minus the 7 cycle delay between OJ0REF and the J0 character output when 0J0REFDLY = 0.
3. The TSE outputs the J0 character at time t_c which is the same time as t_3.
4. The TBS receives the J0 character at time t_d. Approximately 23 SYSCLK cycles following the arrival of the J0 character, the TBS receive FIFO will be half full. The cumulative time from time t_0 to t_d in SYSCLK cycles plus the additional 23 cycle delay into the TBS receive FIFOs should be used for the TBS RJ0DLY value.

14.17 Initialization Procedure

The following is a suggested initialization procedure which may be helpful when writing initialization code for the TBS.

1. Set the TBS Master Incoming register to: TTSI_MODE=01, INCIPL =1, INCIJ0J1=1, IOP=0
   set addr 000h to 0016h

2. Set the TBS Master Outgoing register to: RTSI_MODE=01, INCOPL=1, INCOJ0J1=1, OOP=0, RWSEL_EN=0
   set addr 001h to 0016h

3. Set the CSU Control register to: CSU_ENB=0, CSU_RSTB=1
   set addr 500h to 040Fh

4. Ensure that the CSU shows stable "locked" status by reading registers 0x501 and 0x502.
   Read register 0x502 – expect to see 0x01 representing the interrupt from changes in lock state during reset.
   Read register 0x502 again – expect to see 0x00 indicating stable lock status.
   Read register 0x501 – expect to see LOCKV bit set to 1 indicating that the device is stable in the locked state.

5. After the CSU has locked, the transmit FIFOs must be re-centered since they will have suffered over-run or under-run conditions when the CSU was not locked. To re-center the FIFOs, write a 1 to the CENTER bit in the TWDE/TPDE/TADE Control and Status registers (0x130, 0x230, 0x330, 0x430, 0x140, 0x240, 0x340, 0x440, 0x150, 0x250, 0x350, 0x450).

6. Note the following steps (7 through 9) are required to set the analog sections of the LVDS receive paths to the correct operating defaults. Failure to set these registers correctly will result in an inability to receive LVDS data on the links in question.

7. Set the RW8D 1 – 4 Analog Control register to: DRU_ENB=0, RX_ENB=0 and tuning parameters as shown
   set addresses 163h, 263h, 363h, and 463h to CC34h

8. Set the RP8D 1 – 4 Analog Control register to: DRU_ENB=0, RX_ENB=0 and tuning parameters as shown
   set addresses 173h, 273h, 373h, and 473h to CC34h

9. Set the RA8D 1 – 4 Analog Control register to: DRU_ENB=0, RX_ENB=0 and tuning parameters as shown
   set addresses 183h, 283h, 383h, and 483h to CC34h

10. Set the TWTI, TPTI, and TATI time slot switching per section 14.13.

11. Set the RWTI, RPTI, and RATI time slot switching per section 14.12.

12. Set the TBS Master Receive Synchronization Delay at addr 005h per section 14.16.

13. Change the TTSI and RTSI modes in registers 000h and 001h to TSI_MODE= 00

14. Enable interrupts on the device by setting interrupt enable bits as described below:

    - Set register 000h to ------1111------b (where – indicates don't change and b indicates binary)
    - Set registers 008h, 009h, 00Ah, 00Bh, and 00Ch to FFFFh
    - Set registers 022h, 032h, 042h, 082h, 092h, 0A2h, and 501h to 00001h
    - Set registers 160h, 260h, 360h, and 460h to --------1111----b
    - Set registers 170h, 270h, 370h, and 470h to --------1111----b
    - Set registers 180h, 280h, 380h, and 480h to --------1111----b
    - Set registers 195h, 295h, 395h, and 495h to 0FFFh
    - Set registers 197h, 297h, 397h, and 497h to 0FFFh
    - Set registers 19Ah, 29Ah, 39Ah, and 49Ah to 0FFFh
    - Set registers 1A5h, 2A5h, 3A5h, and 4A5h to 0FFFh
    - Set registers 1A7h, 2A7h, 3A7h, and 4A7h to 0FFFh

- Set registers 1AAh, 2AAh, 3AAh, and 4AAh to 0FFFh
- Set registers 1B5h, 2B5h, 3B5h, and 4B5h to 0FFFh
- Set registers 1B7h, 2B7h, 3B7h, and 4B7h to 0FFFh
- Set registers 1BAh, 2BAh, 3BAh, and 4BAh to 0FFFh
- Set registers 130h, 230h, 330h, and 430h to ----------1----b
- Set registers 140h, 240h, 340h, and 440h to ----------1----b
- Set registers 150h, 250h, 350h, and 450h to ----------1----b
- Set registers 105h, 205h, 305h, and 405h to 0FFFh
- Set registers 107h, 207h, 307h, and 407h to 0FFFh
- Set registers 10Ah, 20Ah, 30Ah, and 40Ah to 0FFFh

14.18 Using the TBS with Low-Order Path Terminating Devices

While the TBS supports decoding of low-order path serial TelecomBus characters for diagnostic purposes, it is not a recommended use of the device.

The TBS does not support encoding of the ITV5[4:1], ITPL[4:1] and ITAIS[4:1] signals as special 8B/10B control characters, which is known as low-order path termination (LPT) encoding mode. These signals may be looped-back to the corresponding signals on the outgoing TelecomBus. This limitation does not compromise the capability of the TBS to receive and decode serial 8B/10B control characters and correctly generate the OTV5[4:1], OTPL[4:1] and OTAIS[4:1] signals for use by a tributary or low-order path processor for diagnostic purposes. It is not recommended that a TBS be used with a low-order path terminating device like the TUPP on the input TelecomBus other than for performance monitoring purposes. Any pointer processing done by the TUPP cannot be propagated by the TBS, and the processing may need to be redone at the far end of the serial link. The TBS can pass valid low-order tributary information when in HPT or MST mode, but it cannot propagate any out of band pointer processing or tributary alarm information.

The TBS can be used with a low-order path terminating/originating device on the output TelecomBus which is capable of receiving the V5 and tributary payload locations for the purpose of low-order pointer generation. This means the device can understand the OTV5 and OTPL signals, and use them to generate valid low-order path overhead. This is provided for diagnostic purposes, but is not a recommended mode of operation. It is recommended that low-order path processing devices be connected to the outgoing TBS TelecomBus to perform pointer interpretation and performance monitoring for downstream tributary processing devices, assuming that the V5 and tributary payload received by the TBS are valid.

14.19 On Using the Working, Protect and Auxiliary Receive Links Independently

Many applications will use the TBS in a situation where the Working and Protect ports are fully utilized with the Protect port providing redundancy for Working port. In some architectures however the LVDS receive links may be used independently with a single link providing redundancy for other individual links. This section explains how J0 pulses are generated so that designers can make informed decisions about independent receive link usage.

Details

The OJ0J1[4:1] outputs use the RJ0FP input to derive an appropriately delayed version of the J0 signal. Therefore a J0 pulse will be provided on the output at the correct time with respect to the payload signal OPL[4:1] every 125 us, regardless of the data received on the TBS serial links. The J0 8B/10B characters received on the serial links are used strictly for serial link framing, frame alignment, and internal uses, but do not control the outgoing TelecomBus control signals. If the device is used in a mode such that the received J0 characters would not propagate correctly to the outgoing TelecomBus, downstream devices will still receive a reference frame pulse based on RJ0FP. This is convenient since system timing is driven by RJ0FP, so the system has direct control over the outgoing TelecomBus J0 indication. This also allows the system designer the flexibility of using the transmit and receive serial links in a completely independent/equivalent fashion.

15 Functional Timing

15.1 Incoming Parallel TelecomBus to Transmit Serial TelecomBus

Figure 16 shows the timing of the Incoming parallel TelecomBus stream. Timing is provided by SYSCLK. SONET/SDH data is carried in the ID[*X*][7:0], where '*X*' denotes one of the four sections of the Incoming TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, ITPL[*X*] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IJ0J1[1] is set high with IPL[1] set low to mark the J0 byte of a transport frame. IJ0J1[4:2] are ignored when the corresponding IPL[4:2] is set low. IJ0J1[*X*] is set high with IPL[*X*] also set high to mark the J1 byte of all the streams within ID[*X*][7:0]. Tributary path frame boundaries are marked by a logic high on the ITV5[*X*] signal. High order streams in AIS alarm are indicated by the IPAIS[*X*] signal, while tributaries in AIS alarm are is indicated by the ITAIS[*X*] signal. The TCMP signal selects the active connection memory page in the Time-slot interchange blocks. It is only valid at the J0 byte position and is ignored at all other positions within the transport frame.

In Figure 16 below, STS-3/STM-1 numbers 1, 2, and 4 are configured for STS-3/AU3 operation. STS-3/STM-1 number 3 is configured for STS-3c/AU4 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on IPL[*X*] and IJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (IPAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by IJ0J1[*X*] being set high at byte S3,1/H3 and IPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 (STM-1 #4, AU3 #1) is configured to carry virtual tributaries/tributary units. The payload frame boundary of one such tributary is located at byte S4,1/B522, as marked by a high level on ITV5[*X*]. In addition, stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on IPL[*X*] at byte S4,1/B0. Stream S1,2 (STM-1 #1, AU3 #2) is also configured to carry virtual tributaries/tributary units. At byte S1,2/B0, ID[*X*][7:0] is shown to carry the V1 tributary overhead byte. Consequently, ITPL[*X*] is set low to indicate that the byte is not a tributary payload byte. At byte S2,2/B0, the tributary carried in stream S2,2 (2 (STM-1 #2, AU3 #2) is shown to be in tributary path AIS by the high level on ITAIS[*X*] signal. The arrangement shown in Figure 16 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 16 Incoming Parallel TelecomBus Timing

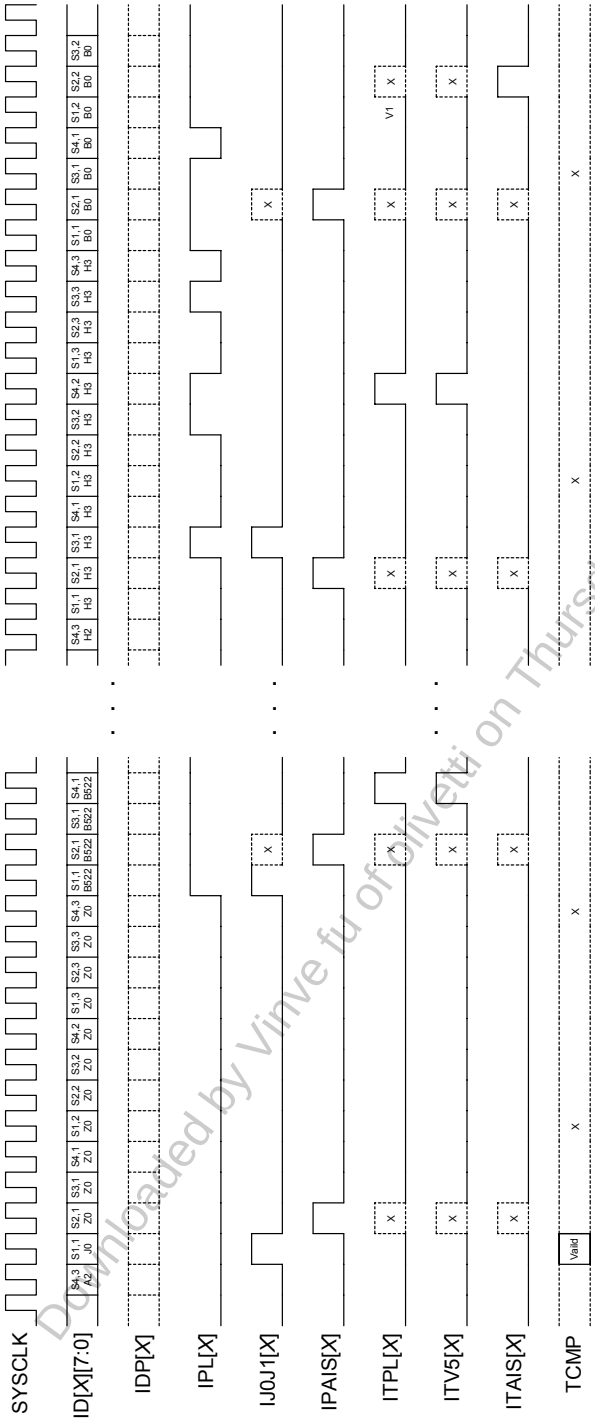
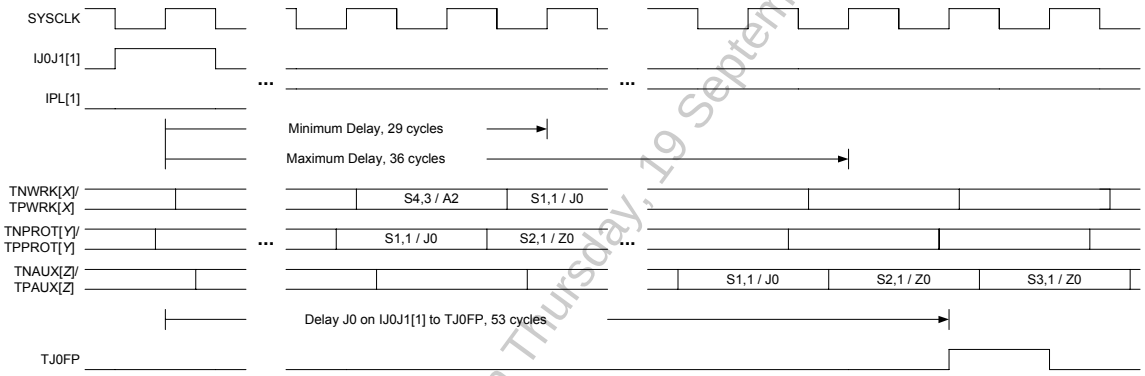


Figure 17 below shows the delay from the Incoming parallel TelecomBus stream to the transmit serial TelecomBus links. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 SYSCLK cycles. The minimum delay (29 SYSCLK cycles) is shown to be incurred by one of the transmit protection serial data links (TPPROT[*X*]/TNPROT[*X*]). The maximum delay (36 cycles) is shown to be incurred by one of the transmit auxiliary serial data links (TPAUX[*X*]/TNAUX[*X*]). TheTJ0FP identifies the time at which all the transmit serial links have transmitted their respective J0 characters. The relative phases of the links in Figure 17 are shown for illustrative purposes only. Links may have different delays relative to other members within each set – working, protection, and auxiliary, and relative to links in other sets than what is shown.

Figure 17 Incoming Parallel TelecomBus to Transmit Serial TelecomBus Timing



15.2 Receive Serial TelecomBus to Outgoing Parallel TelecomBus

Figure 18 below shows the relative timing of the receive serial TelecomBus links. Links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RJ0FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other (within a tolerance level of 24 byte times) but are frequency locked. The delay from RJ0FP being sampled high to the first and last J0 character is shown in Figure 18. In this example, the first J0 is delivered by one of the four protection links (RNPROT[4:1]/RPPROT[4:1]). The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, one of the auxiliary links is shown to be the slowest (RNAUX[4:1]/RPAUX[4:1]). The minimum value for the internal programmable delay (RJ0DLY[13:0]) is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 18 are shown for illustrative purposes only. Links may have different delays relative to other members within each set – working, protection and auxiliary, and relative to links in other sets than what is shown.

Figure 18 Receive serial TelecomBus Link Timing

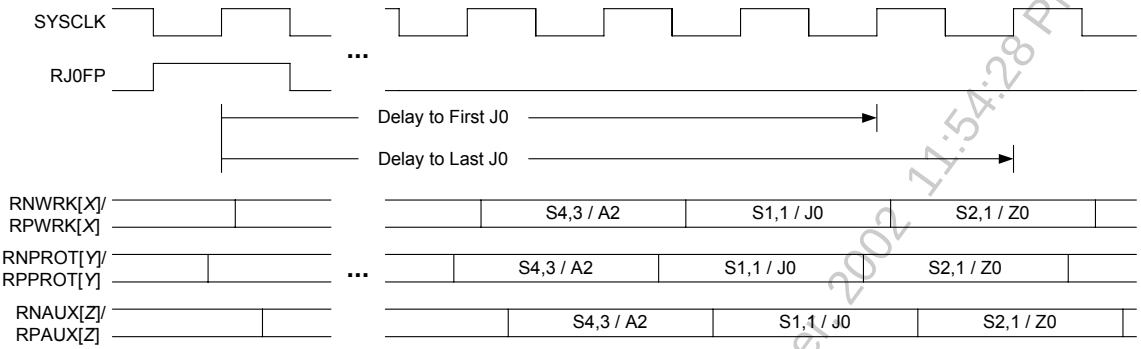


Figure 19 shows the timing relationships around the RJ0FP signal. The Outgoing Memory Page selection signal (OCMP) and the Receive Working Serial Data Select signal (RWSEL) are only valid at the SYSCLK cycle located by RJ0FP. They are ignored at all other locations within the transport frame. The delay from RJ0FP is to the J0 byte on the outgoing parallel TelecomBus stream is the sum of the value programmed into the RJ0DLY[13:0] register and processing delay of 29 SYSCLK cycles.

Figure 19 Outgoing TelecomBus Synchronization Timing

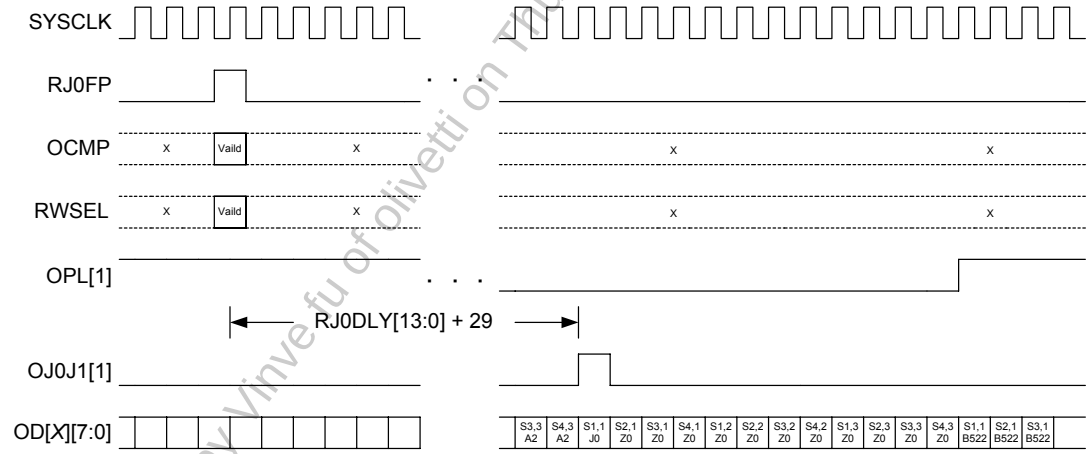
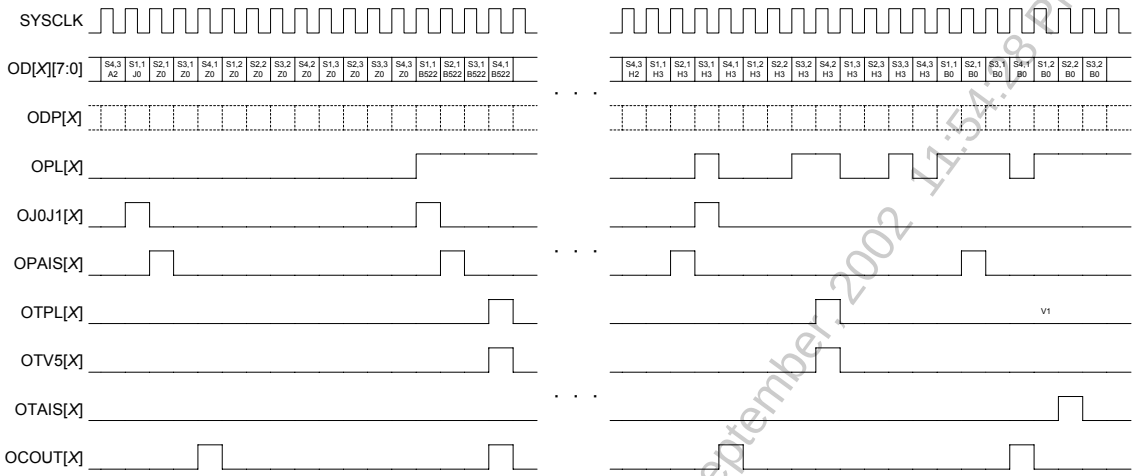


Figure 20 shows the timing of the Outgoing TelecomBus stream. Timing is provided by SYSCLK. SONET/SDH data is carried in the OD[*X*][7:0], where '*X*' denotes one of the four sections of the Outgoing TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, OTPL[*X*] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal All four OJ0J1[4:1] signals are set high with all four OPL[4:1] signals set low to mark the J0 byte of a transport frame. OJ0J1[*X*] is set high with OPL[*X*] also set high to mark the J1 byte of all the streams within OD[*X*][7:0]. Tributary path frame boundaries are marked by a logic high on the OTV5[*X*] signal. High order streams in AIS alarm are indicated by the OPAIS[*X*] signal, while tributaries in AIS alarm are indicated by the OTAIS[*X*] signal. OCOUT[*X*] is a software configurable output that is controllable on a per STS-1/AU3 basis.

In Figure 20 below, STS-3/STM-1 numbers 1, 2, and 4 are configured for STS-3/AU3 operation. STS-3/STM-1 number 3 is configured for STS-3c/AU4 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on OPL[*X*] and OJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (OPAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by OJ0J1[*X*] being set high at byte S3,1/H3 and OPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 (STM-1 #4, AU3 #1) is configured to carry virtual tributaries/tributary units. The payload frame boundary of one such tributary is located at byte S4,1/B522, as marked by a high level on OTV5[*X*]. In addition, stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on OPL[*X*] at byte S4,1/B0. Stream S1,2 (STM-1 #1, AU3 #2) is also configured to carry virtual tributaries/tributary units. At byte S1,2/B0, OD[*X*][7:0] is shown to carry the V1 tributary overhead byte. Consequently, OTPL[*X*] is set low to indicate that the byte is not a tributary payload byte. At byte S2,2/B0, the tributary carried in stream S2,2 (2 (STM-1 #2, AU3 #2) is shown to be in tributary path AIS by the high level on OTAIS[*X*] signal. Stream S4,1 is configured to output a high level on OCOUT[*X*]. The arrangement shown in Figure 20 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 20 Outgoing TelecomBus Timing



16 Absolute maximum ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions. Note: if a voltage is applied to an input pin when the device is powered down, the current needs to be limited below 20mA and the maximum voltage rating does not apply.

Table 15 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (VDDI, AVDL, CSU_AVDL)	-0.3V to +2.5V
3.3V Supply Voltage (VDDO, AVDH, CSU_AVDH)	-0.3V to +4.6V
Input Pad Tolerance	-2V < VDDO < +2V for 10ns, 100mA max
Output Pad Overshoot Limits	-2V < VDDO < +2V for 10ns, 20mA max
Voltage on Any Digital Pin	-0.5V to V_{VDDO}+0.5V
Voltage on LVDS Pin	-0.5V to Avdh+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current on RN[I], RP[I], TN[I], TP[I] pins	±90 mA
Latch-Up Current	±100 mA except RN[I], RP[I], TN[I], TP[I], and RESK
Latch-Up Current on RESK pin	±50 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

17 Power Information

17.1 Power Requirements

Table 16 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
All serial links, parallel buses, PRBS generators and PRBS monitors running.	IDDOP (VDDI)	0.828	—	1.030	A
	IDDOP (VDDO)	0.143	—	0.211	A
	IDDOP (AVDL)	0.161	—	0.210	
	IDDOP (AVDH)	0.172	—	0.200	A
	Total Power	2.82	3.24	—	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, Tj=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system.
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current. Outputs are assumed to be loaded with 30pF (if not otherwise specified).
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.
4. High power values are a “normal high power” estimate, calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: Tj=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics.

17.2 Power Sequencing

Due to ESD protection structures in the TBS pads it is necessary to exercise caution when powering the IC up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. The 1.8 V supplies can be brought up at the same time or after the 3.3 V supplies as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.

2. Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

3. Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA *.

There are no power-up ramp rate restrictions.

The TBS must be powered down according to the same restrictions above.

* These rules are intended to allow for hot-swap of LVDS signals, as the differential links are appropriately current-limited.

17.3 Power Supply Filtering

For detailed information on power supply filtering, which supercedes the initial recommendations given below, please refer to PMC document number PMC-2012540, TBS Power Supply Filtering Guidelines.

The following power supply filtering is recommended to achieve maximum power supply noise tolerance.

CSU_AVDH: 3.3 ohm, 100nF, 10nF

CSU_AVDL[2:0]: 0.47 ohm, 4.7 uF, 10nF (requires one filter per pin)

AVDH[6:0]: 3.3 ohm, 1.0uF, 10nF (can be paired up - maximum of 2 per filter)

AVDL[2:0]: 0 ohm, 100nF, 10nF

18 D. C. Characteristics

T_a = -40°C to T_j = +125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%
(Typical Conditions: T_C = 25°C, V_{VDDI} = 1.8V, V_{AVDL} = 1.8V, V_{CSU_AVDL} = 1.8V
V_{VDDO} = 3.3V, V_{AVDH} = 3.3V, V_{CSU_AVDH}= 3.3V)

Table 17 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	1.71	1.8	1.89	Volts	
V_{VDDO}	Power Supply	3.14	3.3	3.46	Volts	
V_{AVDL}	Power Supply	1.71	1.8	1.89	Volts	
V_{AVDH}	Power Supply	3.14	3.3	3.46	Volts	
V_{CSU_AVDH}	Power Supply	3.14	3.3	3.46	Volts	
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at VDDO=3.14V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	2.7		Volts	Guaranteed output High voltage at VDDO=3.14V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.2			Volts	Applies to RSTB, TRSTB and SYSCLK only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB and SYSCLK only.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB and SYSCLK only.
I_{ILPU}	Input Low Current	-200	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DDO}. Notes 2 and 3.
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
R_{IN}	LVDS Differential Input Impedance	85	100	115	Ω	

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	85	110	115	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Input pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

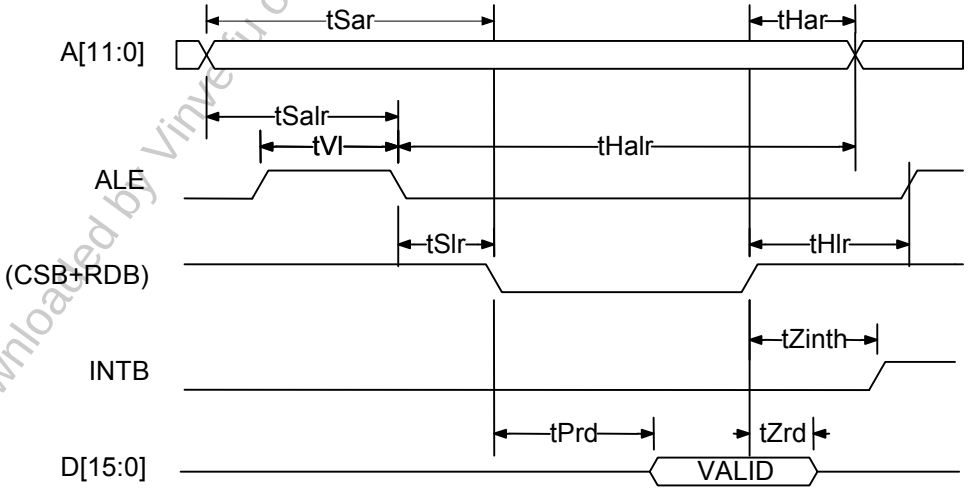
19 Microprocessor Interface Timing Characteristics

(T_a = -40°C to T_j = +125°C, V_{DDI} = $VDDI_{typical}$ ± 5%, V_{DDO} = $VDDO_{typical}$ ± 5%)

Table 18 Microprocessor Interface Read Access (Figure 21)

Symbol	Parameter	Min	Max	Units
tSar	Address to Valid Read Set-up Time	10		ns
tHar	Address to Valid Read Hold Time	5		ns
tSalr	Address to Latch Set-up Time	10		ns
tHalr	Address to Latch Hold Time	10		ns
tVl	Valid Latch Pulse Width	5		ns
tSlr	Latch to Read Set-up	0		ns
tHlr	Latch to Read Hold	5		ns
tPrd	Valid Read to Valid Data Propagation Delay		70	ns
tZrd	Valid Read Negated to Output Tri-state		20	ns
tZinth	Valid Read Negated to INTB Tri-state		50	ns

Figure 21 Microprocessor Interface Read Timing



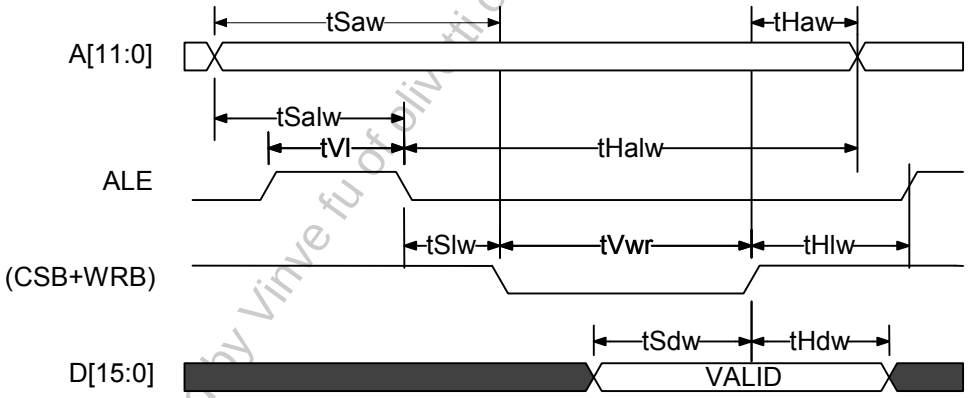
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_{L}, tS_{LR}, and tH_{LR} are not applicable.
5. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 19 Microprocessor Interface Write Access (Figure 22)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{AD}	Address to Valid Write Hold Time	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 22 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameters tH_{AW} and tS_{AN} are not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

20 A.C. timing Characteristics

(T_a = -40°C to T_j = +125°C, V_{DD} = $VDD_{typical}$ ± 5%)

20.1 Serial TelecomBus Interface

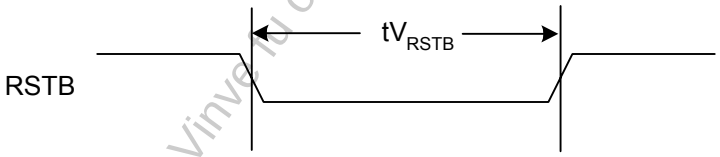
Symbol	Description	Min	Typical	Max	Units
f_{RLVDS}	RPWRK[4:1], RNWRK[4:1], RPPROT[4:1], RNPROT[4:1], RPAUX[4:1], RNAUX[4:1] Bit Rate	$10f_{SYSCLK}$	$10f_{SYSCLK}$	$10f_{SYSCLK}$	Mbps
t_{FALL}	V_{ODM} fall time, 80%-20%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
t_{RISE}	V_{ODM} rise time, 20%-80%, (R_{LOAD}=100Ω ±1%)	200	300	400	ps
t_{SKEW}	Differential Skew			50	ps

20.2 Reset Timing

Table 20 RSTB Timing (Figure 23)

Symbol	Parameter	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 23 RSTB Timing



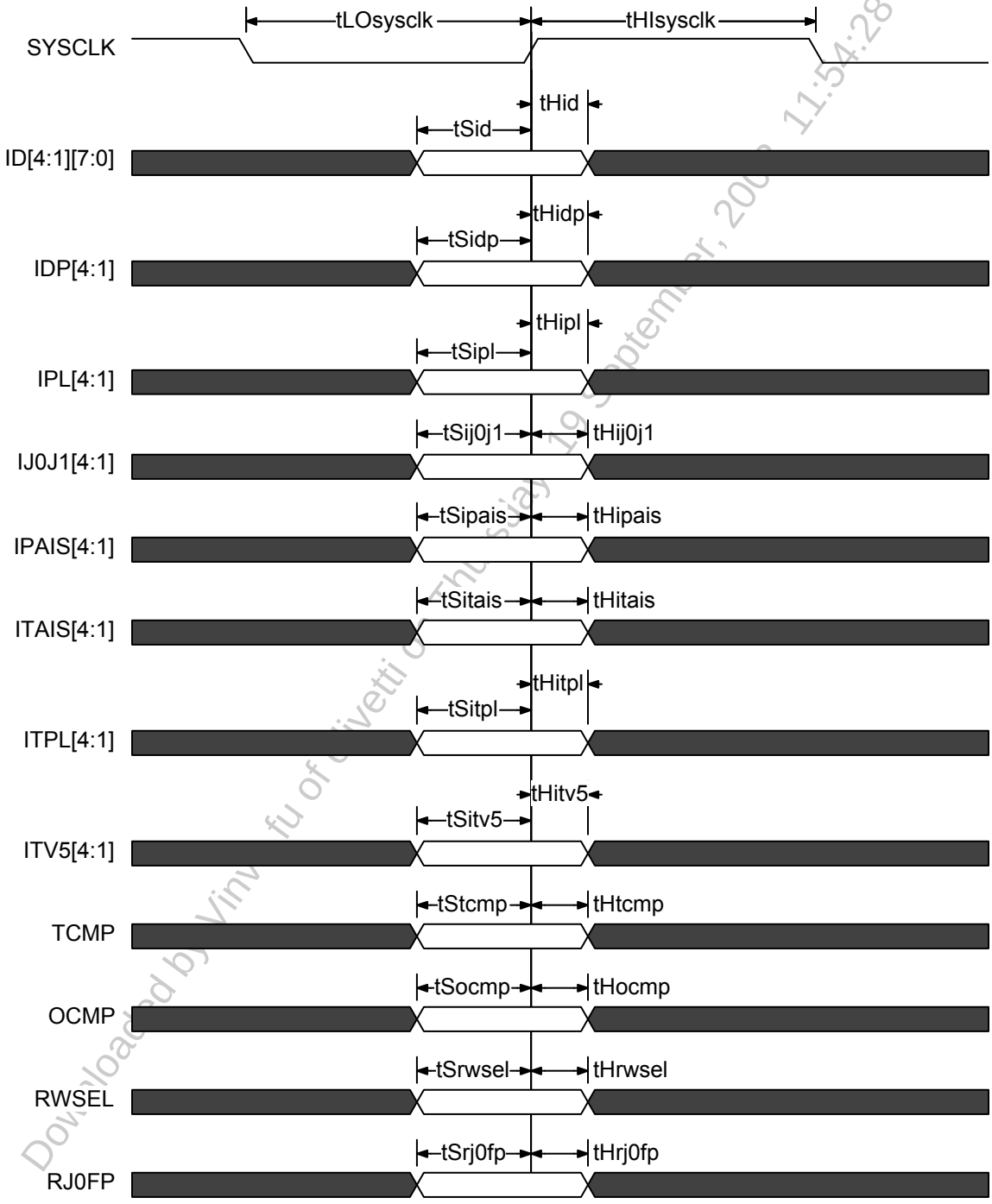
20.3 Parallel TelecomBus Interface

Table 21 TBS Incoming TelecomBus Timing (Figure 24)

Symbol	Description	Min	Max	Units
F_{SYSCLK}	SYSCLK Frequency (nominally 77.76 MHz)	77	78	MHz
THI_{SYSCLK}	SYSCLK HI pulse width	5		Ns
TLO_{SYSCLK}	SYSCLK LO pulse width	5		Ns
TS_{ID}	ID[4:1][7:0] Set-up Time	3		ns

Symbol	Description	Min	Max	Units
TH_{ID}	ID[4:1][7:0] Hold Time	0		ns
TS_{IDP}	IDP[4:1] Set-up Time	3		ns
TH_{IDP}	IDP[4:1] Hold Time	0		ns
tS_{IPL}	IPL[4:1] Set-Up Time	3		ns
tH_{IPL}	IPL[4:1] Hold Time	0		ns
tS_{IJ0J1}	IJ0J1[4:1] Set-Up Time	3		ns
tH_{IJ0J1}	IJ0J1[4:1] Hold Time	0		ns
tS_{IPAIS}	IPAIS[4:1] Set-Up Time	3		ns
tH_{IPAIS}	IPAIS[4:1] Hold Time	0		ns
tS_{ITAIS}	ITAIS[4:1] Set-Up Time	3		ns
tH_{ITAIS}	ITAIS[4:1] Hold Time	0		ns
tS_{ITPL}	ITPL[4:1] Set-Up Time	3		ns
tH_{ITPL}	ITPL[4:1] Hold Time	0		ns
tS_{ITV5}	ITV5[4:1] Set-Up Time	3		ns
tH_{ITV5}	ITV5[4:1] Hold Time	0		ns
tS_{TCMP}	TCMP Set-Up Time	3		ns
tH_{TCMP}	TCMP Hold Time	0		ns
tS_{OCMP}	OCMP Set-Up Time	3		ns
tH_{OCMP}	OCMP Hold Time	0		ns
TS_{RWSEL}	RWSEL Set-Up Time	3		ns
TH_{RWSEL}	RWSEL Hold Time	0		ns
tS_{RJ0FP}	RJ0FP Set-Up Time	3		ns
tH_{RJ0FP}	RJ0FP Hold Time	0		ns

Figure 24 Incoming TelecomBus Timing



Notes on Input Timing:

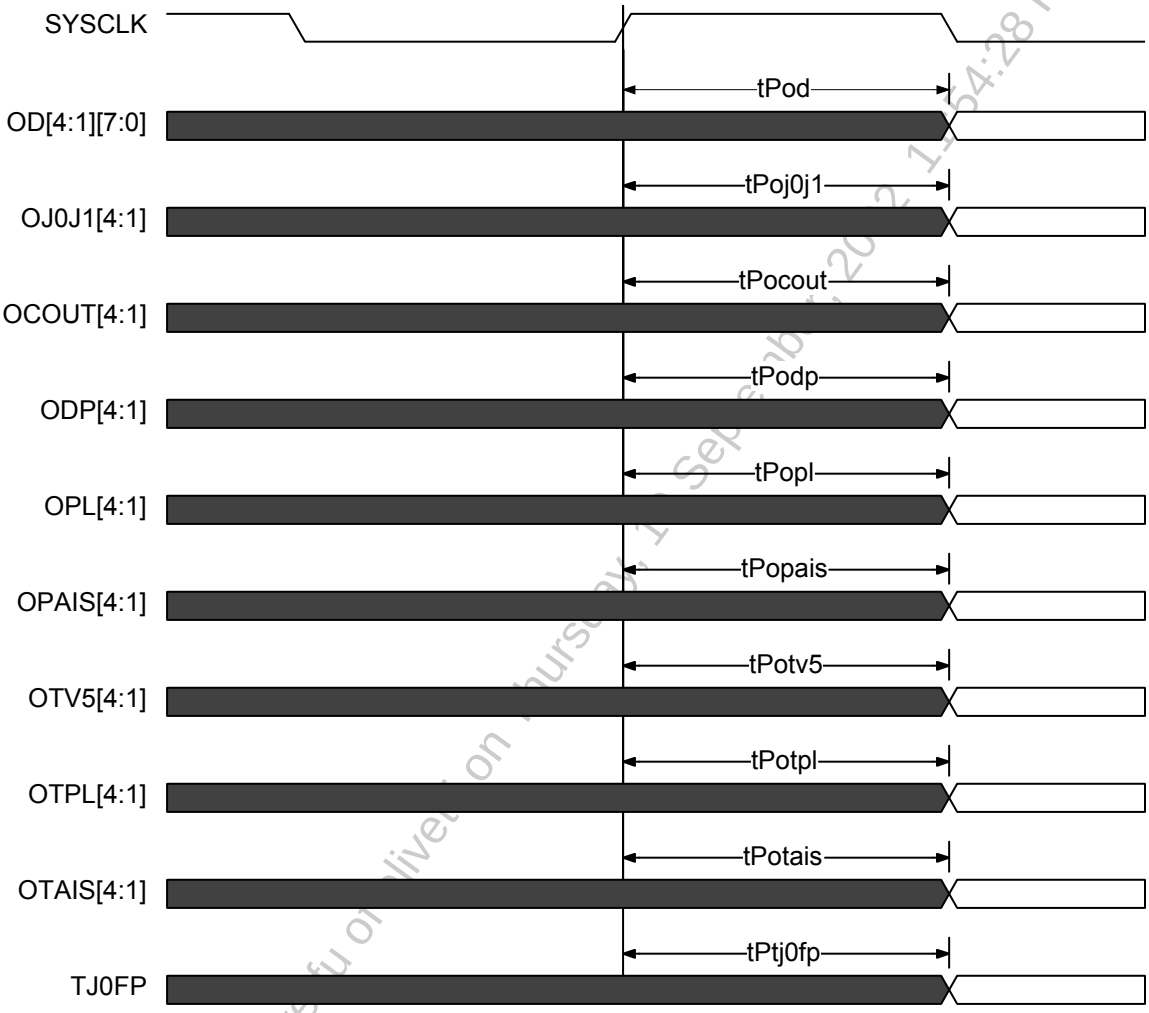
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 22 Outgoing TelecomBus Timing (Figure 25)

Symbol	Description	Min	Max	Units
tP_{OD}	SYSCLK High to OD[7:0] Valid	1	7	ns
tP_{OJ0J1}	SYSCLK High to OJ0J1[4:1] Valid	1	7	ns
tP_{OCOUT}	SYSCLK High to OCOUT[4:1] Valid	1	7	ns
TP_{ODP}	SYSCLK High to ODP[4:1] Valid	1	7	ns
tP_{OPL}	SYSCLK High to OPL[4:1] Valid	1	7	ns
TP_{OPAIS}	SYSCLK High to OPAIS[4:1] Valid	1	7	ns
tP_{OTV5}	SYSCLK High to OTV5[4:1] Valid	1	7	ns
tP_{OTPL}	SYSCLK High to OTPL[4:1] Valid	1	7	ns
tP_{OTAIS}	SYSCLK High to OTAIS[4:1] Valid	1	7	ns
tP_{TJ0FP}	SYSCLK High to TJ0FP Valid	1	7	ns

Figure 25 Outgoing TelecomBus Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except where indicated.

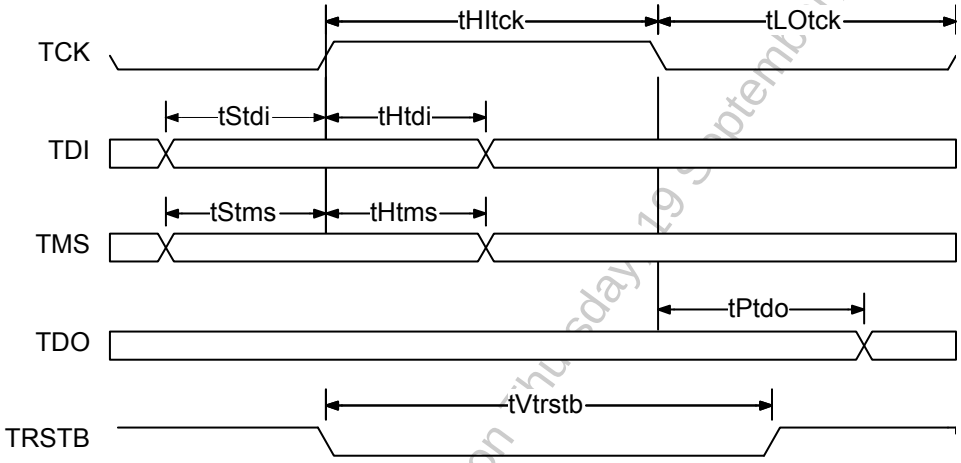
20.4 JTAG Port Interface

Table 23 JTAG Port Interface (Figure 26)

Symbol	Description	Min	Max	Units
F_{TCK}	TCK Frequency		4	MHz
tHI_{tck}	TCK HI Pulse Width	100		ns
tLO_{tck}	TCK LO Pulse Width	100		ns
tS_{tms}	TMS Set-up time to TCK	25		ns

Symbol	Description	Min	Max	Units
tH_{tms}	TMS Hold time to TCK	25		ns
tS_{tdo}	TDI Set-up time to TCK	25		ns
tH_{tdi}	TDI Hold time to TCK	25		ns
tP_{tdo}	TCK Low to TDO Valid	2	35	ns
tV_{trstb}	TRSTB Pulse Width	100		ns

Figure 26 JTAG Port Interface Timing



21 Ordering Information

PART NO.	DESCRIPTION
PM5310-BI	352 Ultra Ball Grid Array (UBGA)

22 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 24 Outside Plant Thermal Information

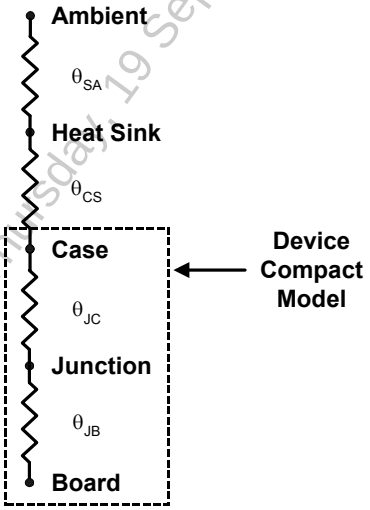
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 25 Device Compact Model[3]

θ_{JC}	0.3 °C/W
θ_{JB}	10.1 °C/W

Table 26 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	[(105-70)/P]-θ_{JC} °C/W[5]
θ_{SA} and θ_{CS} are required for long-term operation	

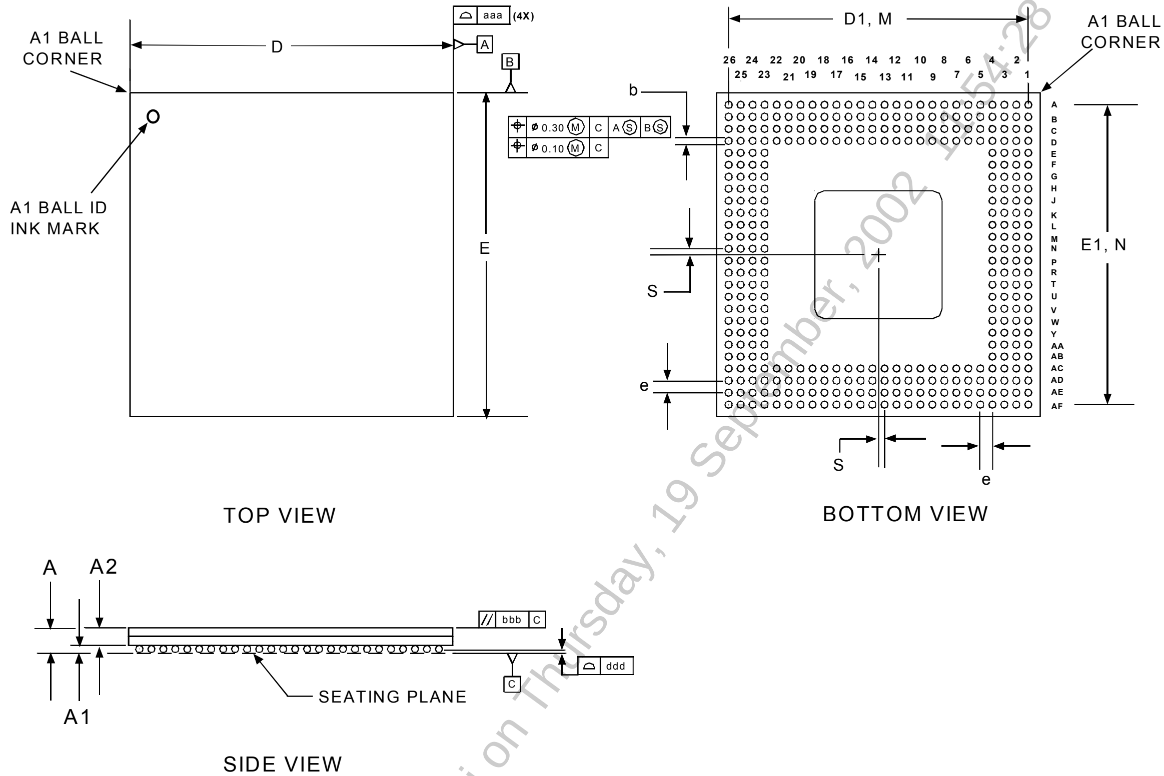


Operating power is dissipated in the package at the worst-case power supply. Power depends upon the operating mode. Please refer to 'High' power values in section 17.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.
3. junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place
5. In this formula P is the operating power.

23 Mechanical Information



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 352 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 27 x 27 x 1.41 MM																
Dim.	A	A1	A2	D	D1	E	E1	M,N	b	d	e	aaa	bbb	ddd	S	
Min.	1.26	0.40	0.86	26.90	-	26.90	-	-	0.50	-	-	-	-	-	0.45	
Nom.	1.41	0.50	0.91	27.00	25.00	27.00	25.00	26x26	0.63	-	1.00	-	-	-	0.56	
Max.	1.56	0.60	0.96	27.10	-	27.10	-	-	0.70	0.20	-	0.20	0.25	0.20	0.55	