P54/74FCT3646C/D—P54/74FCT3648C/D
3.3 VOLT OCTAL TRANSCEIVER/REGISTER

FEATURES

- Function and Drive Compatible with the Fastest TTL Logic
- Inputs and Outputs Interface with TTL Logic Levels
- 3.3V ± 0.2V Power Supply and CMOS for Lowest Power Dissipation
- FCT3-D speed at 4.6ns max. (Com'l)
  FCT3-C speed at 5.4ns max. (Com'l)
- Edge-rate Control Circuitry for Significantly Improved Switching Characteristics
- ESD protection exceeds 2000V
- 64 mA Sink Current (Com'l), 48 mA (Mil)
  15mA Source Current (Com'l), 12 mA (Mil)
- Multiple Center Power and Ground Pins
- Input Clamp Diodes to Limit Bus Reflections
- Independent Register for A and B Buses
- Choice of Non-Inverting and Inverting Data Paths
- Multiplexed Real-Time and Stored Data Transfer
- 3-State Output
- Manufactured in 0.4 micron PACE Technology™

DESCRIPTION

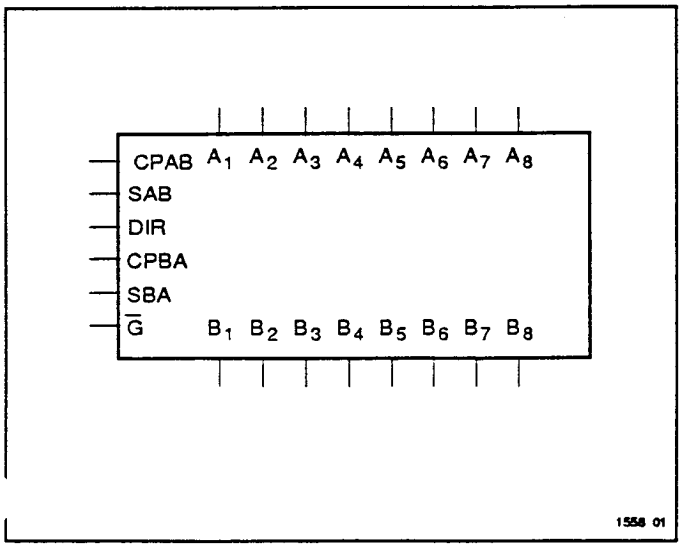
The 'FCT3646 and 'FCT3648 consist of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function.

In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

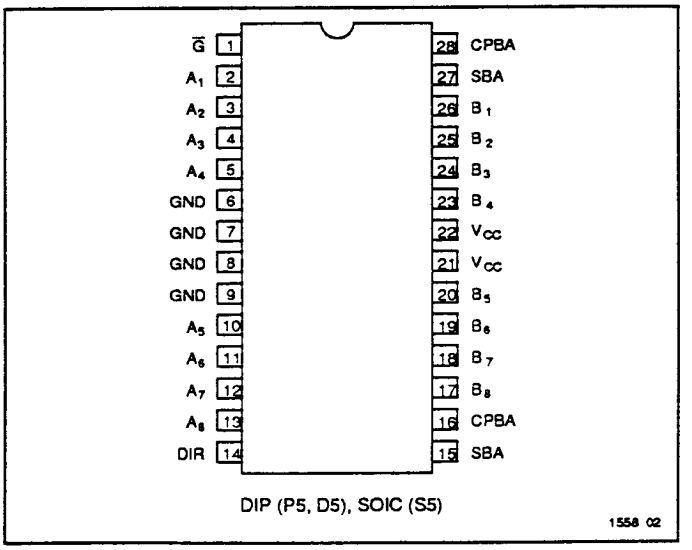
The 'FCT3646 and 'FCT3648 are manu-factured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply voltage is reduced from the conven-tional 5.0V to 3.3V, thus reducing output swings dramat-ically. This, together with the (lower inductance) center power and ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high-speed circuitry.

*For a fan-in/fan-out of 4 at 85°C junction temperature and a 3.3V power supply.

LOGIC SYMBOL



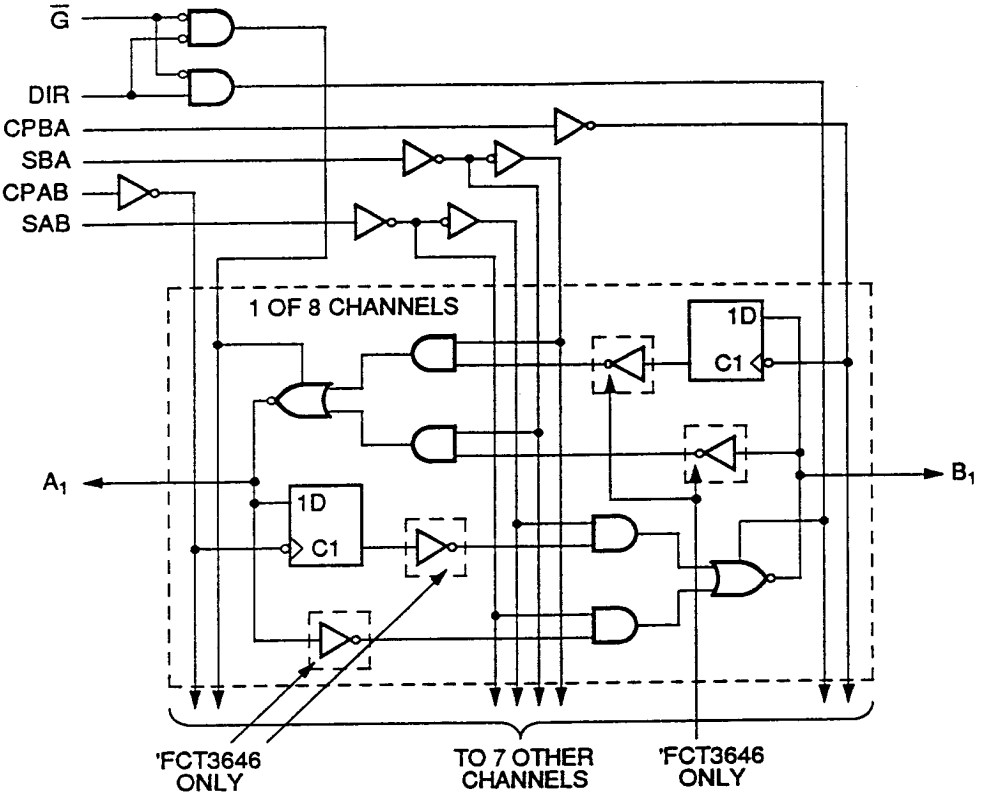
PIN CONFIGURATIONS



PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTION

Pin Names	Description
A_1–A_8	Data Register A Inputs Data Register B Outputs
B_1–B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$, DIR	Output Enable Inputs

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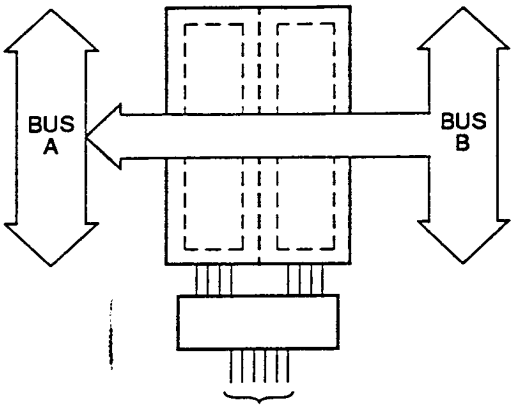
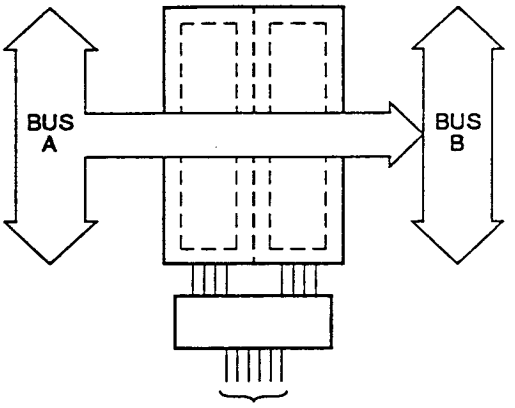


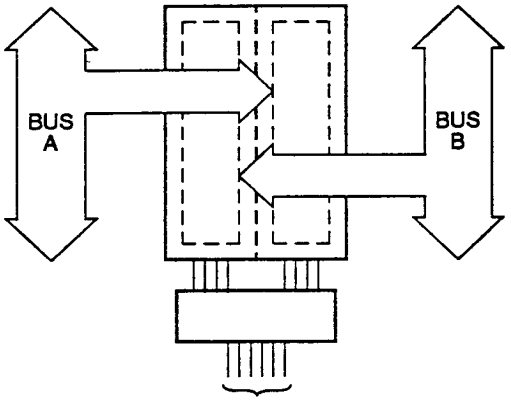
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



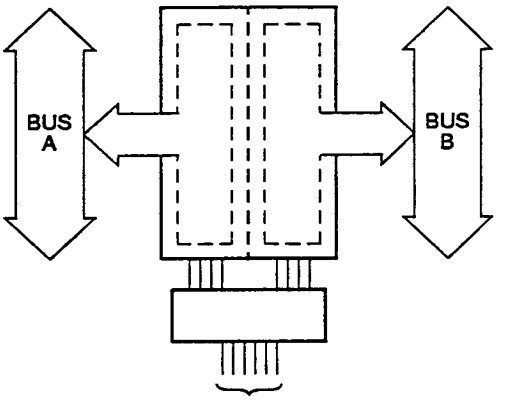
DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
H	L	↓	X	X	X
L	L	X	↓	X	X
X	H	↓	↓	X	X

STORAGE FROM
A AND/OR B



DIR[1]	$\overline{G}$	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED
DATA TO A AND/OR B

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Note:
1. Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLE

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT3646	'FCT3648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↓	↓	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

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Notes:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↓ = LOW-to-HIGH Transition

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +5.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+3.1V	+3.5V
Commercial		

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.55	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF		All I/Os

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Notes:

1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, $V_{IN} = V_{CC} - 0.6V$[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]		1.7	4.0 mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND
			7.0	12.8[4] mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} = V_{CC} - 0.6V$ or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
2. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} * D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT3646C/3648C				'FCT3646D/3648D				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	1.5	5.4	1.5	4.6	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A or B	1.5	6.3	1.5	5.7	1.5	5.7	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	1.5	7.0	1.5	6.2	1.5	6.2	1.5	5.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	8.9	1.5	7.8	1.5	7.8	1.5	6.6	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.7	1.5	6.3	1.5	6.3	1.5	5.4	ns	1, 5

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Note:
1. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT3646C/3648C				'FCT3646D/3648D				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	2.0	—	1.7	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	1.5	—	1.5	—	1.5	—	1.3	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	5.0	—	5.0	—	5.0	—	4.3	—	ns	5

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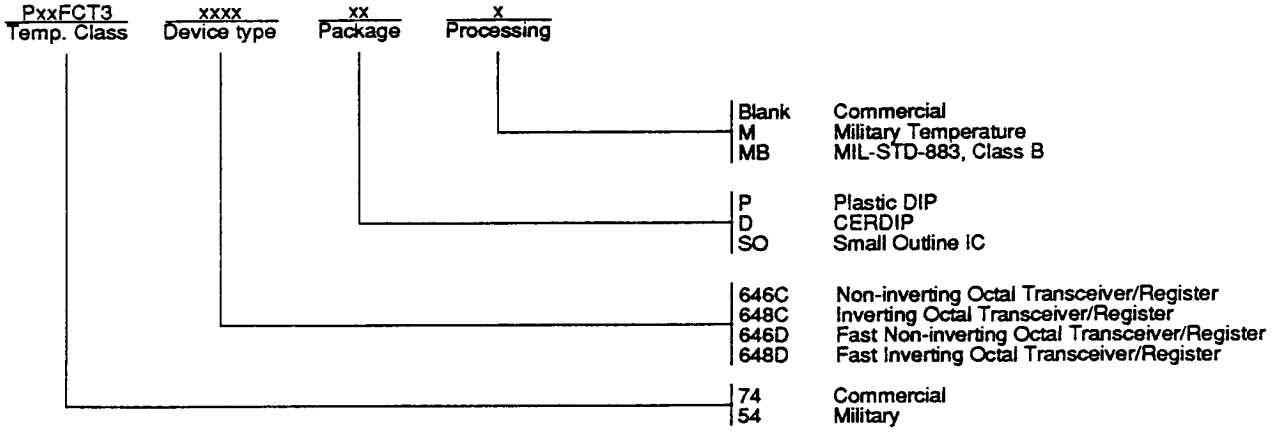
Note:
1. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION



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