HD49322BF

CDS/AGC & 10 Bit A/D Converter

HITACHI

ADE-207-260 (Z)
1st Edition
July 1998

Description

The HD49322BF is a CMOS IC that provides CCD-AGC analog processing (CDS/AGC) suitable for CCD camera digital signal processing systems together with a 10-bit A/D converter in a single chip.

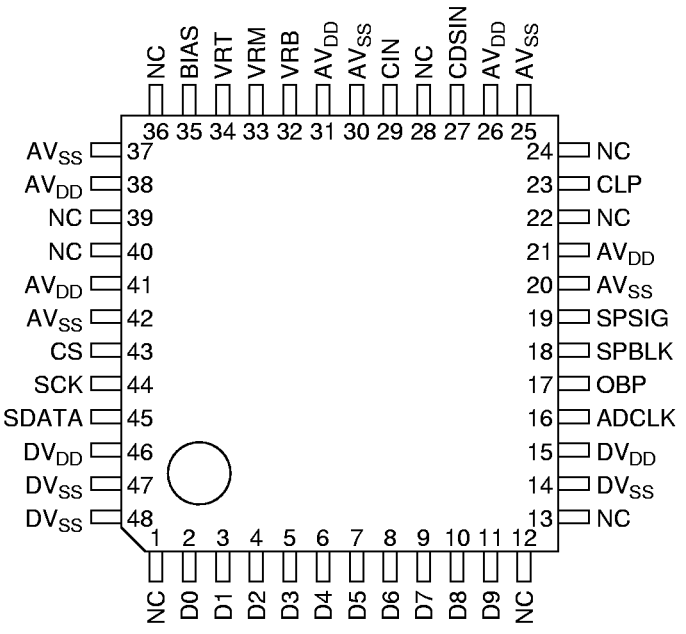
Functions

- Correlated Double Sampling
- AGC
- Sample hold
- Offset compensation
- Serial interface control
- 10 bit-ADC
- 3 V single operation
- Power dissipation: 192 mW (Typ)
- Maximum frequency: 18 MHz (Min)
- ADC direct input mode (chroma input mode only can be used)

Features

- Good suppression of CCD output low-frequency noise is achieved through the use of S/H type correlated double sampling.
- A high S/N ratio is achieved through the use of a AGC type amplifier, and high sensitivity is provided by a wide cover range.
- An auto offset circuit provides compensation of output DC offset voltage fluctuations due to variations in AGC amplifier gain.
- AGC, standby mode, offset control, etc., is possible via a serial interface.
- High precision is provided by a 10-bit-resolution A/D converter.

Pin Arrangement



(Top view)

Pin Description

Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
1	NC	No connection pin	—	—
2	D0	Digital output (LSB)	O	D
3 to 10	D1 to D8	Digital output	O	D
11	D9	Digital output (MSB)	O	D
12, 13	NC	No connection pin	—	—
14	DV_{SS}	Digital ground (0 V)	—	D
15	DV_{DD}	Digital power supply (3 V) Connect off-chip in common with AV_{DD}.	—	D
16	ADCLK	ADC conversion clock input pin	I	D
17	OBP	Optical black pulse input pin	I	D
18	SPBLK	Black level sampling clock input pin	I	D
19	SPSIG	Signal level sampling clock input pin	I	D
20	AV_{SS}	Analog ground (0 V)	—	A
21	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
22	NC	No connection pin	—	—
23	CLP *1	Clamp voltage pin	—	A
24	NC	No connection pin	—	—
25	AV_{SS}	Analog ground (0 V)	—	A
26	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
27	CDSIN	CDS input pin	I	A
28	NC	No connection pin	—	—
29	CIN	Chroma signal input pin	I	A
30	AV_{SS}	Analog ground (0 V)	—	A
31	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
32	VRB	Reference voltage pin 3 Connect a 0.1 µF ceramic capacitor between VRB and AV_{SS}.	—	A
33	VRM	Reference voltage pin 2 Connect a 0.1 µF ceramic capacitor between VRB and AV_{SS}.	—	A
34	VRT	Reference voltage pin 1 Connect a 0.1 µF ceramic capacitor between VRB and AV_{SS}.	—	A

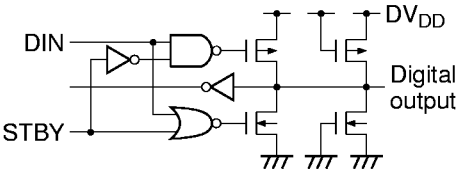
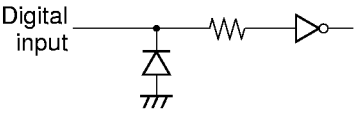
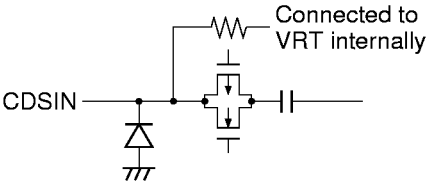
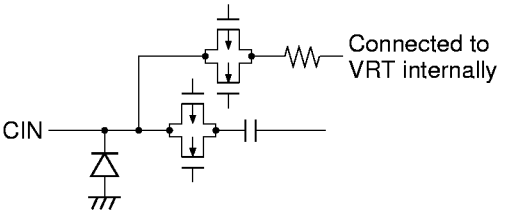
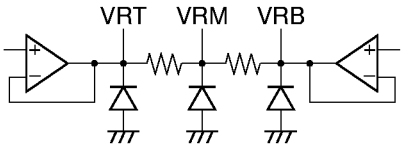
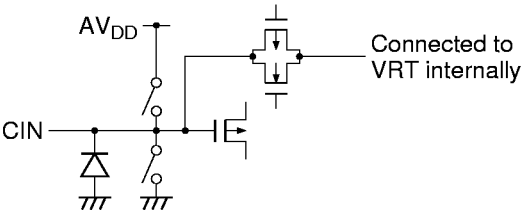
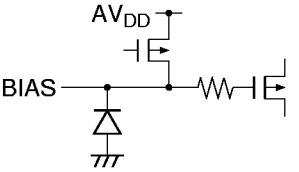
Note: 1. CLP is the clamp voltage pin; a capacitor of 1 µF or more should be connected between this pin and AV_{SS}.

Pin Description (cont)

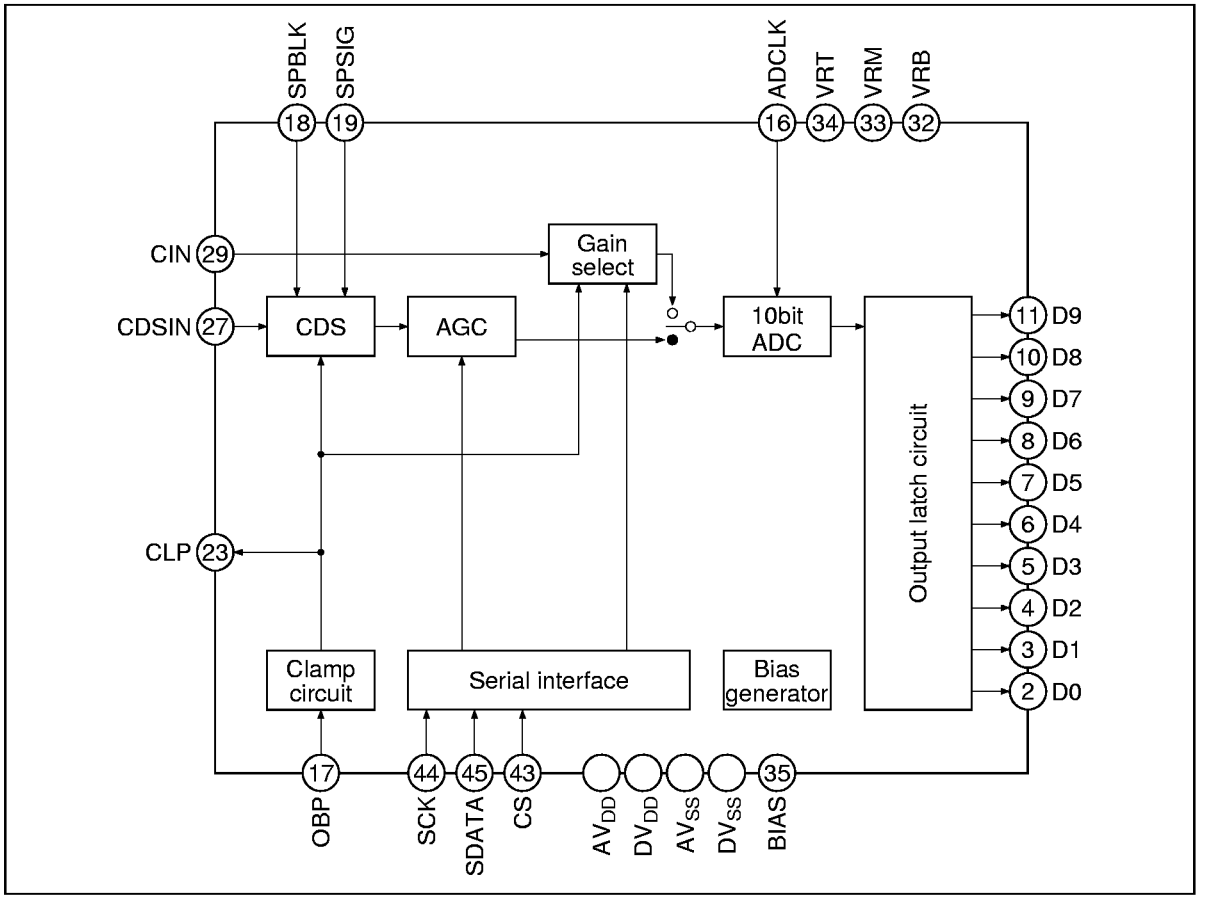
Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
35	BIAS *2	Internal bias pin	—	A
36	NC	No connection pin	—	—
37	AV_{SS}	Analog ground (0 V)	—	A
38	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
39, 40	NC	No connection pin	—	—
41	AV_{DD}	Analog power supply (3 V) Connect off-chip in common with DV_{DD}.	—	A
42	AV_{SS}	Analog ground (0 V)	—	A
43	CS	Serial interface control input pin	I	D
44	SCK	Serial clock input pin	I	D
45	SDATA	Serial data input pin	I	D
46	DV_{DD}	Digital power supply (3 V) Connect off-chip in common with AV_{DD}.	—	D
47, 48	DV_{SS}	Digital ground (0 V)	—	D

Note: 2. A resistor (24 kΩ) should be connected between BIAS and AV_{SS} off-chip for internal bias setting.

Input/Output Equivalent Circuit

Pin Name		Equivalent Circuit
Digital output	D0 to D9	
Digital input	ADCLK OBP SPBLK SPSIG CS SCK SDATA	
Analog input	CDSIN	
	CIN	
Reference voltage input	VRT VRM VRB	
Clamp	CLP	
Internal bias	BIAS	

Block Diagram



Internal Functions

Functional Description

- CDS (Correlated Double Sampling) circuit
- AGC gain selection (10 bit digital control) *
- ADC direct input selection *
  — 9-bit gain adjustment possible between 0.625 times (–4.1 dB) and 4.617 times (13.3 dB)
  — Chroma signal mode: input signal center level clamped at 512 LSB (Typ)
- CDS, AGC, and ADC automatic offset adjustment possible by means of serial data control *

Note: Serial data control

Operating Description

Figure 1 shows CDS/AGC +ADC function block.

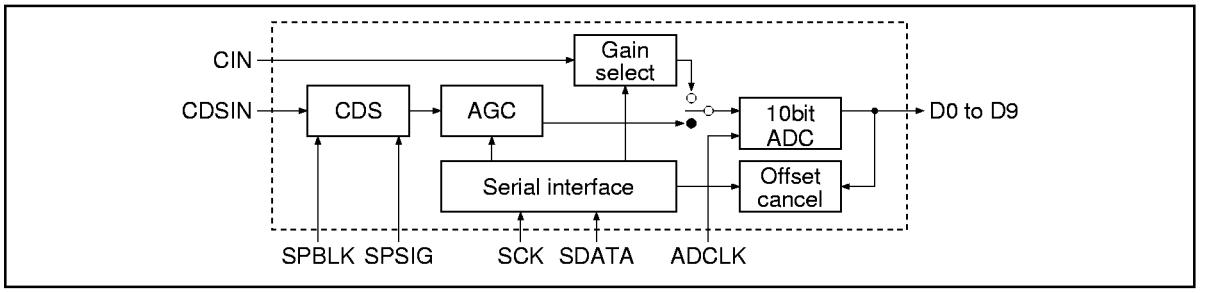


Figure 1 CDS/AGC +ADC Function Block

1. CDS (Correlated Double Sampling) Circuit

   The CCD imaging element alternately outputs a black level (A-period signal) and a signal including the black level (B-period signal). The CDS circuit extracts the differential voltage between the black level and the signal including the black level (see figure 3).

   Black level sampling is performed at the rising edge of the SPBLK pulse, and signal level sampling is performed at the rising edge of the SPSIG pulse. This sequence of operations extracts the differential voltage between the black level and the signal including the black level, and supplies this to the next-stage AGC circuit.

2. AGC Circuit

   This circuit sets the AGC gain by means of 10-bit digital data. The setting range is 0 to 29.4 dB (0.034 dB/step). However, codes 354 to 512 cannot be used when setting the AGC gain by means of digital data.

3. Gain Select Circuit

   This circuit is used for direct input of analog signals to the 10-bit ADC. The gain is set by means of 9-bit digital data. The setting range is 0.625 times (–4.1 dB) to 4.617 times (13.3 dB) in 0.0078-times steps.

4. Offset Cancel Circuit

   This circuit performs automatic adjustment, by means of serial data control, of the offset voltages generated by the CDS, AGC, ADC, and other circuits.

Timing Chart

Figure 2 shows the output timing when the CDSIN and ADCIN input pins are used. ADCIN indicates CIN.

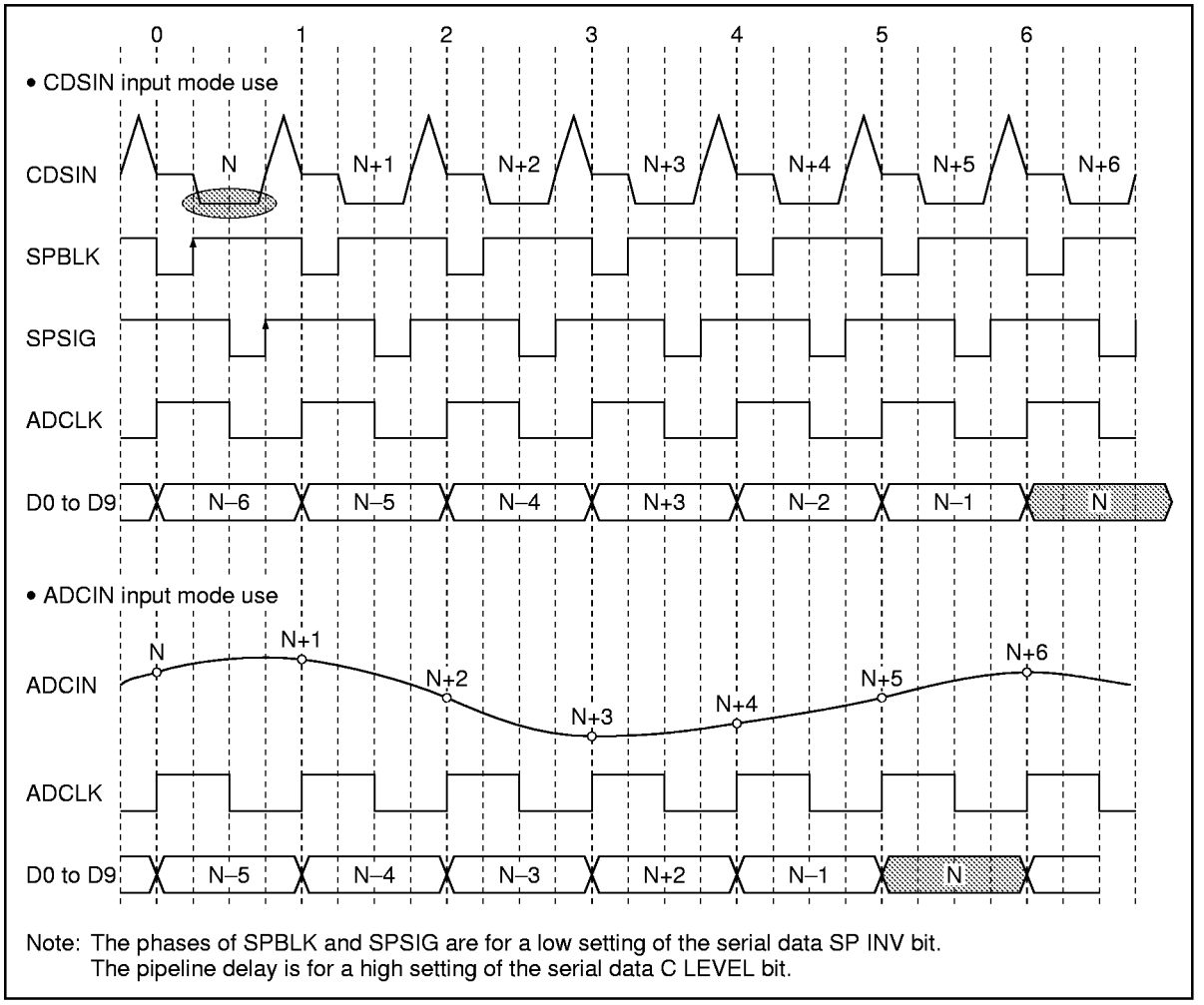
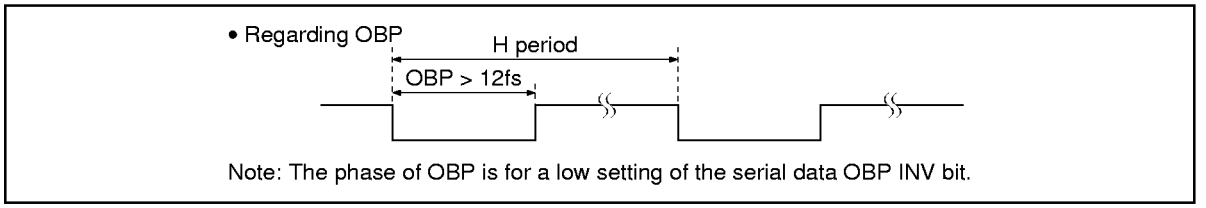


Figure 2 Output Timing when Using CDSIN and ADCIN Input Pins

- The ADC output signals (D0 to D9) are output at the rising edge of ADCLK in both input modes.
- The pipeline delay is 6 clocks when CDSIN is used, and 5 clocks when ADCIN is used.
- In the ADCIN input mode, input signal sampling is performed at the rising edge of ADCLK.



Details of Timing Specifications

Details of Timing Specifications when Using CDSIN

Details of the timing specifications when using CDSIN are shown in figure 3, and the timing specifications are summarized in table 1.

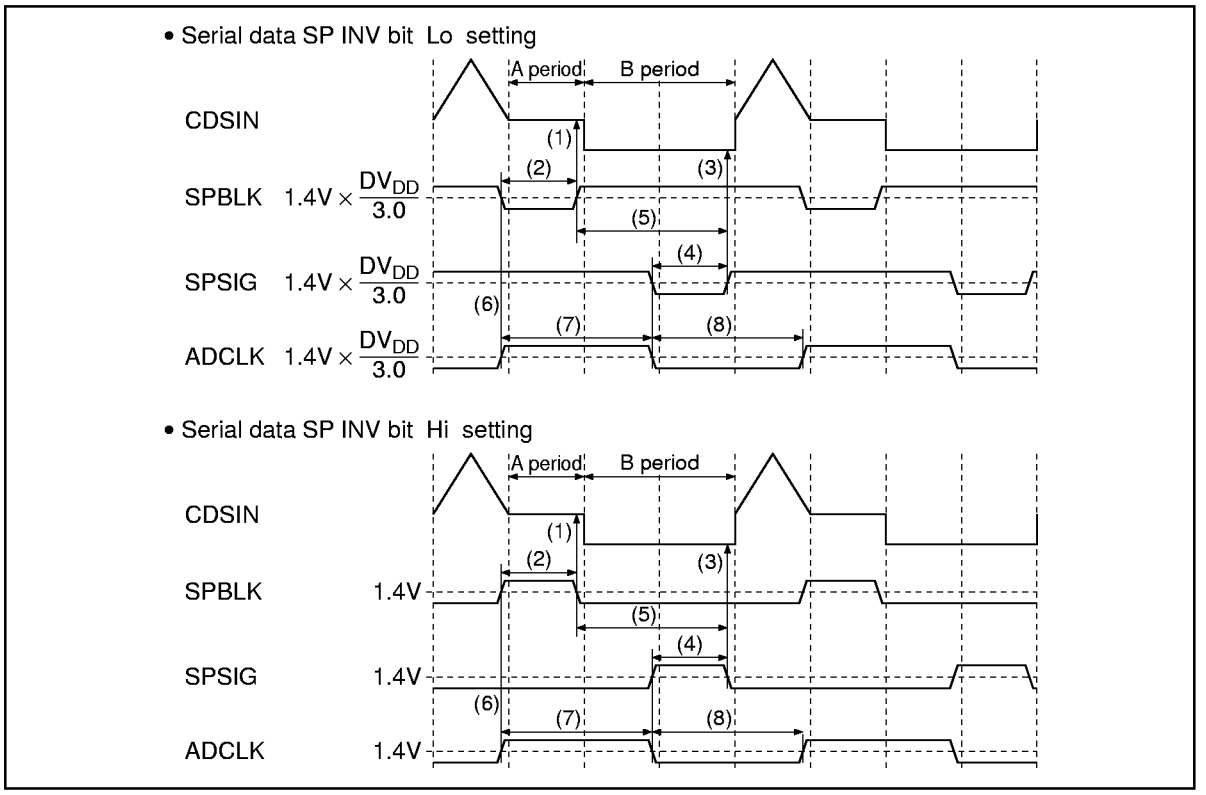
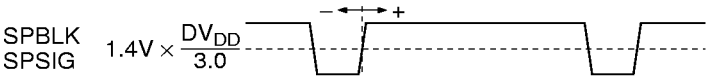


Figure 3 Details of Timing Specifications when Using CDSIN

Table 1 Each Timing Specifications

No.	Timing	Min	Typ	Max	Unit	Note
(1)	Black level signal read-in time	0	5	10	ns	1
(2)	SPBLK "Lo" period	11.5	$1/4f_{ADCLK}$	Typ × 1.2	ns	2
(3)	Signal level read-in time	0	5	10	ns	1
(4)	SPSIG "Lo" period	11.5	$1/4f_{ADCLK}$	Typ × 1.2	ns	2
(5)	SPBLK rise to SPSIG rise	20.0	$1/2f_{ADCLK}$	Typ × 1.15	ns	2
(6)	SPBLK fall to ADCLK rise	–10.0	0.0	10.0	ns	2
(7), (8)	ADCLK t_{WH} Min / t_{WL} Min	24.0	—	—	ns	

Note: 1. Negative when data before the rising edge of SPBLK/SPSIG is sampled, and positive when data after the rising edge is sampled.



2. The polarity of SPBLK and SPSIG is for a low setting of the serial data SPINV bit.

Details of Timing Specifications when Using ADCIN

Details of the timing specifications when using ADCIN are shown in figure 4.

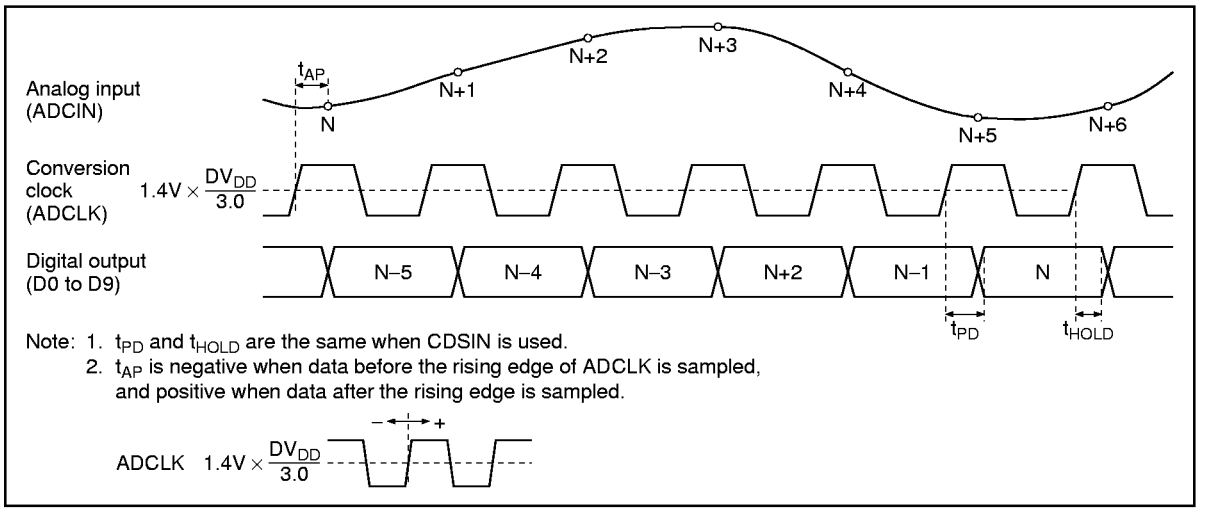


Figure 4 Details of Timing Specifications when Using ADCIN

Output Code Table

Table 2 Function Table

				Digital Output										Operation
STBY	**TEST**	**LINV**	**MINV**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Mode**
H	X	X	X	Hi-Z										Low power standby
L	L	L	L	Table 3 as follows										Normal operation
		L	H	In the table 3 below, D9 is inverted										
		H	L	In the table 3 below, D8 to D0 are inverted										
		H	H	In the table 3 below, D9 to D0 are inverted										
	H	L	L	L	H	L	H	L	H	L	H	L	H	Test mode
		L	H	H	H	L	H	L	H	L	H	L	H	
		H	L	L	L	H	L	H	L	H	L	H	L	
		H	H	H	L	H	L	H	L	H	L	H	L	

Note: STBY, TST, LINV and MINV are serial control.

Table 3 Output Code Table

Output			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output code	Step	0	L	L	L	L	L	L	L	L	L	L
		1	L	L	L	L	L	L	L	L	L	H
		2	L	L	L	L	L	L	L	L	H	L
		3	L	L	L	L	L	L	L	L	H	H
		.	.	.	.	.	.	.	.	.	.	.
		.	.	.	.	.	.	.	.	.	.	.
		.	.	.	.	.	.	.	.	.	.	.
		511	L	H	H	H	H	H	H	H	H	H
		512	H	L	L	L	L	L	L	L	L	L
		.	.	.	.	.	.	.	.	.	.	.
		.	.	.	.	.	.	.	.	.	.	.
		.	.	.	.	.	.	.	.	.	.	.
		1020	H	H	H	H	H	H	H	H	L	L
		1021	H	H	H	H	H	H	H	H	L	H
		1022	H	H	H	H	H	H	H	H	H	L
		1023	H	H	H	H	H	H	H	H	H	H

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	$V_{DD(max)}$	6.0	V
Power dissipation	$P_{D(max)}$	400	mW
Analog input voltage	$V_{IN(max)}$	–0.3 to AV_{DD} +0.3	V
Digital input voltage	$V_{I(max)}$	–0.3 to 6.0	V
Operating temperature	Topr	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Note: 1. V_{DD} indicates AV_{DD} and DV_{DD}.
2. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ)

- Items common to CDSIN input mode and ADCIN input mode (ADCIN indicates CIN)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	V_{DD}	2.85	3.00	3.60	V	f_{CLK} = 18 MHz	
Conversion speed range	f_{CLK} max	5.5	—	18.2	MHz		
CCD allowable offset	$V_{OF(CCD)}$	(–30)	—	(30)	mV		*1
Digital input voltage	V_{IH}	$2.0 \times \frac{DV_{DD}}{3.0}$	—	5.0	V		5 V amplitude input possible
	V_{IL}	0	—	$0.8 \times \frac{DV_{DD}}{3.0}$	V		
	V_{IH2}	$2.25 \times \frac{DV_{DD}}{3.0}$	—	5.0	V		
	V_{IL2}	0	—	$0.6 \times \frac{DV_{DD}}{3.0}$	V		
Digital output voltage	V_{OH}	DV_{DD} –0.5	—	—	V	I_{OH} = –2 mA	
	V_{OL}	—	—	0.5	V	I_{OL} = +2 mA	
Digital input current	I_{IH}	—	—	50	µA	V_{IH} = 5.0 V	
	I_{IL}	–50	—	—	µA	V_{IL} = 0 V	
Digital output current	I_{OZH}	—	—	50	µA	V_{OH} = V_{DD}	
	I_{OZL}	–50	—	—	µA	V_{OL} = 0 V	
ADC resolution	RES	10	10	10	bit		
ADC integration linearity	INL+	—	1.0	3.0	LSB	f_{CLK} = 18 MHz	
	INL–	–3.0	–1.0	—	LSB		
ADC differentiation linearity	DNL+	—	0.3	0.8	LSB	f_{CLK} = 18 MHz	*2
	DNL–	–0.8	–0.3	—	LSB		
Digital output delay time	t_{PD}	—	—	35	ns	C_L = 10 pF	
Digital output hold time	t_{HOLD}	10	—	—	ns		
Sleep current	I_{SLP}	–100	0	100	µA	Digital input pins fixed at 0 V, output pins open	
Standby current	I_{STBY}	—	10	14	mA	Digital input pins fixed at 0 V	
Input range	V_{INp-p}	—	(1.0)	—	V	Gain 0 dB	*1

Note: 1. Items in parentheses are reference values. Refer to page 17.
2. DNL calculate the difference of linearity error between next two codes.

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ) (cont)

- Items applicable to CDSIN input mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Quiescent current	I_{DD1}	—	64	74	mA	f_{CLK} = 18 MHz	CDSIN use
Timing specification (1)	t_{CDS1}	0	5	10	ns		*3
Timing specification (2)	t_{CDS2}	11.5	$1/4f_{ADCLK}$	Typ × 1.2	ns		
Timing specification (3)	t_{CDS3}	0	5	10	ns		
Timing specification (4)	t_{CDS4}	11.5	$1/4f_{ADCLK}$	Typ × 1.2	ns		
Timing specification (5)	t_{CDS5}	20.0	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specification (6)	t_{CDS6}	–10.0	0.0	10.0	ns		
Timing specification (7)	t_{CDS7}	24.0	—	—	ns		
Timing specification (8)	t_{CDS8}	24.0	—	—	ns		
Input current	IIN_{CDS}	–60	—	10	µA	f_{CLK} = 18 MHz, Black/signal level difference = 1 V, gain = 0 dB	*4
Clamp level	CLP_{CDS}	—	(32)	—	LSB	Serial data CLEBEL = Low	*1
		—	(48)	—	LSB	Serial data CLEBEL = High	*1
AGC gain	AGC(0000)	–2.0	0.0	2.0	dB		*5
	AGC(0128)	2.4	4.4	6.4	dB		
	AGC(0256)	6.7	8.7	10.7	dB		
	AGC(0353)	10.0	12.0	14.0	dB		
	AGC(0513)	10.0	12.0	14.0	dB		
	AGC(0640)	14.4	16.4	18.4	dB		
	AGC(0768)	18.7	20.7	22.7	dB		
	AGC(0896)	23.1	25.1	27.1	dB		
	AGC(1023)	26.9	29.4	31.4	dB		

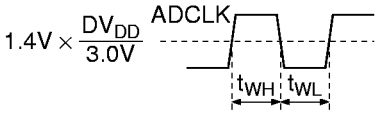
Note: 3. Refer to page 9 (Details of Timing Specifications when Using CDSIN).
4. This is not transition current, but static current.
5. Refer to page 19 (Correspondence between AGC Gain Setting and Serial Data Setting Gain).

Electrical Characteristics (Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, R_{EXT} = 24 kΩ) (cont)

- Items applicable to ADCIN input mode

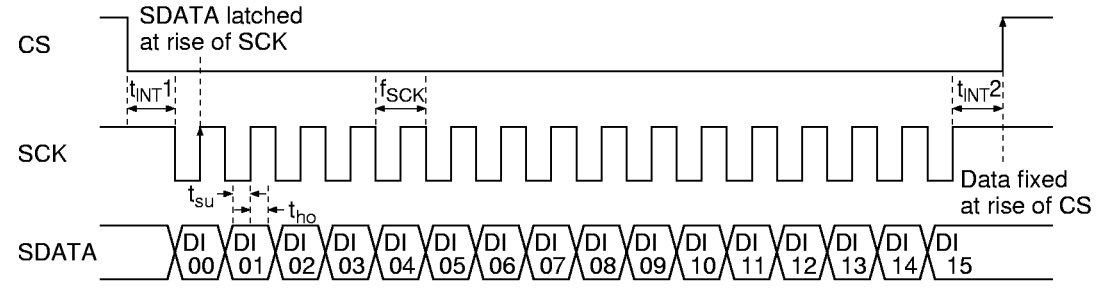
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Quiescent current	I_{DD2}	—	48	57	mA	f_{ADCLK} = 18 MHz, f_{IN} = 1 kHz, sine wave	
Minimum clock pulse width	t_{WH} Min	—	—	24	ns	f_{ADCLK} = 18 MHz, f_{IN} = 9.001 MHz, sine wave	*6
	t_{WL} Min	—	—	24	ns		
Maximum clock pulse width	t_{WH} Max	100	—	—	ns		
	t_{WL} Max	100	—	—	ns		
Analog signal read-in time	t_{AP}	0	—	15	ns		*7
Input current for chroma input	IIN_{CIN}	–60	—	60	µA	V_{IN} = 1.0 to 2.0 V	*4
Clamp level for chroma input	OF2	462	512	562	LSB		
Gain select block gain	GSL(000)	0.50	0.63	0.79			
	GSL(064)	0.89	1.13	1.43			
	GSL(128)	1.29	1.63	2.05			
	GSL(192)	1.69	2.13	2.68			
	GSL(256)	2.08	2.63	3.31			
	GSL(320)	2.49	3.13	3.94			
	GSL(384)	2.88	3.63	4.57			
	GSL(448)	3.28	4.13	5.20			
	GSL(511)	3.67	4.62	5.81			
Input capacitance	CIN_{ADC}	—	(10)	—	pF		*1

Note: 6. Regarding t_{WH} and t_{WL}.



7. Refer to page 11 (Details of Timing Specifications when Using ADCIN).

Serial Interface Specification



Note: 1. SDATA is latched at the rise of SCK.
2. Input 16 SCK clocks while CS is low. If the number of clocks is more or less than 16, the data will be invalid.

Timing Specifications

	Min	Max
f_{CLK}		3MHz
$t_{INT}1$, 2	$1/t_{CLK}$	
t_{su}	50ns	
t_{ho}	50ns	

Figure 5 Serial Interface Specification

Black Level Signal Level Difference during OBP Period

The difference between the black level sampling voltage and signal level sampling voltage during the OBP period is designated $V_{OF\ (CCD)}$. This value is positive when (signal level sampling voltage) > (black level sampling voltage).

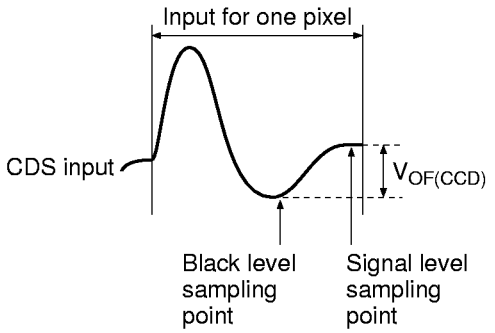


Figure 6 Black Level Signal Level Difference during OBP Period

Table 4 Serial Data Function Table

	Function			
DI 00	Lo	Hi	Lo	Hi
DI 01	Lo	Lo	Hi	Hi
DI 02	AGC gain setting(LSB)	Lo→CDSIN input mode Hi→ADCIN input mode	SP INV SPSIG/SPBLK inversion	CIF Lo→CLK>10MHZ Hi→CLK<10MHZ
DI 03	AGC gain setting	Test mode Low *4	Test mode *4 Use prohibited ALL Low	Test mode *4 Use prohibited ALL Low
DI 04	AGC gain setting	Gain select circuit gain setting(LSB)		
DI 05	AGC gain setting	Gain select circuit gain setting		
DI 06	AGC gain setting	Gain select circuit gain setting		
DI 07	AGC gain setting	Gain select circuit gain setting		
DI 08	AGC gain setting	Gain select circuit gain setting	C level Lo→Black level=32/1023 Hi→Black level=48/1023	
DI 09	AGC gain setting	Gain select circuit gain setting	OBP inv Lo→Negative input Hi→Positive input	
DI 10	AGC gain setting	Gain select circuit gain setting	Test mode *4 Use prohibited ALL Low	
DI 11	AGC gain setting(MSB)	Gain select circuit gain setting		
DI 12	Output mode setting (LINV)	Gain select circuit gain setting(MSB)		
DI 13	Output mode setting (MINV)	RESET Lo→Reset mode Hi→Normal operation mode		
DI 14	Output mode setting (TEST)	OFRST Lo→Normal operation mode Hi→Offset cancel mode		
DI 15	Output mode setting (STBY) *2 *3	SLP Lo→Normal operation mode*2 Hi→Sleep mode		

Notes: 1. When the ADCIN input mode is selected, the ADC gain setting is invalid and data 354 to 512 cannot be used. (see table 6).
2. STBY: Reference voltage generation circuit is in the operational state.
SLP: All circuits are in the sleep state.
3. When selecting STBY mode, set the ADCIN input mode before setting STBY to high.
4. Test mode is used for IC testing, and so cannot be used.
An all low setting should be made.
5. This IC has two operating modes, determined by the C level setting (see table 5).

Table 5 Operation Mode Comparison Table

DI 00 = Lo **DI 01 = Hi**	**C level = Lo** **Black level = 32/1023**		**C level = Hi** **Black level = 48/1023**	
Clamp level	32 LSB		48 LSB	
Pipe line delay	ADCIN	CDSIN	ADCIN	CDSIN
	4 CLK	5 CLK	5 CLK	6 CLK
OBP polarity *[1]	Corresponds to OBPinv setting		Corresponds to OBPinv setting	

Note: 1. OBP polarity

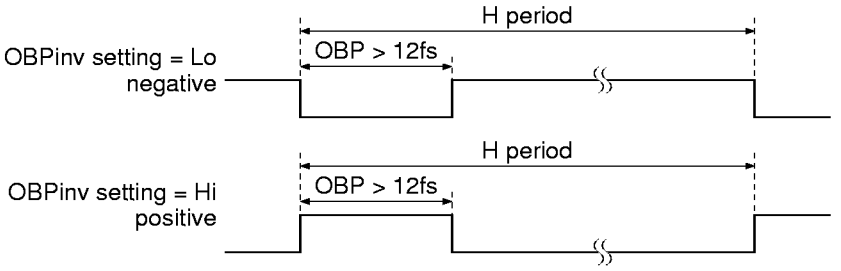
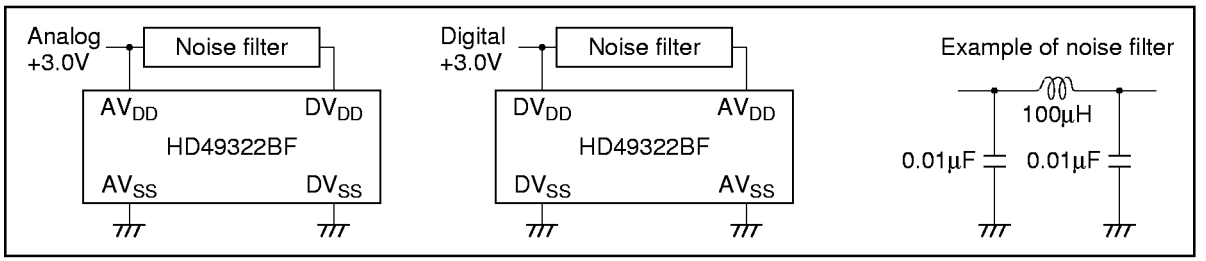


Table 6 Correspondence between AGC Gain Setting and Serial Data Setting Gain

	Gain Setting Serial Data										
Gain Setting Data	**GA9 (MSB)**	**GA8**	**GA7**	**GA6**	**GA5**	**GA4**	**GA3**	**GA2**	**GA1**	**GA0 (LSB)**	**Setting G Gain (dB)**
0	0	0	0	0	0	0	0	0	0	0	0.0
1	0	0	0	0	0	0	0	0	0	1	0.034
2	0	0	0	0	0	0	0	0	1	0	0.068
3	0	0	0	0	0	0	0	0	1	1	0.102
4	0	0	0	0	0	0	0	1	0	0	0.136
:						:					:
353	0	1	0	1	1	0	0	0	0	1	12.002
354	0	1	0	1	1	0	0	0	1	0	can not
:						:					use
511	0	1	1	1	1	1	1	1	1	1	
512	1	0	0	0	0	0	0	0	0	0	
513	1	0	0	0	0	0	0	0	0	1	12.036
514	1	0	0	0	0	0	0	0	1	0	12.070
:						:					:
1023	1	1	1	1	1	1	1	1	1	1	29.376

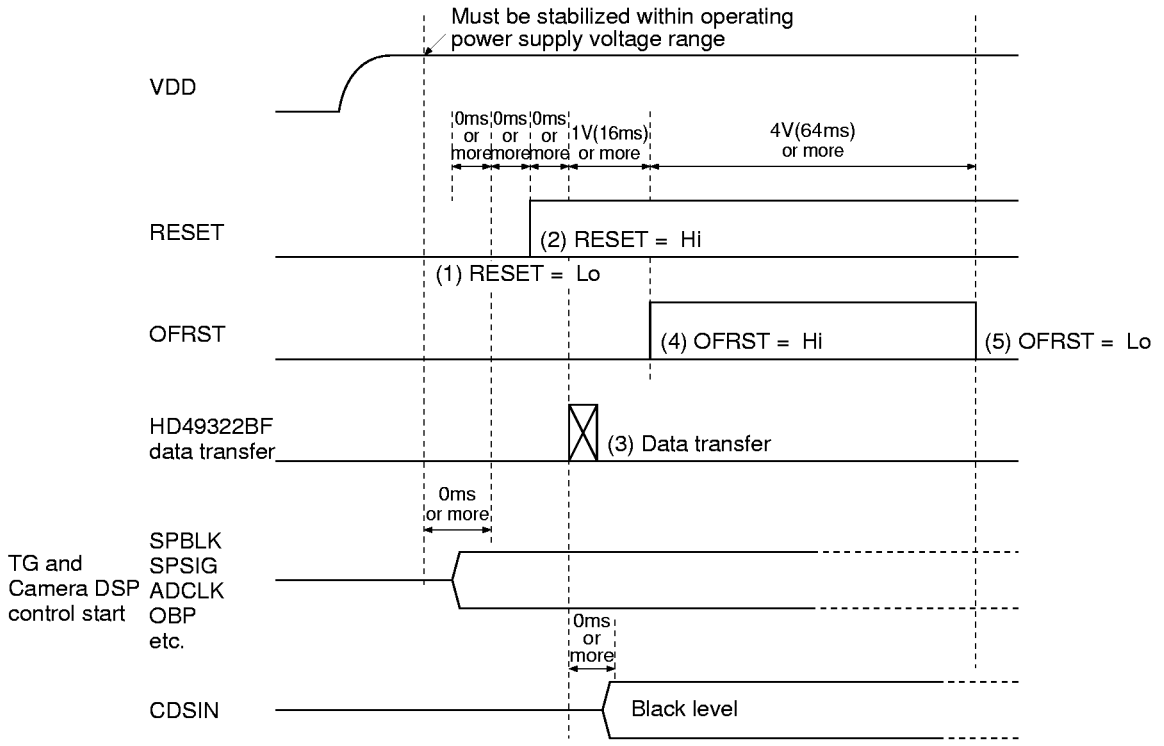
Notice for Use

1. Careful handling is necessary to prevent damage due to static electricity.
2. This product has been developed for consumer applications, and should not be used in non-consumer applications.
3. As this IC is sensitive to power line noise, the ground impedance should be kept as small as possible. Also, to prevent latchup, a ceramic capacitor of 0.1 mF or more and an electrolytic capacitor of 10 mF or more should be inserted between the ground and power supply.
4. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.
5. If a noise filter is necessary, make a common connection after passage through the filter, as shown in the figure below.



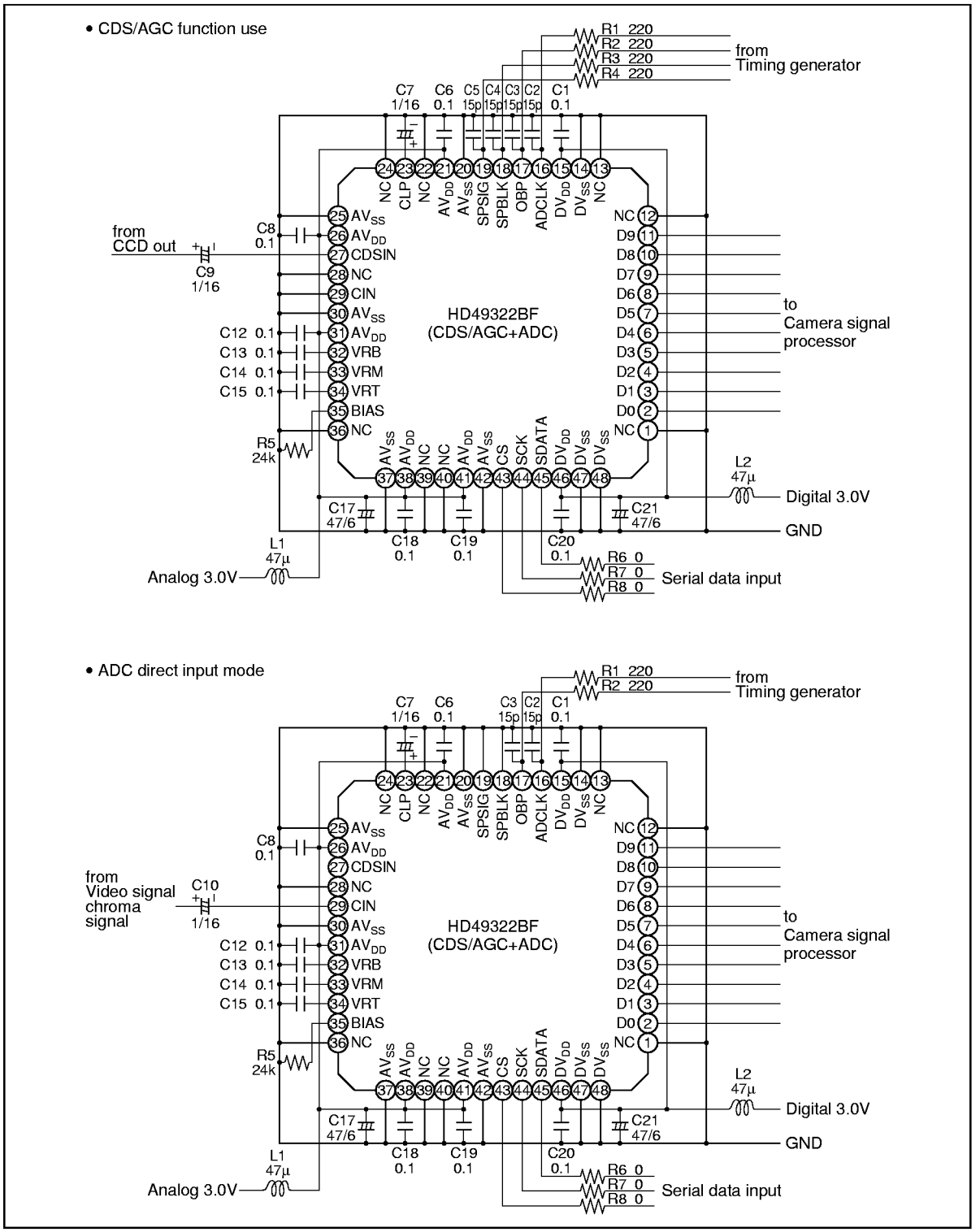
6. Connect AV_{SS} and DV_{SS} off-chip using a common ground. If there are separate analog system and digital system set grounds, connect to the analog system.
7. When V_{DD} is specified in the delivery specification, this indicates AV_{DD} and DV_{DD}.
8. No Connection (NC) pins are not connected inside the IC, but it is recommended that they be used as power supply ground pins or left open to prevent crosstalk in adjacent analog pins.
9. To ensure low thermal resistance of the package, a Cu-type lead material is used. As this material is less tolerant of bending than Fe-type lead material, careful handling is necessary.
10. The infrared reflow soldering method should be used to mount the chip. Note that general heating methods such as solder dipping cannot be used.
11. Confirm that the difference between the black level sampling voltage and signal level sampling voltage during the OBP period is within ±30 mV. Be sure to inform Hitachi if this range is exceeded. Depending on the mounting state, picture quality (crosscut [??] noise, wave pattern, etc.) will be dependent upon the timing of the SPBLK, SPSIG, and ADCLK signals. Check the mounting state thoroughly before use.
12. Serial communication should not be performed during the effective video period, since this will result in degraded picture quality. Also, use of dedicated ports is recommended for the SCK and SDATA signals used in the HD49322BF. If ports are to be shared with another IC, picture quality should first be thoroughly checked.

Operating Sequence at Power-On



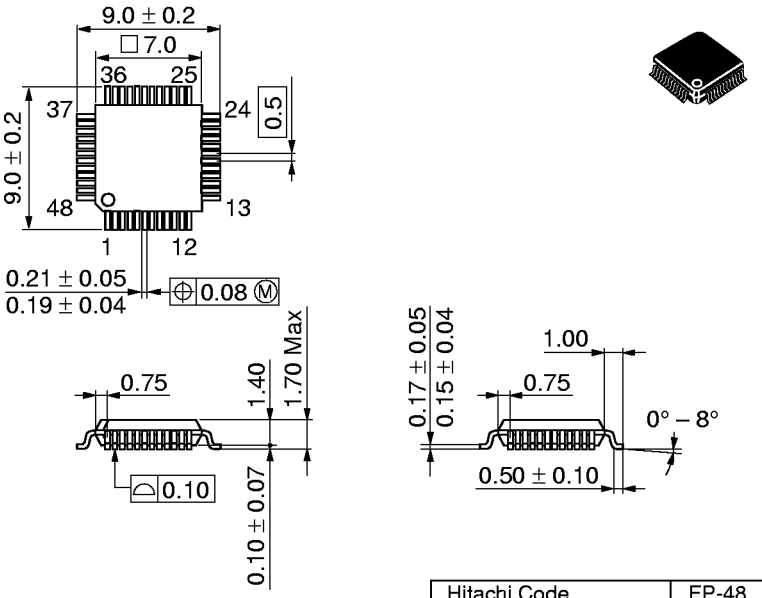
Note: 1. RESET and OFRST both use serial data transmission.
2. Stable input of SPBLK, SPSIG, ADCLK, and OBP is assumed before RESET is transmitted.
3. Numbers in parentheses in the figure show the order of transfer.
4. The CCD output black level need not be latched in accordance with the above timing.

Example of Recommended External Circuit



Package Dimensions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-48
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.2 g