Serial interface IC for DIMMs supporting plug & play

BU9877FV

The BU9877FV is a 2-k bit EEPROM with a write protect function, developed for DIMMs (Dual In-line Memory Modules) containing a synchronous DRAM. This IC stores IDs in memory in order to enable Plug & Play functions.

●Applications

168-pin and 144-pin DRAM modules containing synchronous DRAM

●Features

1) 2-k bit EEPROM with configuration of 256 words × 8 bits.
2) Compliance with SPD data format.
3) Dual-line serial (I^2C bus) interface.
4) Protective functions enabled by a one-time ROM and write protect pin.
   Soft ware protection. as a one-time ROM: 00 to 7Fh.
   Hard ware protection (WP pin): 80 to FFh.
5) Compact SSOP-B 8-pin package.

●Absolute maximum ratings (Ta = 25°C)

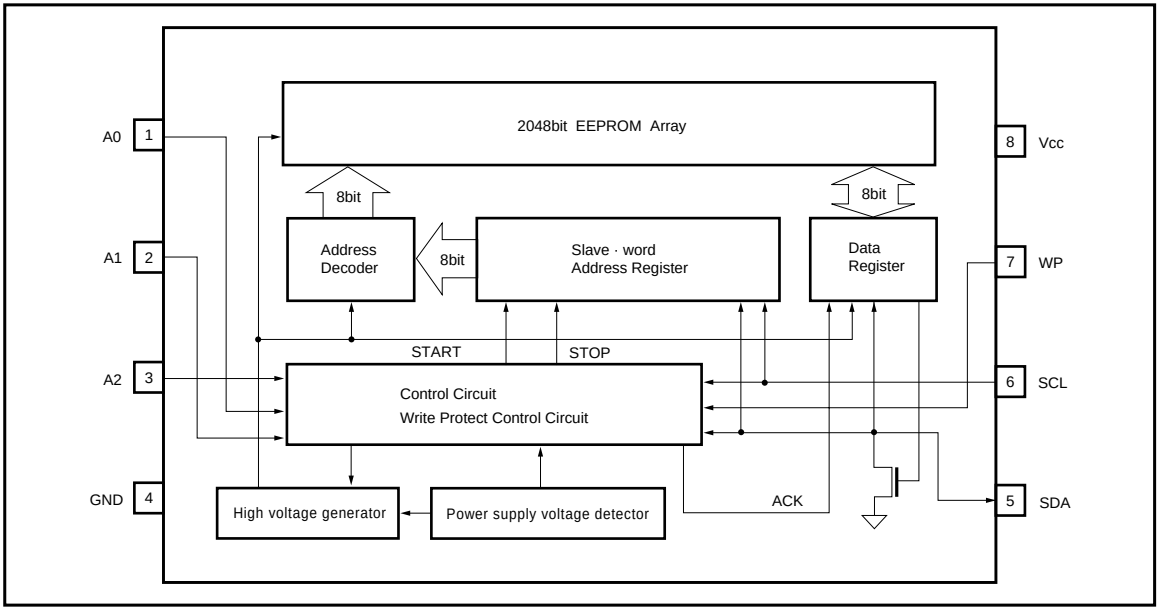
Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	– 0.3 ~ + 7.0	V
Power dissipation	Pd	300*	mW
Storage temperature	Tstg	– 65 ~ + 125	°C
Operating temperature	Topr	– 40 ~ + 85	°C
Input voltage	—	– 0.3 ~ V_{CC} + 0.3	V

*1 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7 ~ 5.5	V
Input voltage	V_{IN}	0 ~ V_{CC}	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	I / O	Function
1, 2, 3	A0, A1, A2	I	Slave address setting (pin)
4	GND	—	Input / output reference voltage of 0V
5	SDA	I / O	Slave and word address, serial data input / output
6	SCL	I	Serial clock input
7	WP	I	Write protect input
8	V_{CC}	—	Connect the power supply to this.

Note: The SDA pin is Nch open drain output, and should be used with external pull-up resistor.
The WP pin is equipped with internal pull-down resistor, so can be left open when used.

●Electrical characteristics (unless otherwise noted, Ta = – 40 to + 85°C, Vcc = 2.7V to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Input high level voltage	V_{IH}	0.7V_{CC}	—	—	V	—	—
Input low level voltage	V_{IL}	—	—	0.3V_{CC}	V	—	—
Output low level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0mA (SDA)	Fig.1
Input leakage current 1	I_{LI1}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}	Fig.2
Input leakage current 2	I_{LI2}	– 1	—	20	µA	V_{IN} = 0V ~ V_{CC} (WP)	Fig.2
Output leakage current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC}	Fig.2
Operating current consumption	I_{CC}	—	—	3.0	mA	V_{CC} = 5.5V, f_{SCL} = 100kHz	Fig.3
Standby current	I_{SB}	—	—	2.0	µA	V_{CC} = 5.5V, SDA · SCL = V_{CC}	Fig.4
SCL frequency	f_{SCL}	—	—	100	kHz	—	—

●Measurement circuits

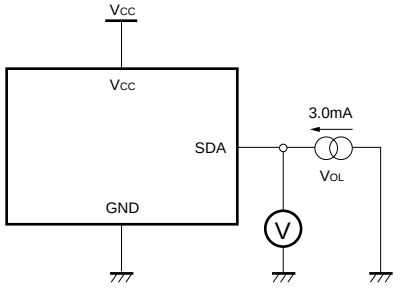


Fig. 1 LOW output voltage measurement circuit

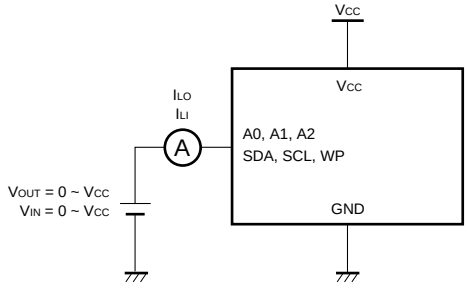


Fig. 2 Input / output leakage current measurement circuit

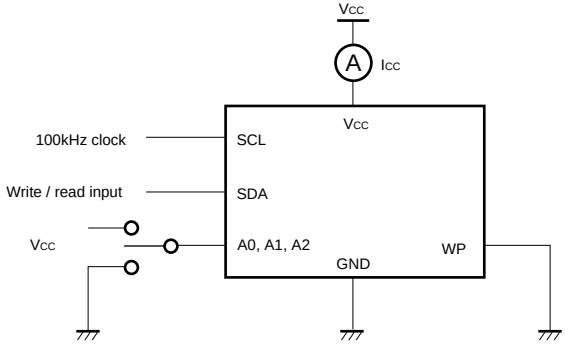


Fig. 3 Current consumption measurement circuit

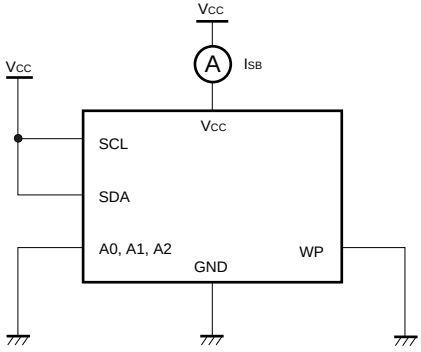


Fig. 4 Standby current measurement circuit

●Circuit operation

(1) Synchronous data I / O timing

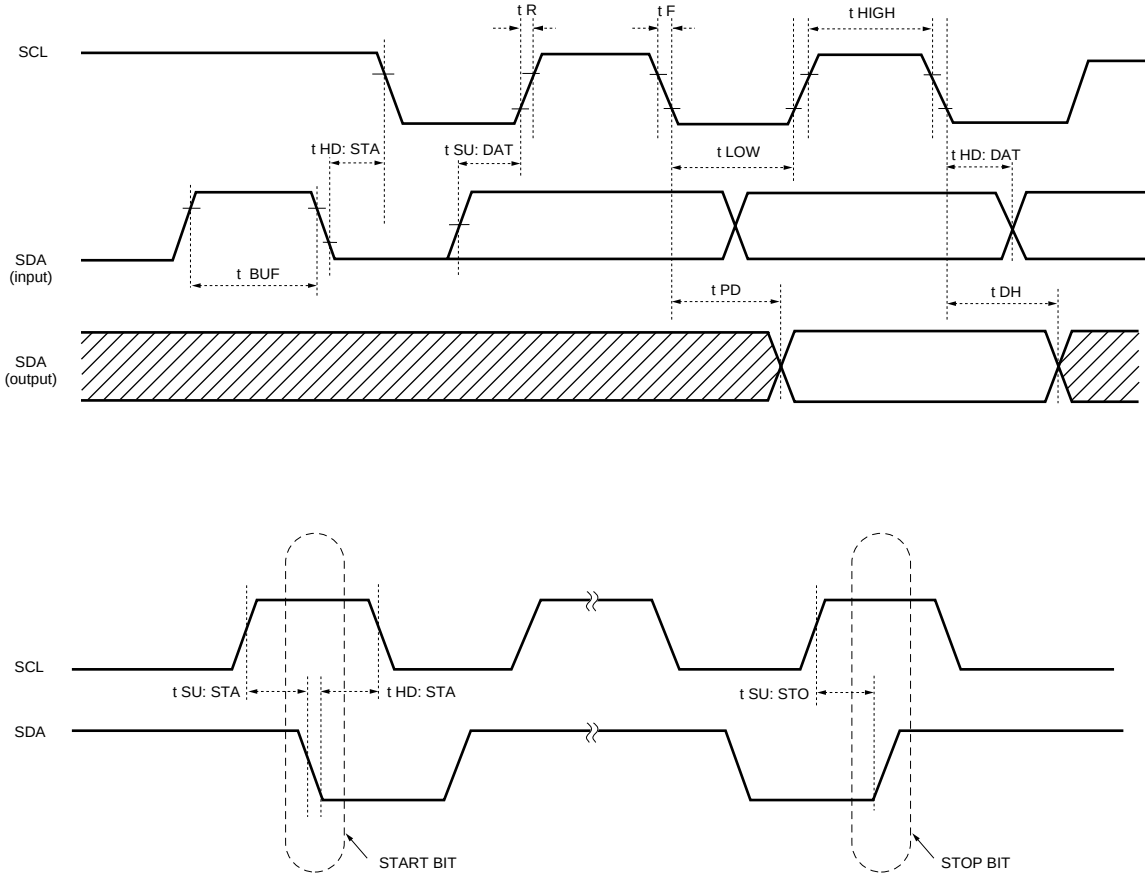


Fig. 5

• Reading of input is done at the rising edge of SCL.

• Output of data is synchronized to the falling edge of SCL.

●Operation timing characteristics (unless otherwise noted, Ta = – 40 to + 85°C , Vcc = 2.7V to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data clock HIGH time	t HIGH	4.0	—	—	µs
Data clock LOW time	t LOW	4.7	—	—	µs
SDA / SCL rise time	t R	—	—	1.0	µs
SDA / SCL fall time	t F	—	—	0.3	µs
Start condition hold time	t HD: STA	4.0	—	—	µs
Start condition setup time	t SU: STA	4.7	—	—	µs
Input data hold time	t HD: DAT	0	—	—	ns
Input data setup time	t SU: DAT	250	—	—	ns
Output data delay time	t PD	—	—	3.5	µs
Output data hold time	t DH	0.3	—	—	µs
Stop condition setup time	t SU:STO	4.7	—	—	µs
Bus release time prior to start of transfer	t BUF	4.7	—	—	µs
Internal write cycle time *1	t WR1	—	—	10	ms
Internal write cycle time *2	t WR2	—	—	15	ms
Effective noise elimination interval (SCL, SDA pins)	t I	—	—	0.1	µs

*1 Vcc = 4.5V to 5.5V
*2 Vcc = 2.7V to 5.5V

(3) Start condition (start bit recognition)
Before executing the various commands, a start condition (start bit) must be input. This is recognized when SCL is HIGH and SDA falls from HIGH to LOW.
If a start condition is not input, no commands will be received.
(4) Stop condition (stop bit recognition)
To terminate the various commands, a stop condition (stop bit) must be input. This is recognized when SCL is HIGH and SDA rises from LOW to HIGH.
(5) Precautions concerning the write command
With the write command, internal writing is initiated by inputting the stop bit after the data has been input.
(6) Device addressing (specifying the slave address)
The master address should be output first, followed by the start condition, and then the slave address. The first four bits of the slave address are used to recognize the device type. The device code for this IC is fixed at "1010". When accessing the write protect register, a device code of "0110" is used.
The next three bits of the slave address (A2, A1, A0) are used to select the device, and the IC begins to function only if the data input for A2 to A0 matches the states of input pins A2 to A0. Consequently, up to eight of these ICs may be connected on the same bus, depending on the combination of A2 to A0.

The last bit of the slave address (R / $\overline{W}$) is used to specify either writing or reading, and is as shown below.

R / $\overline{W}$ set to 0: Writing or Random Read
R / $\overline{W}$ set to 1: Reading

Device type	Device address				
1 0 1 0	A2	A1	A0	R / $\overline{W}$	Access to memory
0 1 1 0	A2	A1	A0	$\overline{W}$	Access to write protect register

(7) Write protect command

The write protect command is used to prohibit writing of data to addresses 00 to 7Fh, among the 256 word address data. Be aware that once a write protect register has been specified, it cannot be canceled (one-time memory). The write protect command can function regardless of the state of the WP pin.

(8) WP (write protect pin)

Setting the WP pin to Vcc (HIGH level) has the same effect as using the write protect command, and inhibits writing of data to addresses 80 to FFh, among the 256 word address data. Normal writing is enabled by setting this pin to GND (LOW level). (If the write protect command is used to inhibit writing, data cannot be written regardless of the status of the WP pin.) The WP pin is equipped with an internal pull-down resistor, so if the protect function is not being used, this should be left open or set to GND.

(9) ACK signal

The acknowledge signal (ACK signal) is determined by the software, and indicates whether or not the data has been correctly transmitted. Regardless of whether the address is a master or slave address, the device on the transmitter (sending signal) side (the master when a slave address is input for a write command or a read command, and the EEPROM when read command data is output) opens the bus after this 8-bit data is output. With a device on the receiving (reception) side (the EEPROM when a slave address is input for a read command or write command, and the master when data is output for a read command), SDA is set to LOW during the nine-clock cycle, and the acknowledge signal (ACK signal) is output when 8-bit data is received.

For writing operations, the acknowledge signal (ACK signal) is output in the LOW state each time that 8-bit data (word address or write data) is received.

In reading operations, 8-bit data (read data) is output, and then the acknowledge signal (ACK signal) in the LOW state is detected. If the acknowledge signal (ACK signal) is detected and no stop condition is sent from the master (microcomputer) side, this IC continues to output data. If the acknowledge signal (ACK signal) is not detected, this IC interrupts the transmission of data, recognizes a stop condition (stop bit), and terminates the reading operation. The IC then enters the standby mode.

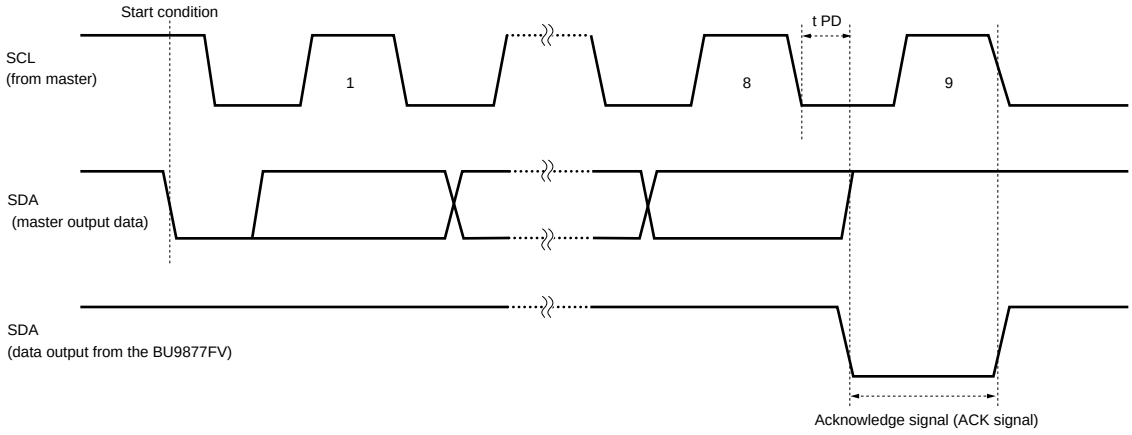


Fig. 6 Acknowledge signal (ACK signal) response
(when slave address is input for writing or reading)

(10) Timing charts

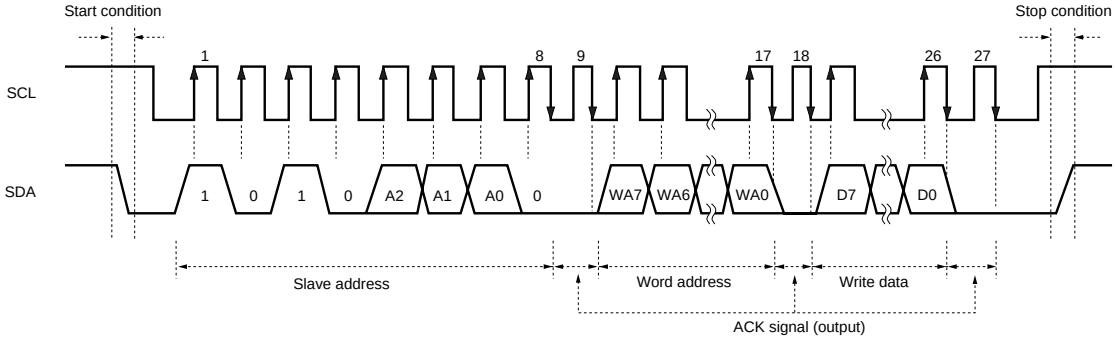


Fig. 7 Byte write cycle

- Data is written to the address specified by the word address (n address).
- After 8 bits of data are input, a stop bit is generated. This initiates writing of the data to the memory cell.

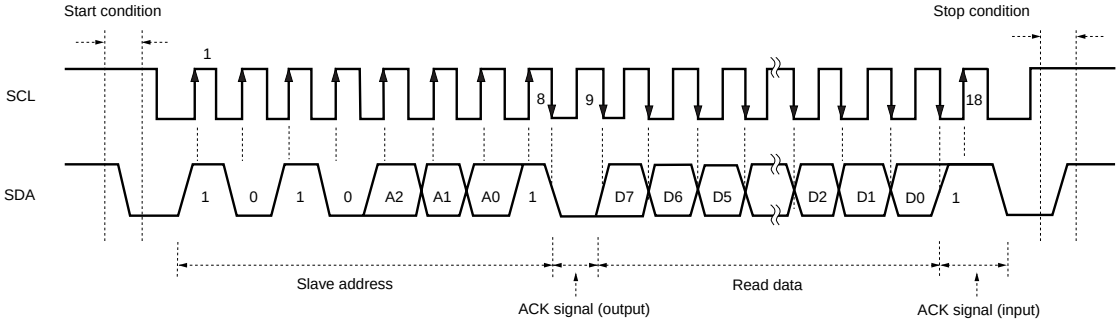


Fig. 8 Current read cycle

- This IC has an internal circuit address counter to store the previously accessed address in the memory. If the previous command was a write command, the write word address data (n) is read, and if the previous command was a read command, the read word address data (n) incremented by one address (n + 1) is read.
- If the ACK signal LOW following D0 is detected and no stop condition is sent from the master side, reading can be continued sequentially to the next data.

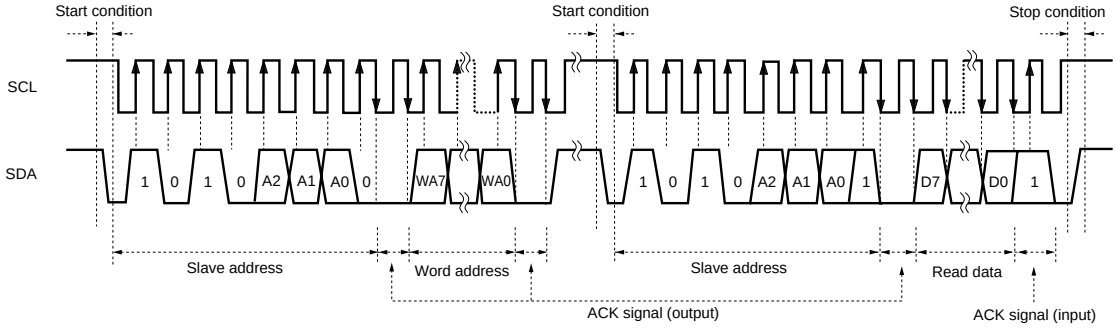


Fig. 9 Random read cycle

- This command enables reading of the data at the specified word address.
- If the ACK signal LOW following D0 is detected and no stop condition is sent from the master side, reading can be continued sequentially to the data of the next word address.
- To terminate this command, HIGH is input at the ACK signal timing (following any D0), then stop condition is input.

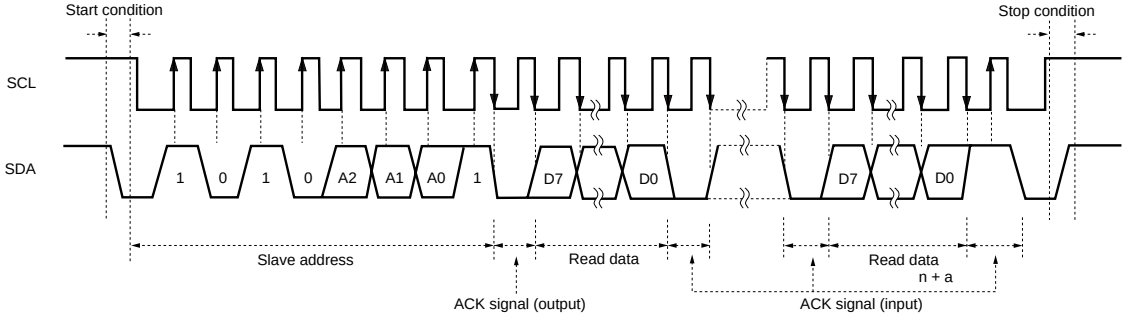


Fig. 10 Sequential read cycle

- If the ACK signal is detected following D0 and no stop condition is sent from the master side, reading can be continued sequentially to the data of the next word address.
- To terminate this command, HIGH is input at the ACK signal timing (following any D0), then stop condition is input.

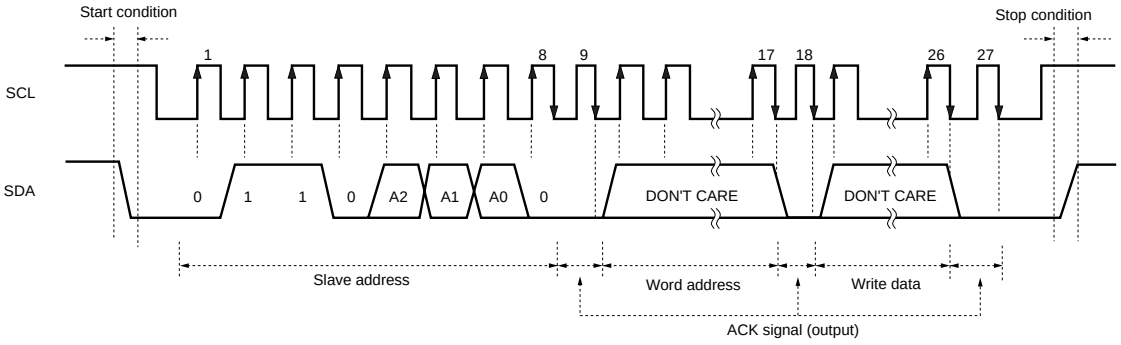
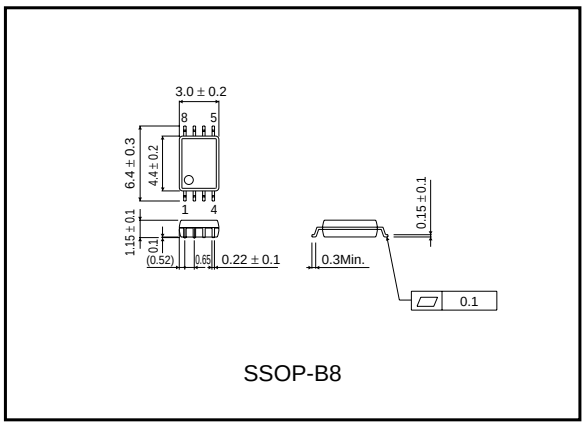


Fig. 11 Write protect cycle

- The write protect command is used to prohibit writing of data to addresses 00 to 7Fh, among the 256 word address data, and cannot be altered (one-time memory).
- The command is canceled if a stop condition has been input before the 27th clocks.
- If the write protect command is input when the protect status is already in effect, the command is canceled.

●External dimensions (Units: mm)



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