16 Mbit Concurrent SuperFlash + 2 / 4 Mbit SRAM ComboMemory
SST34HF1621 / SST34HF1641

Data Sheet

FEATURES:

- **Flash Organization: 1M x16**
- **Dual-Bank Architecture for Concurrent Read/Write Operation**
  - 16 Mbit: 12 Mbit + 4 Mbit
- **SRAM Organization:**
  - 2 Mbit: 256K x8 or 128K x16
  - 4 Mbit: 512K x8 or 256K x16
- **Single 2.7-3.3V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 25 mA (typical)
  - Standby Current: 20 µA (typical)
- **Hardware Sector Protection (WP#)**
  - Protects 4 outer most sectors (4 KWord) in the larger bank by holding WP# low and unprotects by holding WP# high
- **Hardware Reset Pin (RST#)**
  - Resets the internal state machine to reading data array
- **Sector-Erase Capability**
  - Uniform 1 KWord sectors
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Read Access Time**
  - Flash: 70 and 90 ns
  - SRAM: 70 and 90 ns
- **Latched Address and Data**
- **Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Word-Program Time: 14 µs (typical)
  - Chip Rewrite Time: 8 seconds (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
  - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Conforms to Common Flash Memory Interface (CFI)**
- **Packages Available**
  - 56-ball LFBGA (8mm x 10mm)

PRODUCT DESCRIPTION

The SST34HF1621/1641 ComboMemory devices integrate a 1M x16 CMOS flash memory bank with a 256K x8/ 128K x16 or 512K x8/ 256K x16 CMOS SRAM memory bank in a Multi-Chip Package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF1621/1641 devices are ideal for applications such as cellular phones, GPSs, PDAs and other portable electronic devices in a low power and small form factor system.

The SST34HF1621/1641 features dual flash memory bank architecture allowing for concurrent operations between the two flash memory banks and the SRAM. The devices can read data from either bank while an Erase or Program operation is in progress in the opposite bank. The two flash memory banks are partitioned into 4 Mbit and 12 Mbit with top or bottom sector protection options for storing boot code, program code, configuration/parameter data and user data.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF1621/1641 devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years. With high performance Word-Program, the flash memory banks provide a typical Word-Program time of 14 µsec. The entire flash memory bank can be erased and programmed word-by-word in typically 8 seconds for the SST34HF1621/1641, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST34HF1621/1641 devices contain on-chip hardware and software data protection schemes.

www.DataS

The SST logo and SuperFlash are registered trademarks of Silicon Storage Technology, Inc.
Concurrent SuperFlash, CSF, and ComboMemory are trademarks of Silicon Storage Technology, Inc.
These specifications are subject to change without notice.

The flash and SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The SRAM bank enable signal, BES1# and BES2, selects the SRAM bank. The flash memory bank enable signal, BEF#, has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area. Bus contention is eliminated as the device will not recognize both bank enables as being simultaneously active.

Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF1621/1641 are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements.

Device Operation

The SST34HF1621/1641 uses BES1#, BES2 and BEF# to control operation of either the flash or the SRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES1# is low, and BES2 is high the SRAM is activated for Read and Write operation. BEF# and BES1# cannot be at low level, and BES2 cannot be at high level at the same time. If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage. All address, data, and control lines are shared by flash and SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES1# bank enables are raised to V_{IHC} (Logic High) or when BEF# is high and BES2 is low.

Concurrent Read/Write Operation

Dual bank architecture of SST34HF1621/1641 devices allows the Concurrent Read/Write operation whereby the user can read from one bank while program or erase in the other bank. This operation can be used when the user needs to read system code in one bank while updating data in the other bank. See Figure 1 for Dual-Bank Memory Organization.

CONCURRENT READ/WRITE STATE TABLE

Flash		
Bank 1	Bank 2	SRAM
Read	Write	No Operation
Write	Read	No Operation
Write	No Operation	Read
No Operation	Write	Read
Write	No Operation	Write
No Operation	Write	Write

Note: For the purposes of this table, write means to Block-, Sector, or Chip-Erase, or Word-Program as applicable to the appropriate bank.

Flash Read Operation

The Read operation of the SST34HF1621/1641 is controlled by BEF# and OE#, both have to be low for the system to obtain data from the outputs. BEF# is used for device selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 6).

Flash Word-Program Operation

The SST34HF1621/1641 are programmed on a word-by-word basis. Before Program operations, the memory must be erased first. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed typically within 10 µs. See Figures 7 and 8 for WE# and BEF# controlled Program operation timing diagrams and Figure 21 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Flash Sector/Block-Erase Operation

The Sector/Block-Erase operation allows the system to erase the device on a sector-by-sector or block-by-block basis. The SST34HF1621/1641 offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 1 KWord. The Block-Erase mode is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. See Figures 12 and 13 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Flash Chip-Erase Operation

The SST34HF1621/1641 provide a Chip-Erase operation, which allows the user to erase all unprotected sectors/blocks to the "1" state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 24 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Flash Write Operation Status Detection

The SST34HF1621/1641 provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) pin. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), Data# Polling (DQ_7) or Toggle Bit (DQ_6) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Ready/Busy# (RY/BY#)

The SST34HF1621/1641 includes a Ready/Busy# (RY/BY#) output signal. RY/BY# is actively pulled low during internal Program/Erase operation. The status of RY/BY# is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Bank-Erase, the RY/BY# is valid after the rising edge of sixth WE# or (CE#) pulse. RY/BY# is an open drain output that allows several devices to be tied in parallel to V_{DD} via an external pull up resistor. Ready/Busy# is in high impedance whenever OE# or CE# is high or RST# is low.

Flash Data# Polling (DQ_7)

When the SST34HF1621/1641 are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling (DQ_7) is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling (DQ_7) is valid after the rising edge of sixth WE# (or BEF#) pulse. After the completion of a Program operation, Data# Polling on DQ_7 remains active and the device may not return to the Read mode for approximately 1 µs. See Figure 9 for Data# Polling (DQ_7) timing diagram and Figure 22 for a flowchart.

Flash Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. After the completion of a Program operation, DQ_6 will stop toggling for approximately 1 µs. The device is then ready for the next operation. The Toggle Bit (DQ_6) is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit (DQ_6) is valid after the rising edge of sixth WE# (or BEF#) pulse. See Figure 10 for Toggle Bit timing diagram and Figure 22 for a flowchart.

Data Protection

The SST34HF1621/1641 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF1621/1641 provide a hardware block protection which protects the outermost 4 KWord in the larger bank.The block is protected when WP# is held low. See Figure 1 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 18). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 17).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST34HF1621/1641 provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HP1621/1641 are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ_{15}-DQ_8 are "Don't Care" during any SDP command sequence.

Common Flash Memory Interface (CFI)

The SST34HF1621/1641 also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as Software ID Entry command with 98H (CFI Query command) to address 555H in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 5 through 7. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Product Identification

The Product Identification mode identifies the devices as the SST34HF1621/1641 and manufacturer as SST. This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin A_9 may damage this device. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 3 and 4 for software operation, Figure 14 for the software ID entry and read timing diagram and Figure 23 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	ADDRESS	DATA
Manufacturer's ID	0000H	00BFH
Device ID		
SST34HF1621	0001H	2761H
SST34HF1641	0001H	2761H

T1.2 523

Product Identification Mode Exit/ CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/ CFI Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 16 for timing waveform and Figure 23 for a flowchart.

SRAM Operation

With BES1# low, BES2 and BEF# high, the SST34HF162x operates as 256K x8 or 128K x16 CMOS SRAM, and the SST34HF164x operates as 512K x8 or 256K x16 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The CIOs pin configures the SRAM for x8 or x16 SRAM operation modes. The SST34HF162x SRAM is mapped into the first 256 KByte/128 KWord address space of the device, and the SST34HF164x SRAM is mapped into the first 512 KByte/256 KWord address space. When BES1#, BEF# are high and BES2 is low, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 3 for SRAM Read and Write data byte control modes of operation.

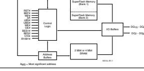
SRAM Read

The SRAM Read operation of the SST34HF1621/1641 is controlled by OE# and BES1#, both have to be low with WE# and BES2 high for the system to obtain data from the outputs. BES1# and BES2 are used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 3, for further details.

SRAM Write

The SRAM Write operation of the SST34HF1621/1641 is controlled by WE# and BES1#, both have to be low, BES2 have to be high for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES1#, WE#, or the falling edge of BES2 whichever occurs first. The write time is measured from the last falling edge of BES#1 or WE# or the rising edge of BES2 to the first rising edge of BES1#, or WE# or the falling edge of BES2. Refer to the Write cycle timing diagram, Figures 4 and 5, for further details.

FUNCTIONAL BLOCK DIAGRAM


A_{MS} - A_0
Address Buffers
SuperFlash Memory (Bank 1)
SuperFlash Memory (Bank 2)
RST#
BEF#
WP#
SA
LBS#
UBS#
WE#
OE#
BES1#
BES2
CIOs
RY/BY#
Control Logic
I/O Buffers
DQ_{15} - DQ_8
DQ_7 - DQ_0
Address Buffers
2 Mbit or 4 Mbit SRAM
[illegible]

A_{MS} = Most significant address

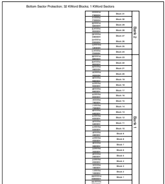

Bottom Sector Protection; 32 KWord Blocks; 1 KWord Sectors
FFFFFH F8000H Block 31
F7FFFH F0000H Block 30
EFFFFH E8000H Block 29
E7FFFH E0000H Block 28
DFFFFH D8000H Block 27
D7FFFH D0000H Block 26
CFFFFH C8000H Block 25
C7FFFH C0000H Block 24
Bank 2
BFFFFH B8000H Block 23
B7FFFH B0000H Block 22
AFFFFH A8000H Block 21
A7FFFH A0000H Block 20
9FFFFH 98000H Block 19
97FFFH 90000H Block 18
8FFFFH 88000H Block 17
87FFFH 80000H Block 16
7FFFFH 78000H Block 15
77FFFH 70000H Block 14
6FFFFH 68000H Block 13
67FFFH 60000H Block 12
5FFFFH 58000H Block 11
57FFFH 50000H Block 10
4FFFFH 48000H Block 9
47FFFH 40000H Block 8
3FFFFH 38000H Block 7
37FFFH 30000H Block 6
2FFFFH 28000H Block 5
27FFFH 20000H Block 4
1FFFFH 18000H Block 3
17FFFH 10000H Block 2
00FFFFH 008000H Block 1
007FFFH 001000H
000FFFH 000000H Block 0
Bank 1
4 KWord Sector Protection
(Four 1 KWord Sectors)
523 ILL F02.1

FIGURE 1: SST34HF1621/1641, 1 MBIT x 16 CONCURRENT SUPERFLASH DUAL-BANK MEMORY ORGANIZATION

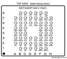


FIGURE 2: PIN ASSIGNMENTS FOR 56-BALL LFBGA (8MM X 10MM) COMBOMEMORY PINOUT

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1] to A_0	Address Inputs	To provide flash address, A_{19}-A_0. To provide SRAM address, A_{16}-A_0 for 2M and A_{17}-A_0 for 4M
SA	Address Input (SRAM)	To provide SRAM address input in byte mode (x8). When CIOs is V_{IL}, the SRAM is in Byte mode and SA provides the most significant address input. When CIOs is V_{IH}, the SRAM is in Word mode and SA becomes a Don't Care pin.
DQ_{15}-DQ_0	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# is high or BES1# is high or BES2 is low and BEF# is high.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low
BES1#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES1# is low
BES2	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES2 is high
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
UBS#	Upper Byte Control (SRAM)	To enable DQ_{15}-DQ_8
LBS#	Lower Byte Control (SRAM)	To enable DQ_7-DQ_0
CIOs	I/O Configuration (SRAM)	CIOs = V_{IH} is Word mode (x16), CIOs = V_{IL} is Byte mode (x8)
WP#	Write Protect	To protect and unprotect sectors from Erase or Program operation
RST#	Reset	To Reset and return the device to Read mode
RY/BY#	Ready/Busy#	To output the status of a Program or Erase Operation RY/BY# is a open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.
V_{SS}	Ground	
V_{DDF}	Power Supply (Flash)	2.7-3.3V Power Supply to Flash only
V_{DDS}	Power Supply (SRAM)	2.7-3.3V Power Supply to SRAM only
NC	No Connection	Unconnected pins

T2.6 523

1. A_{MS} = Most Significant Address

TABLE 3: OPERATIONAL MODES SELECTION[1]

Mode	BEF#	BES1#	BES2[2]	CIOs[3]	OE#	WE#	SA	LBS#	UBS#	DQ_{0-7}	DQ_{8-15}
Full Standby	V_{IH}	V_{IH}	X	X	X	X	X	X	X	HIGH-Z	HIGH-Z
		X	V_{IL}	X	X	X	X	X	X		
Output Disable	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}	X	X	X	HIGH-Z	HIGH-Z
		V_{IL}	V_{IH}	V_{IH}	X	X	X	V_{IH}	V_{IH}		
	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IH}	X	X	X	HIGH-Z	HIGH-Z
		X	V_{IL}								
Flash Read	V_{IL}	V_{IH}	X	X	V_{IL}	V_{IH}	X	X	X	D_{OUT}	D_{OUT}
		X	V_{IL}								
Flash Write	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IL}	X	X	X	D_{IN}	D_{IN}
		X	V_{IL}								
Flash Erase	V_{IL}	V_{IH}	X	X	V_{IH}	V_{IL}	X	X	X	X	X
		X	V_{IL}								
SRAM Read	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	D_{OUT}	D_{OUT}
								V_{IH}	V_{IL}	HIGH-Z	D_{OUT}
								V_{IL}	V_{IH}	D_{OUT}	HIGH-Z
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	SA	X	X	D_{OUT}	HIGH-Z
SRAM Write	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	X	V_{IL}	V_{IL}	D_{IN}	D_{IN}
								V_{IH}	V_{IL}	HIGH-Z	D_{IN}
								V_{IL}	V_{IH}	D_{IN}	HIGH-Z
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	SA	X	X	D_{IN}	HIGH-Z
Product Identification[4]	V_{IL}	V_{IH}	X	X	V_{IL}	V_{IH}	X	X	X	Manufacturer's ID[5] Device ID[5]	
		X	V_{IL}								

T3.4 [illegible]

1. X can be V_{IL} or V_{IH}, but no other value.
2. Do not apply BEF# = V_{IL}, BES1# = V_{IL} and BES2 = V_{IH} at the same time
3. SRAM I/O configuration input CIOs: V_{IH} = x16 (word mode), V_{IL} = x8 (byte mode)
4. Software mode only
5. With A_{19}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0,
   SST34HF1621/1641 Device ID = 2761H, is read with A_0 = 1

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[4]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_X[4]	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[5,6]	5555H	AAH	2AAAH	55H	5555H	90H						
CFI Query Entry[5]	5555H	AAH	2AAAH	55H	5555H	98H						
Software ID Exit/ CFI Exit[6]	5555H	AAH	2AAAH	55H	5555H	F0H						

T4.4 520

1. Address format A_{14}-A_0 (Hex),Address A_{15}-A_{19} can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. Data format DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for Command sequence.
3. WA = Program Word address
4. SA_X for Sector-Erase; uses A_{19}-A_{11} address lines
   BA_X for Block-Erase; uses A_{19}-A_{15} address lines
5. The device does not remain in Software Product Identification mode if powered down.
6. With A_{19}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0 = 0
   SST34HF1621/1641 Device ID = 2761H, is read with A_0 = 1.

TABLE 5: CFI QUERY IDENTIFICATION STRING[1]

Address	Data	Data
10H	0051H	Query Unique ASCII string "QRY"
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set
14H	0007H	
15H	0000H	Address for Primary Extended Table
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	0000H	

T5.0 520

1. Refer to CFI publication 100 for more details.

TABLE 6: SYSTEM INTERFACE INFORMATION

Address	Data	Data
1BH	0027H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	0036H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	0000H	V_{PP} Min (00H = no V_{PP} pin)
1EH	0000H	V_{PP} Max (00H = no V_{PP} pin)
1FH	0004H	Typical time out for Word-Program 2^N µs (24 = 16 µs)
20H	0000H	Typical time out for Min size buffer program 2^N µs (00H = not supported)
21H	0004H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	0006H	Typical time out for Chip-Erase 2^N ms (2^6 = 64 ms)
23H	0001H	Maximum time out for Word-Program 2^N times typical ($2^1 \times 2^4$ = 32 µs)
24H	0000H	Maximum time out for buffer program 2^N times typical
25H	0001H	Maximum time out for individual Sector/Block-Erase 2^N times typical ($2^1 \times 2^4$ = 32 ms)
26H	0001H	Maximum time out for Chip-Erase 2^N times typical ($2^1 \times 2^6$ = 128 ms)

T6.0 525

TABLE 7: DEVICE GEOMETRY INFORMATION

Address	Data	Data
27H	0015H	Device size = 2^N Byte (15H = 21; 2^{21} = 2M Bytes)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	Maximum number of byte in multi-byte write = 2^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Sector/Block sizes supported by device
2DH	00FFH	Sector Information (y + 1 = Number of sectors; z x 256B = sector size)
2EH	0003H	y = 1023 + 1 = 1024 sectors (03FF = 1023)
2FH	0008H	
30H	0000H	z = 8 x 256 Bytes = 2 KByte/sector (0008H = 8)
31H	001FH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	0000H	y = 31 + 1 = 32 blocks (001F = 31)
33H	0000H	
34H	0001H	z = 256 x 256 Bytes = 64 KByte/block (0100H = 256)

T7.0 525

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . -20°C to +85°C
Storage Temperature . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . -0.5V to V_{DD}[1]+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . -1.0V to V_{DD}[1]+1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . 240°C
Output Short Circuit Current[2] . . . . 50 mA

1. $V_{DD} = V_{DDF}$ and V_{DDS}
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 19 and 20	

TABLE 8: DC OPERATING CHARACTERISTICS (V_{DD} = V_{DDF} AND V_{DDS} = 2.7-3.3V)

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{DD}	Active V_{DD} Current				Address input=V_{IL}/V_{IH}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		35	mA	BEF#=V_{IL}, BES1#=V_{IH} or BES2=V_{IL}
	SRAM		20	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
	Concurrent Operation		60	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
	Write[1]				
	Flash		40	mA	BEF#=V_{IL}, BES1#=V_{IH}, or BES2=V_{IL}, OE#=V_{IH}
	SRAM		20	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
I_{SB}	Standby V_{DD} Current 3.0V		40	µA	V_{DD} = V_{DD} Max, BEF#=BES1#=V_{IHC}, BES2=V_{ILC}
	3.3V		75	µA	
I_{ALP}	Auto Low Power Mode 3.0V		40	µA	V_{DD}=V_{DD} Max, BEF#=V_{ILC}, WE#=V_{IHC}
	3.3V		75	µA	All I/O=V_{ILC}/V_{IHC}
I_{RT}	Reset V_{DD} Current		30	µA	Reset=V_{SS}±0.3V
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	V_{DD}=V_{DD} Max
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OLF}	Flash Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OHF}	Flash Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min
V_{OLS}	SRAM Output Low Voltage		0.4	V	IOL =1 mA, V_{DD}=V_{DD} Min
V_{OHS}	SRAM Output High Voltage	2.2		V	IOH =-500 µA, V_{DD}=V_{DD} Min

T8.6 520

1. I_{DD} active while Erase or Program is in progress.

TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU\text{-}READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU\text{-}WRITE}$[1]	Power-up to Write Operation	100	µs

T9.1 520

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: CAPACITANCE (T_A = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T10.0 520

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11: FLASH RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T11.1 520

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 12: SRAM READ CYCLE TIMING PARAMETERS

Symbol	Parameter	SST34HF1621/1641-70		SST34HF1621/1641-90		Units
		Min	Max	Min	Max	
T_{RCS}	Read Cycle Time	70		90		ns
T_{AAS}	Address Access Time		70		90	ns
T_{BES}	Bank Enable Access Time		70		90	ns
T_{OES}	Output Enable Access Time		35		45	ns
T_{BYES}	UBS#, LBS# Access Time		70		90	ns
T_{BLZS}[1]	BES# to Active Output	0		0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		0		ns
T_{BYLZS}[1]	UBS#, LBS# to Active Output	0		0		ns
T_{BHZS}[1]	BES# to High-Z Output		25		35	ns
T_{OHZS}[1]	Output Disable to High-Z Output		25		35	ns
T_{BYHZS}[1]	UBS#, LBS# to High-Z Output		35		45	ns
T_{OHS}	Output Hold from Address Change	10		10		ns

T12.3 520

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: SRAM WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	SST34HF1621/1641-70		SST34HF1621/1641-90		Units
		Min	Max	Min	Max	
T_{WCS}	Write Cycle Time	70		90		ns
T_{BWS}	Bank Enable to End-of-Write	60		80		ns
T_{AWS}	Address Valid to End-of-Write	60		80		ns
T_{ASTS}	Address Set-up Time	0		0		ns
T_{WPS}	Write Pulse Width	60		80		ns
T_{WRS}	Write Recovery Time	0		0		ns
T_{BYWS}	UBS#, LBS# to End-of-Write	60		80		ns
T_{ODWS}	Output Disable from WE# Low		30		40	ns
T_{OEWS}	Output Enable from WE# High	0		0		ns
T_{DSS}	Data Set-up Time	30		40		ns
T_{DHS}	Data Hold from Write Time	0		0		ns

T13.3 520

TABLE 14: FLASH READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST34HF1621/1641-70		SST34HF1621/1641-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}[1]	BEF# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	BEF# High to High-Z Output		20		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns
T_{RP}[1]	RST# Pulse Width	500		500		ns
T_{RHR}[1]	RST# High Before Read	50		50		ns
T_{RY}[1,2]	RST# Pin Low to Read		150		150	µs

T14.4 520

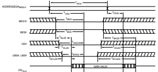
1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase and Block-Erase operations. This parameter does not apply to Chip-Erase operations.

TABLE 15: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and BEF# Setup Time	0		ns
T_{CH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{BY}[1]	RY/BY# Delay Time	90		ns
T_{BR}	Bus Recovery Time		1	µs
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

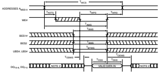
T15.3 520

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.


T_{RCS}
ADDRESSES A_{MSS-0}
T_{AAS}
T_{OHS}
BES1#
T_{BES}
BES2
T_{BES}
T_{BLZS}
T_{BHZS}
OE#
T_{OES}
T_{OLZS}
T_{OHZS}
UBS#, LBS#
T_{BYES}
T_{BYLZS}
T_{BYHZS}
DQ_{15-0}
DATA VALID
520 ILL F15.0

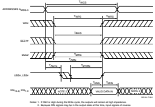
A_{MSS} = Most Significant SRAM Address

FIGURE 3: SRAM Read Cycle Timing Diagram


T_{WCS}
ADDRESSES A_{MSS-0}
T_{ASTS}
T_{WPS}
T_{WRS}
WE#
T_{AWS}
T_{BWS}
BES1#
BES2
T_{BWS}
T_{BYWS}
UBS#, LBS#
T_{ODWS}
T_{OEWS}
T_{DSS}
T_{DHS}
DQ_{15-8}, DQ_{7-0}
NOTE 2
VALID DATA IN
NOTE 2
520 ILL F16.2

Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES1# goes Low or BES2 goes high coincident with or after WE# goes Low, the output will remain at high impedance.
If BES1# goes High or BES2 goes low coincident with or before WE# goes High, the output will remain at high impedance.
Because DIN signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 4: SRAM Write Cycle Timing Diagram (WE# Controlled)[1]


TWCS
ADDRESSES AMSS-0
TWPS
TWRS
WE#
TBWS
BES1#
BES2
TBWS
TAWS
TASTS
TBYWS
UBS#, LBS#
TDSS
TDHS
DQ15-8, DQ7-0
NOTE 2
VALID DATA IN
NOTE 2
520 ILL F18.0

Notes: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because DIN signals may be in the output state at this time, input signals of reverse polarity must not be applied.

FIGURE 5: SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]

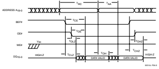
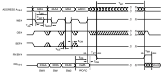
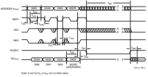

T_RC
T_AA
ADDRESS A19-0
BEF#
T_CE
OE#
T_OE
WE#
V_IH
T_OLZ
T_OHZ
DQ15-0
HIGH-Z
T_CLZ
T_OH
T_CHZ
DATA VALID
DATA VALID
HIGH-Z
523 ILL F06.0

FIGURE 6: Flash Read Cycle Timing Diagram


T_BP
ADDRESS A19-0
5555
2AAA
5555
ADDR
T_AH
T_WP
WE#
T_AS
T_WPH
OE#
BEF#
T_CH
T_CS
RY/BY#
T_BY
T_BR
T_DS
T_DH
DQ15-0
XXAA
XX55
XXA0
DATA
VALID
SW0
SW1
SW2
WORD
(ADDR/DATA)
523 ILL F05.3

Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 7: Flash WE# Controlled Word-Program Cycle Timing Diagram


ADDRESS A_{19-0}
BEF#
OE#
WE#
RY/BY#
DQ_{15-0}
5555
2AAA
5555
ADDR
T_{BP}
T_{AH}
T_{CP}
T_{AS}
T_{CPH}
T_{CH}
T_{CS}
T_{BY}
T_{BR}
T_{DS}
T_{DH}
XXAA
XX55
XXA0
DATA
VALID
SW0
SW1
SW2
WORD
(ADDR/DATA)
523 ILL F06.3

Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 8: FLASH BEF# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

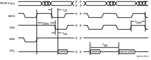

ADDRESS A_{19-0}
BEF#
OE#
WE#
DQ_7
T_{CE}
T_{OEH}
T_{OE}
T_{OES}
T_{BR}
DATA#
DATA#
VALID DATA
523 ILL F07.3

FIGURE 9: FLASH DATA# POLLING TIMING DIAGRAM

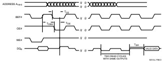
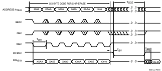
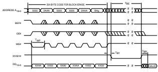

ADDRESS A_{19-0}
BEF#
OE#
WE#
DQ_6
T_{CE}
T_{OEH}
T_{OE}
T_{BR}
VALID DATA
TWO READ CYCLES WITH SAME OUTPUTS
523 ILL F08.3

FIGURE 10: FLASH TOGGLE BIT TIMING DIAGRAM


SIX-BYTE CODE FOR CHIP-ERASE
T_{SCE}
ADDRESS A_{19-0}
5555
2AAA
5555
5555
2AAA
555
BEF#
OE#
WE#
T_{WP}
RY/BY#
T_{BY}
T_{BR}
DQ_{15-0}
XXAA
XX55
XX80
XXAA
XX55
XX10
VALID
523 ILL F08.6

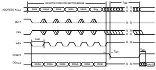
Note: This device also supports BEF# controlled Chip-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 15)
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 11: FLASH WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM


SIX-BYTE CODE FOR BLOCK-ERASE
TBE
ADDRESS A19-0
5555
2AAA
5555
5555
2AAA
BAX
BEF#
OE#
WE#
TWP
RY/BY#
TBY
TBR
DQ15-0
XXAA
XX55
XX80
XXAA
XX55
XX50
VALID
520 ILL F10.0

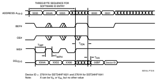
Note: This device also supports BEF# controlled Block-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 15)
BA_X = Block Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 12: Flash WE# Controlled Block-Erase Timing Diagram


SIX-BYTE CODE FOR SECTOR-ERASE
TSE
ADDRESS A19-0
5555
2AAA
5555
5555
2AAA
SAX
BEF#
OE#
WE#
TWP
RY/BY#
TBY
TBR
DQ15-0
XXAA
XX55
XX80
XXAA
XX55
XX30
VALID
520 ILL F11.0

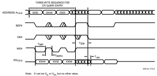
Note: This device also supports BEF# controlled Sector-Erase operation. The WE# and BEF# signals are interchageable as long as minimum timings are met. (See Table 15)
SA_X = Sector Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 13: Flash WE# Controlled Sector-Erase Timing Diagram


THREE-BYTE SEQUENCE FOR SOFTWARE ID ENTRY
ADDRESS A14-0
5555
2AAA
5555
0000
0001
BEF#
OE#
WE#
TWP
TWPH
TIDA
TAA
DQ15-0
XXAA
XX55
XX90
00BF
Device ID
523 ILL F12.6

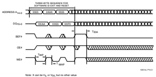
Device ID = 2761H for SST34HF1621 and 2761H for SST34HF1641
Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 14: Flash Software ID Entry and Read


THREE-BYTE SEQUENCE FOR CFI QUERY ENTRY
ADDRESS A14-0
5555
2AAA
5555
BEF#
OE#
WE#
TWP
TWPH
TIDA
TAA
DQ15-0
XXAA
XX55
XX98
523 ILL F13.2

Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 15: Flash CFI Entry and Read


THREE-BYTE SEQUENCE FOR SOFTWARE ID EXIT AND RESET
ADDRESS A_{14-0}
5555
2AAA
5555
DQ_{15-0}
XXAA
XX55
XXF0
BEF#
OE#
WE#
T_{WP}
T_{WHP}
T_{IDA}
520 ILL F14.3

Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 16: Flash Software ID Exit/CFI Exit

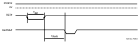

RY/BY#
0V
RST#
T_{RP}
CE#/OE#
T_{RHR}
520 ILL F29.0

FIGURE 17: RST# Timing (when no internal operation is in progress)

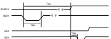
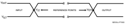

T_{RY}
RY/BY#
RST#
T_{RP}
CE#
OE#
T_{BR}
520 ILL F30.0

FIGURE 18: RST# Timing (during Sector- or Block-Erase operation)


V_{IHT}
V_{ILT}
INPUT
V_{IT}
REFERENCE POINTS
V_{OT}
OUTPUT
523 ILL F19.0

AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 19: AC INPUT/OUTPUT REFERENCE WAVEFORMS

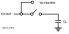
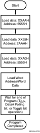

TO TESTER
TO DUT
C_L
523 ILL F20.0

FIGURE 20: A TEST LOAD EXAMPLE


Start
Load data: XXAAH
Address: 5555H
Load data: XX55H
Address: 2AAAH
Load data: XXA0H
Address: 5555H
Load Word
Address/Word
Data
Wait for end of
Program (T$_{BP}$,
Data# Polling
bit, or Toggle bit
operation)
Program
Completed
523 ILL F21.4

Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 21: WORD-PROGRAM ALGORITHM

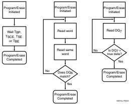
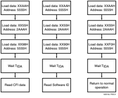
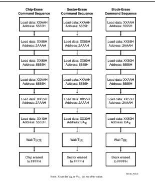

Internal Timer
Program/Erase Initiated
Wait TBP, TSCE, TSE or TBE
Program/Erase Completed
Toggle Bit
Program/Erase Initiated
Read word
Read same word
No
Does DQ6 match?
Yes
Program/Erase Completed
Data# Polling
Program/Erase Initiated
Read DQ7
No
Is DQ7 = true data?
Yes
Program/Erase Completed
520 ILL F22.0

FIGURE 22: WAIT OPTIONS


CFI Query Entry Command Sequence
Load data: XXAAH Address: 5555H
Load data: XX55H Address: 2AAAH
Load data: XX98H Address: 5555H
Wait T_{IDA}
Read CFI data
Software Product ID Entry Command Sequence
Load data: XXAAH Address: 5555H
Load data: XX55H Address: 2AAAH
Load data: XX90H Address: 5555H
Wait T_{IDA}
Read Software ID
Software ID Exit/CFI Exit Command Sequence
Load data: XXAAH Address: 5555H
Load data: XX55H Address: 2AAAH
Load data: XXF0H Address: 5555H
Wait T_{IDA}
Return to normal operation
523 ILL F23.3

Note: X can be V_{IL} or V_{IH}, but no other value.

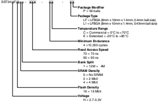
FIGURE 23: SOFTWARE PRODUCT ID/CFI COMMAND FLOWCHARTS


Chip-Erase Command Sequence
Sector-Erase Command Sequence
Block-Erase Command Sequence
Load data: XXAAH Address: 5555H
Load data: XX55H Address: 2AAAH
Load data: XX80H Address: 5555H
Load data: XXAAH Address: 5555H
Load data: XX55H Address: 2AAAH
Load data: XX10H Address: 5555H
Load data: XX30H Address: SA$_X$
Load data: XX50H Address: BA$_X$
Wait T$_{SCE}$
Wait T$_{SE}$
Wait T$_{BE}$
Chip erased to FFFFH
Sector erased to FFFFH
Block erased to FFFFH
523 ILL F24.2

Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 24: Erase Command Sequence

PRODUCT ORDERING INFORMATION



Package Modifier
P = 56 balls

Package Type
LF = LFBGA (8mm x 10mm x 1.4mm, 0.4mm ball size)
L1 = LFBGA (8mm x 10mm x 1.4mm, 0.45mm ball size)

Temperature Range
C = Commercial = 0°C to +70°C
E = Extended = -20°C to +85°C

Minimum Endurance
4 =10,000 cycles

Read Access Speed
70 = 70 ns
90 = 90 ns

Bank Split
1 = 12M + 4M

SRAM Density
0 = No SRAM
2 = 2 Mbit
4 = 4 Mbit

Flash Density
16 = 16 Mbit

Voltage
H = 2.7-3.3V

Valid combinations for SST34HF1621

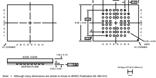
SST34HF1621-70-4C-LFP	SST34HF1621-70-4C-L1P
SST34HF1621-90-4C-LFP	SST34HF1621-90-4C-L1P
SST34HF1621-70-4E-LFP	SST34HF1621-70-4E-L1P
SST34HF1621-90-4E-LFP	SST34HF1621-90-4E-L1P

Valid combinations for SST34HF1641

SST34HF1641-70-4C-LFP	SST34HF1641-70-4C-L1P
SST34HF1641-90-4C-LFP	SST34HF1641-90-4C-L1P
SST34HF1641-70-4E-LFP	SST34HF1641-70-4E-L1P
SST34HF1641-90-4E-LFP	SST34HF1641-90-4E-L1P

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

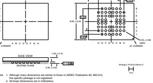
PACKAGING DIAGRAMS


TOP VIEW
8
7
6
5
4
3
2
1
A B C D E F G H
A1 CORNER
BOTTOM VIEW
10.00 ± 0.20
0.80
0.80
8.00 ± 0.20
0.80
0.80
8
7
6
5
4
3
2
1
H G F E D C B A
A1 CORNER
0.40 ± 0.05
(56X)
SIDE VIEW
1.30 ± 0.10
SEATING PLANE
0.32 ± 0.05
0.12
56-fbga-LFP-8x10-400mic-8
1mm

Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. The actual shape of the corners may be slightly different than as portrayed in the drawing.

56-ball Low-profile, Fine-pitch Ball Grid Array (LFBGA) 8mm x 10mm
SST Package Code: LFP

Note: This package will be replaced by L1P which increases the ball size from 400-micron to 450-micron. Check with factory for migration schedule.


TOP VIEW
8
7
6
5
4
3
2
1
A B C D E F G H
A1 CORNER
BOTTOM VIEW
10.00 ± 0.20
0.80
0.80
8.00 ± 0.20
0.80
0.80
8
7
6
5
4
3
2
1
H G F E D C B A
0.45 ± 0.05
(56X)
A1 CORNER
SIDE VIEW
1.30 ± 0.10
SEATING PLANE
0.35 ± 0.05
0.12
1mm

Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. The actual shape of the corners may be slightly different than as portrayed in the drawing.

56-ball Low-profile, Fine-pitch Ball Grid Array (LFBGA) 8mm x 10mm
SST Package Code: L1P