

PEMD24; PUMD24

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NPN/PNP resistor-equipped transistors;
R1 = 100 k Ω , R2 = 100 k Ω

Rev. 01 — 2 May 2005

Product data sheet

1. Product profile

1.1 General description

NPN/PNP Resistor-Equipped Transistors (RET).

Table 1: Product overview

Type number	Package		PNP/PNP complement	NPN/PNP complement
	Philips	JEITA		
PEMD24	SOT666	-	PEMB24	PEMH24
PUMD24	SOT363	SC-88	PUMB24	PUMH24

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

Table 2: Quick reference data

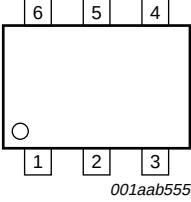
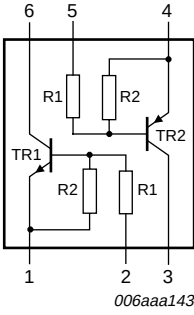
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current (DC)		-	-	20	mA
R1	bias resistor 1 (input)		70	100	130	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

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2. Pinning information

Table 3: Pinning

Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1	 001aab555	 006aaa143
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4: Ordering information

Type number	Package		
	Name	Description	Version
PEMD24	-	plastic surface mounted package; 6 leads	SOT666
PUMD24	SC-88	plastic surface mounted package; 6 leads	SOT363

4. Marking

Table 5: Marking codes

Type number	Marking code [1]
PEMD24	6N
PUMD24	T8*

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	50	V
V _{EBO}	emitter-base voltage	open collector	-	10	V
V _I	input voltage TR1				
	positive		-	+40	V
	negative		-	−10	V
	input voltage TR2				
	positive		-	+10	V
	negative		-	−40	V
I _O	output current (DC)		-	20	mA
I _{CM}	peak collector current		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363		[1] -	200	mW
	SOT666		[1] [2] -	200	mW
T _{stg}	storage temperature		−65	+150	°C
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		−65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT363		[1] -	300	mW
	SOT666		[1] [2] -	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	-	625 K/W
	SOT666		[1] [2]	-	-	625 K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	-	416 K/W
	SOT666		[1] [2]	-	-	416 K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

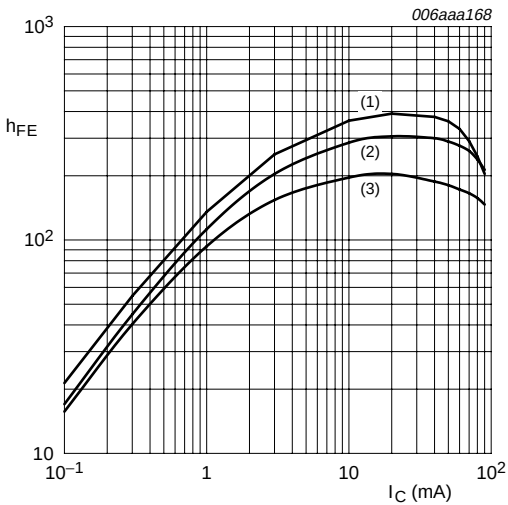
[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8: Characteristics

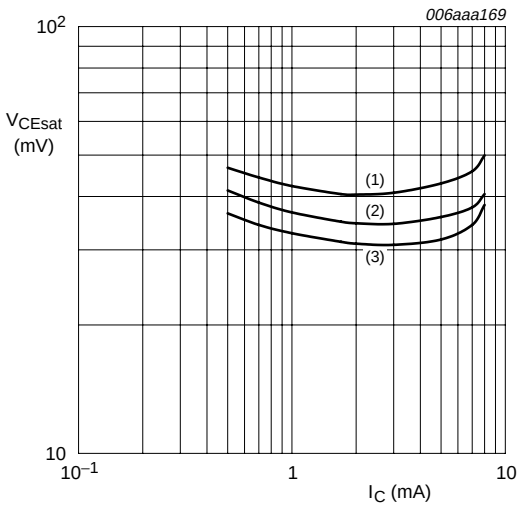
 $T_{amb} = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ °C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$	-	-	50	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}$; $I_B = 0.25\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ μA}$	-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 1\text{ mA}$	3	1.5	-	V
R1	bias resistor 1 (input)		70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = I_E = 0\text{ A}$; $f = 1\text{ MHz}$				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF



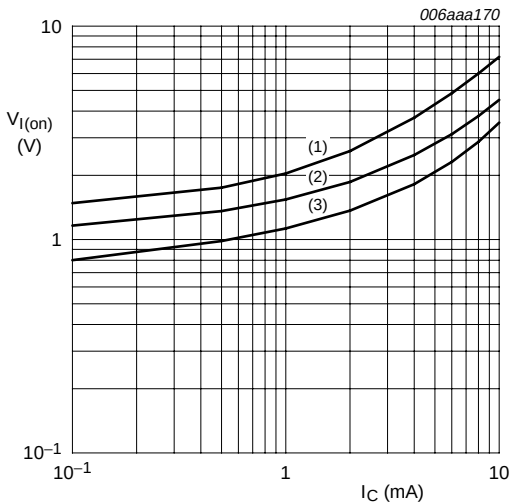
- $V_{CE} = 5\text{ V}$
(1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values



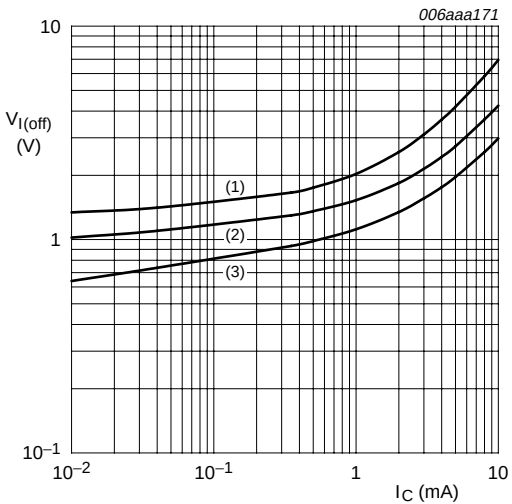
- $I_C/I_B = 20$
(1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



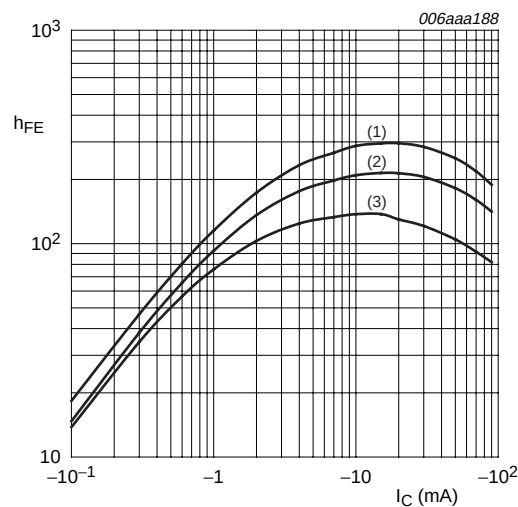
- $V_{CE} = 0.3\text{ V}$
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



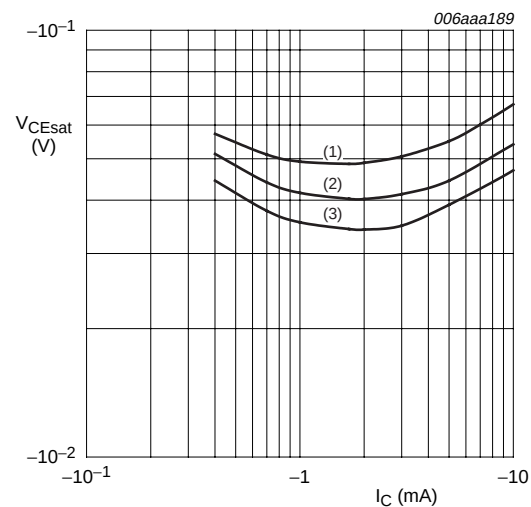
- $V_{CE} = 5\text{ V}$
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



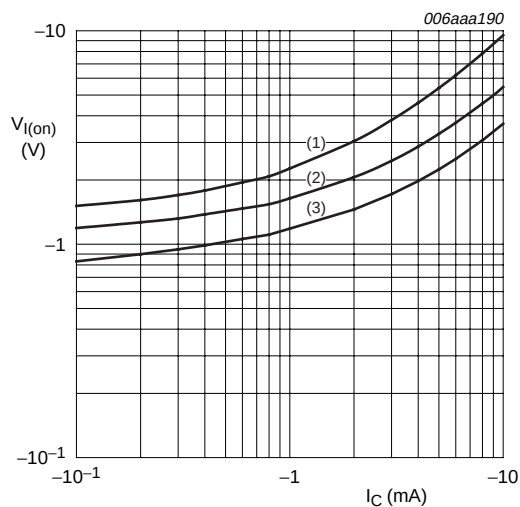
- $V_{CE} = -5$ V
- (1) $T_{amb} = 100$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = -40$ °C

Fig 5. TR2 (PNP): DC current gain as a function of collector current; typical values



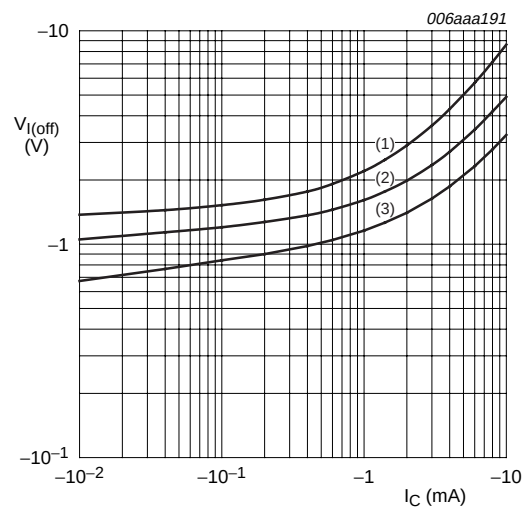
- $I_C/I_B = 20$
- (1) $T_{amb} = 100$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = -40$ °C

Fig 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = -0.3$ V
- (1) $T_{amb} = -40$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = 100$ °C

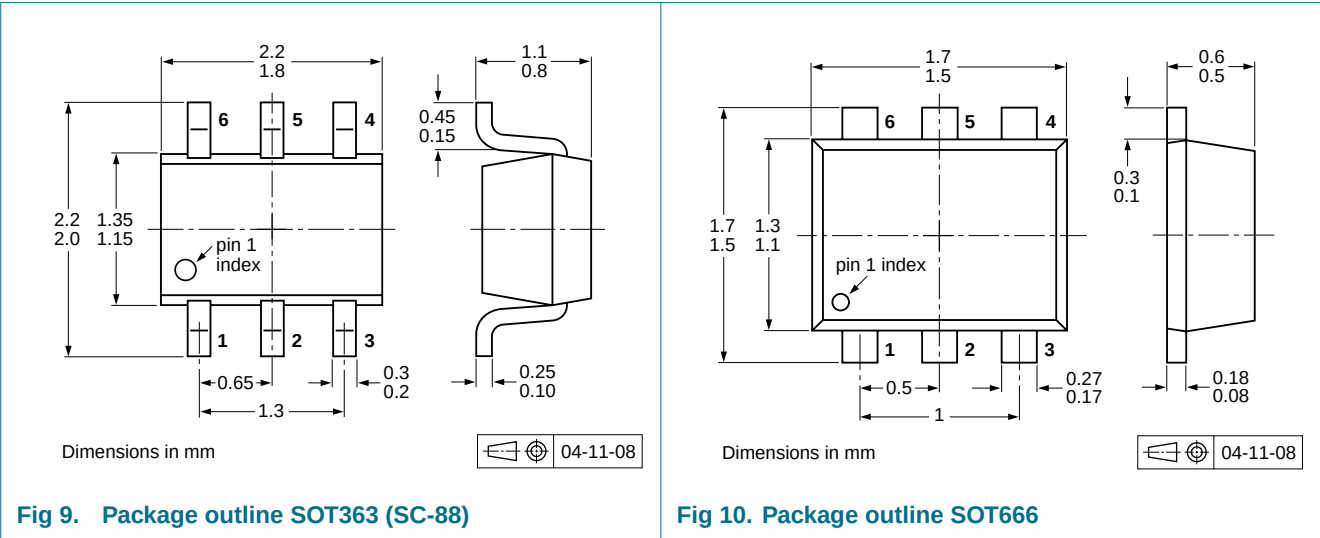
Fig 7. TR2 (PNP): On-state input voltage as a function of collector current; typical values



- $V_{CE} = -5$ V
- (1) $T_{amb} = -40$ °C
 - (2) $T_{amb} = 25$ °C
 - (3) $T_{amb} = 100$ °C

Fig 8. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

8. Package outline



9. Packing information

Table 9: Packing methods
The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD24	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMD24	SOT363	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 15](#).
[2] T1: normal taping
[3] T2: reverse taping

10. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PEMD24_PUMD24_1	20050502	Product data sheet	-	9397 750 14457	-

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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