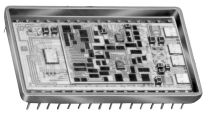


HIGH POWER 16-BIT D/R CONVERTER

DESCRIPTION

The DRC-10520 is a 16 bit, 32 pin triple DIP D/R converter with 2 VA drive capability. It features a power amplifier that may be driven by a standard ±15 VDC power supply or by the reference source (when used with the optional power transformer DDC/PN 29306). The DRC-10520 provides compatibility with microprocessors through its 8-bit 2-byte transparent input latch. Data input is natural binary angles in TTL compatible parallel positive logic format.

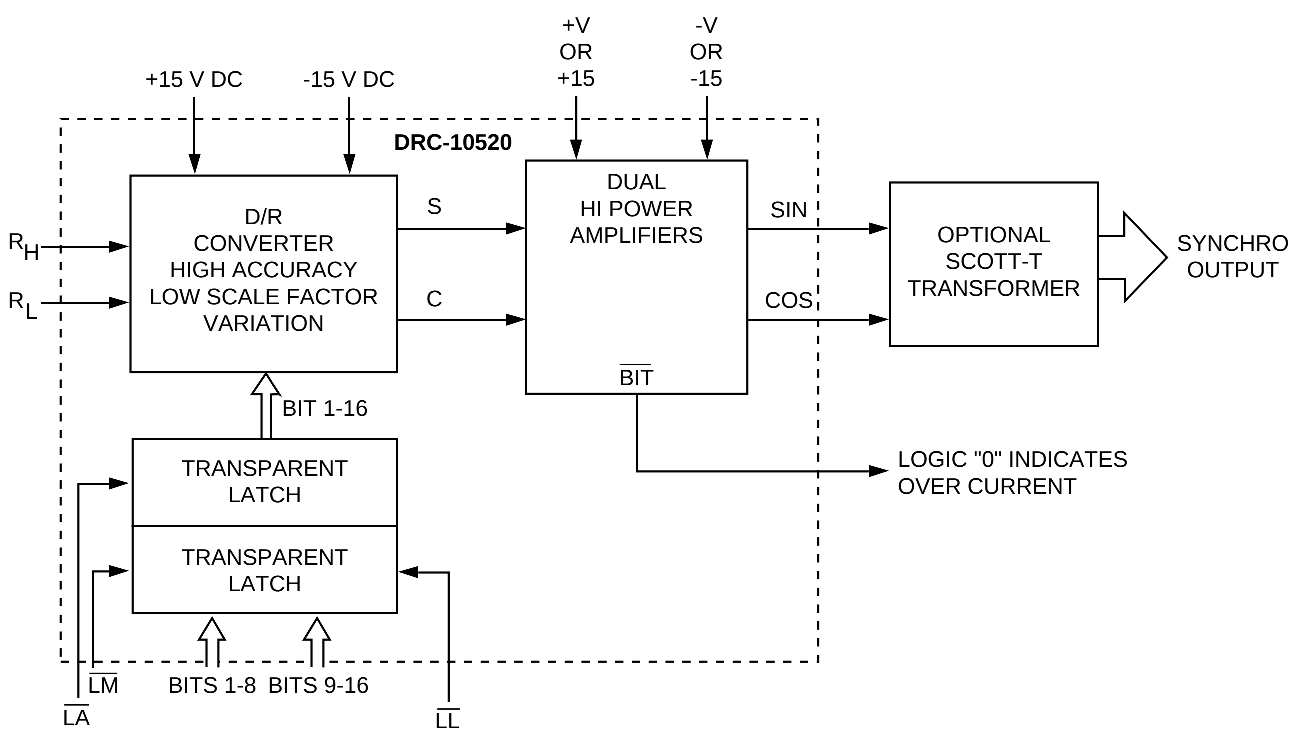
The DRC-10520 is comprised of a high accuracy D/R converter and a dual power amplifier stage that has high accuracy and low scale factor variation. In addition, a standard $\overline{BIT}$ circuit provides a digital overcurrent signal output. A logic "0" $\overline{BIT}$ output indicates an overcurrent condition in the sine or cosine outputs. Reference inputs are scalable with external resistors. Loss of the reference signal will not damage the converter.

APPLICATION

The DRC-10520 can be used where digitized shaft angle data must be converted to an analog format for driving control transformers. With its built-in input latches, the DRC-10520 is especially compatible with a microprocessor-based system including flight simulators, flight instrumentation, fire control systems, radar and navigation systems, and air data computers.

FEATURES

- ***2 VA Drive Capacity***
- ***8-Bit/2-Byte Double Buffered Transparent Latch***
- ***Resolution: 16 Bits Accuracy: to 1 Minute***
- ***Power Amplifier Uses AC Reference or DC Supplies***
- ***$\overline{BIT}$ Output***



DRC-10520 BLOCK DIAGRAM

TABLE 1. DRC-10520 SPECIFICATIONS Apply over temperature range power supply ranges reference voltage and frequency range and 10% harmonic distortion in the reference.	
PARAMETER	**VALUE**
RESOLUTION	16 bits
ACCURACY AND DYNAMICS	
Output Accuracy	
Without Scott-T	±1 or ±4 minutes
With Scott-T P/N29305	±10 minutes (1.5 VA min for CT load) ±16 minutes (2 VA min for CT load)
Differential Linearity	±1 LSB
Output Settling Time	Less than 40 µsec for any digital input step change
DIGITAL INPUT	
Logic Type	Natural binary angle parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected.
Logic Voltage level	Logic 0 = 0 to +1.25 V Logic 1 = 2 V to 5 V
Load Current	20 µA max to GND ($\overline{\text{bit 1-16}}$) 20 µA max to V_L ($\overline{LL}$ $\overline{LM}$ $\overline{LA}$)
Timing	See Timing Diagram (FIGURE 2).
REFERENCE INPUT	
Type	Differential 3.4 V rms
Voltage	Higher voltages are scaled by adding series resistors
Frequency	DC to 1 kHz
Input Impedance	
Single Ended	13 kΩ ±0.5%
Differential	26 kΩ ±0.5%
ANALOG OUTPUT	
Type	Resolver
Output Current	300 mA rms min (2 VA min)
Max Output Voltage (tracks reference input voltage)	6.8 V rms max line-to-line ±1%
Scale Factor Variation	Simultaneous amplitude variation in all output lines as function of digital angle is ±0.1% max.
DC Offset (each line to ground)	±15 mV max varies with input angle.
Protection	Output is protected from overcurrent short circuits and voltage feedback transients.
POWER SUPPLIES	
Voltage	+15 V | -15 V | +V | -V
Voltage Limits	+5% | +5% | 20 V peak max 3 V above output voltage min.
Max Voltage Without Damage	+18 V | -18 V | +25 V | -25 V
Current	20 mA max | 20 mA max | load dependent
Peak Current At Power Turn On or Short Circuit (when using Transformer)	700 mA max
TEMPERATURE RANGES	
Operating (-3xx)	0°C to +70°C case
(-1xx)	-55°C to +125°C case
Storage	-55°C to +135°C
PHYSICAL CHARACTERISTICS	
Package Type	32 pin triple DIP
Size	1.14 x 1.74 x 0.18 inch (29 x 44 x 4 mm)
Weight	1.15 oz (33 g)

TECHNICAL INFORMATION INTRODUCTION

The DRC-10520 is a digital-to-resolver (D/R) converter which has an inherently high accuracy and low scale factor variation. The circuit is based on an algorithm whose theoretical math error is only ±3.5 arc seconds and whose theoretical scale factor variation with angle is less than ±0.015%. Therefore accuracy and scale factor are limited only by the physical components, not by the algorithm.

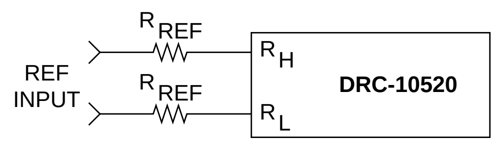
The digital inputs are CMOS double buffered transparent latches (FIGURE 1). Angular output is determined by adding bits in the logic 1 state.

REFERENCE LEVEL ADJUSTMENT

The input is specified for operation at a reference level of 3.4 V rms; however, reference levels other than 3.4 V rms may be scaied by calculating the value of the scaling resistor with the following equation:

$$R_{REF} = \frac{(V_{REF} - 3.4)}{3.4} \times 13k$$

eg., if V_{REF} = 26 V rms, then $R_{REF} = \frac{(26 - 3.4)}{3.4} \times 13k$



The output is 6.8 V rms line-to-line resolver format signal which may be converted into a synchro format of 11.8 V line-to-line with the companion Scott-T transformer module available as DDC P/N 29305.

DRIVING THE POWER AMPLIFIER WITH THE REFERENCE

The high power amplifier stage can be driven by a standard ±15 V DC supply or with a high efficiency pulsating power supply derived from the reference voltage source. A companion power transformer DDC P/N 29306, designed to implement the pulsating power source for the DRC-10520, is also available (FIGURE 3). The DRC-10520 will not be damaged by sequencing order in the ±15 V, V_L supplies or the reference input.

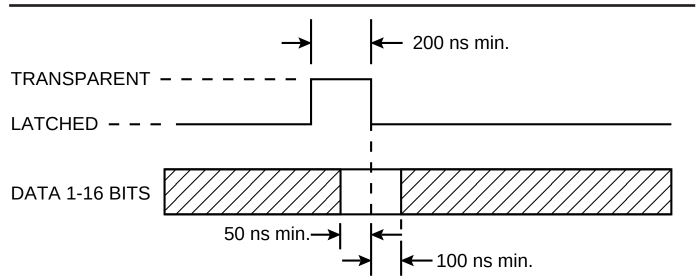


FIGURE 2. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAM

OUTPUT PROTECTION AND BIT

The output is protected from overcurrent, short circuits and voltage feedback transients. The BIT circuit detects overcurrent conditions in the sine or cosine resolver output. A logic “0” is used for overcurrent detection. Normal operation is logic “1.” The BIT line is normally at logic “1.” An overload or short circuit will cause the BIT line to drop after 1 sec when the output current exceeds a peak level of approximately 450 mA.

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

$$\sin = (R_H - R_L)\, A_O\, [1 + A(\theta)]\, \sin\theta$$
$$\cos = (R_H - R_L)\, A_O\, [1 + A(\theta)]\, \cos\theta$$

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (R_H-R_L). The amplitude factor A_O is 2 for 6.8 V rms L-L output. The maximum variation in A_O from all causes is 0.3%. The term A (θ) represents the variation of the amplitude with the digital input angle. A (θ), which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.1% for all values of θ. The total maximum variation in A_O [1 + A (θ)] is therefore ±0.4%.

Because the amplitude factor (R_H-R_L) A_O [1 + A (θ)] varies simultaneously on all output lines, it will not be a source of error when the DRC-10520 is to drive a ratiometric system such as a resolver or synchro. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

THERMAL CONSIDERATIONS

The power stage consists of two power amplifiers: one for the sine output and one for the cosine output. Maximum power stage junction temperature rise occurs at 0° and 180° for the sine output and 90° and 270° for the cosine output.

Maximum power dissipation for the hybrid occurs at the interquadrant points: 45°, 135°, 225°, and 315°. At these points the total power dissipation of each amplifier is 0.707 max. Therefore, the total power dissipation is 1.41 times the max for any one amplifier.

The thermal resistance junction to the outside of the case is 10.6°C/W. For a 2 VA purely inductive load and ±15 VDC power supplies, the junction temperature rise is 42°C. For a real inductive load (one that has some power dissipation) and using pulsating supplies, the power dissipated is cut in half. The temperature rise is also halved to 21°C.

TABLE 2. PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	N.C.	12	5	23	14
2	N.C.	13	6	24	RL
3	16 (LSB)	14	7	25	RH
4	COS	15	8	26	15
5	DIN	16	LM	27	-15 V
6	+V	17	LL	28	GND
7	-V	18	9	29	LA
8	1 (MSB)	19	10	30	+15 V
9	2	20	11	31	BIT
10	3	21	12	32	N.C.
11	4	22	13		

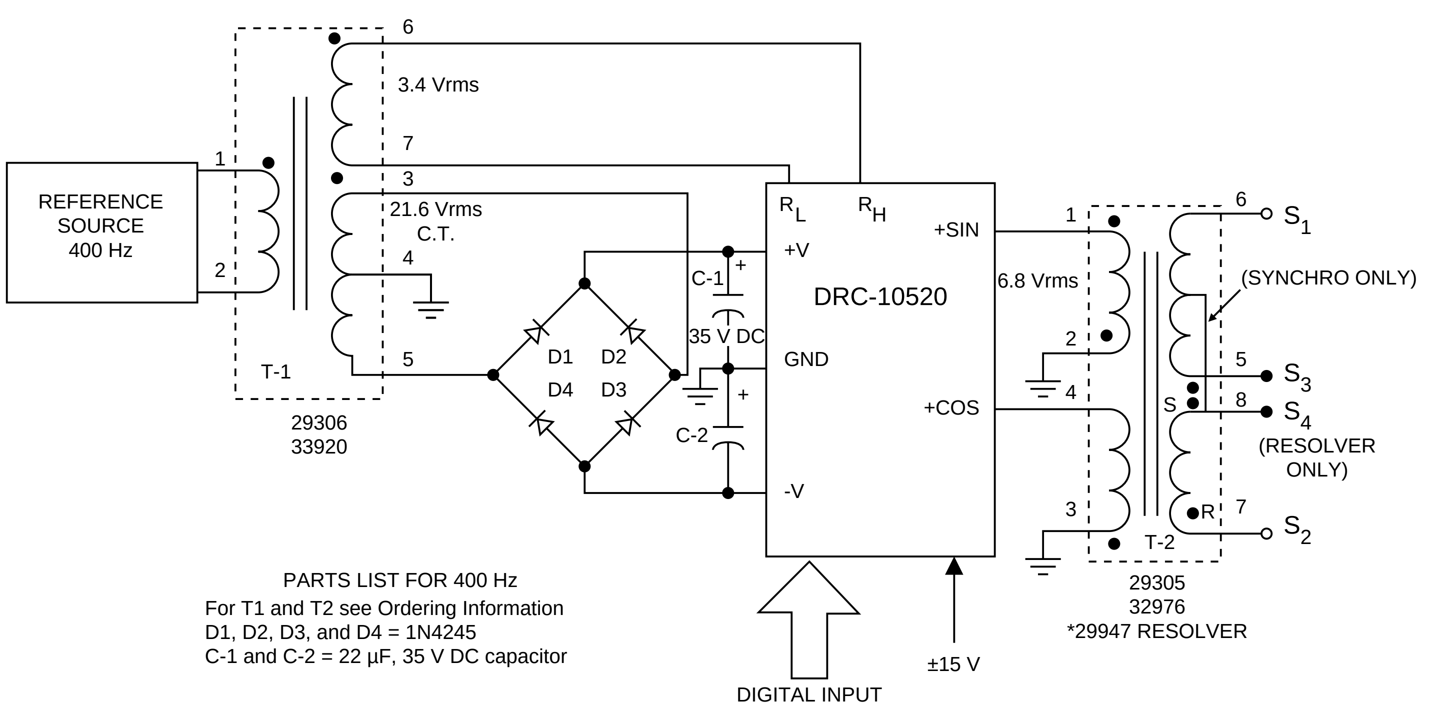


FIGURE 3. TYPICAL CONNECTION DIAGRAM UTILIZING PULSATING POWER SOURCE FOR SYNCHRO OUTPUT

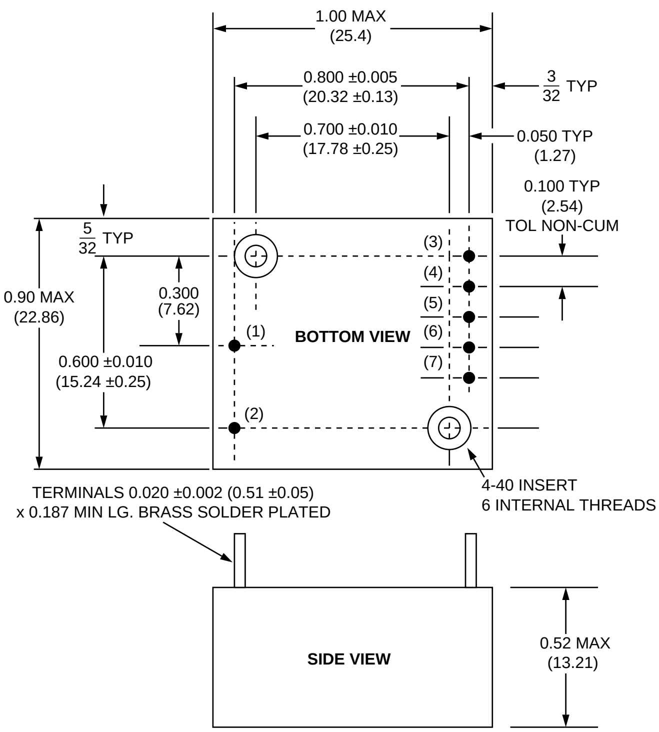


FIGURE 4. POWER TRANSFORMER (29306, 33920) MECHANICAL OUTLINE

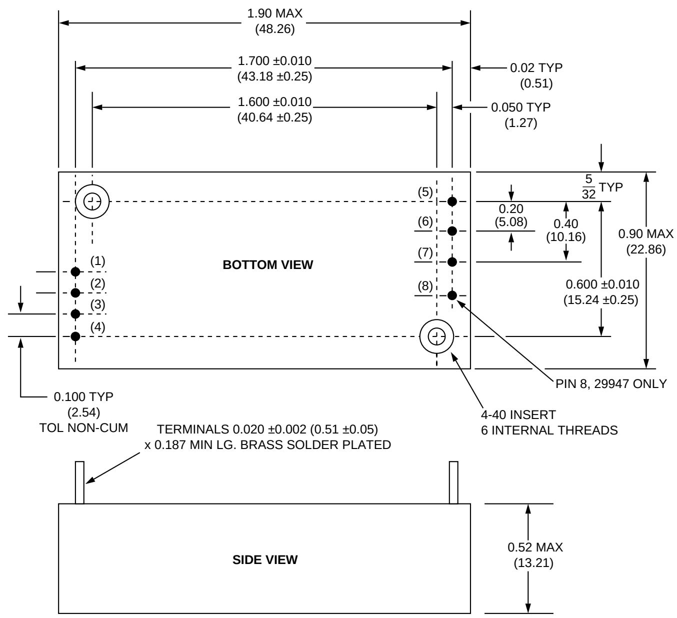
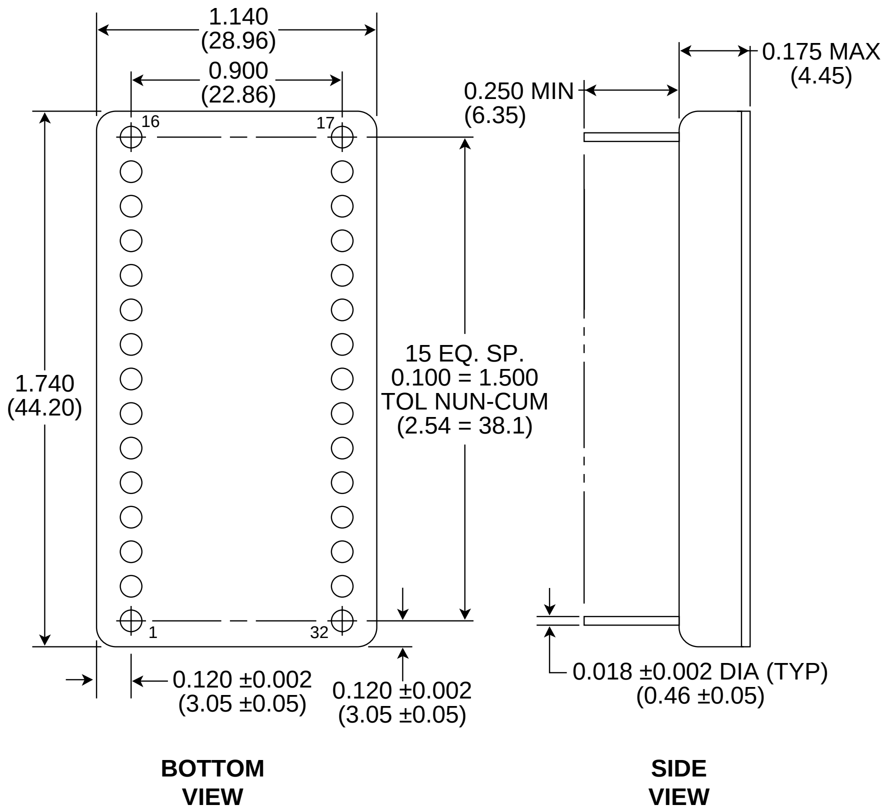


FIGURE 5. OUTPUT SCOTT-T TRANSFORMERS (29305, 29947, 32976) MECHANICAL OUTLINE

TABLE 3. TRANSFORMER INFORMATION

	POWER TRANSFORMER		SCOTT-T TRANSFORMER		
	29306	**33920**	**29305**	**29947**	**32976**
Freq. Range	400 Hz ±10% for all transformers				
Drive	2 VA for all transformers				
Input (1-2)	26 V	115 V	6.8 V	6.8 V	6.8 V
Output	see note 1	see note 1	Synchro 11.8 V L-L	Resolver 11.8 V L-L	Synchro 90 V L-L
Phase Shift	note 2	note 2	—	—	—
Rated Load (over -55 to +125°C)	—	—	1.1 VA 6 min; 2.0 VA 12 min	2.0 VA 2 min	1.1 VA 4 min
Dielectric withstanding volt. (between windings)	250 Vrms @ 60 Hz	500 Vrms @ 60 Hz	500 Vrms @ 60 Hz	500 Vrms @ 60 Hz	500 Vrms @ 60 Hz
Weight	1 oz.	1 oz.	2.0 oz.	2.0 oz.	2.0 oz.

Notes:
1. (3-4-5) 20.68 volts Centertapped, 7.5% Regualtion over temperature range.
(6-7) 3.4 volts, 5% Regulation over temperature range.
2. Max from winding 1-2 to 6-7 is 5° for ambient temperature -55 to +125°C.



NOTES:
1. Dimensions shown are in inches (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.010 (±2.54) of outline dimensions.
   Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-PRF-38534, Method 2003.
5. Tol ±0.005 (±0.13) unless otherwise noted.

FIGURE 6. DRC-10520 MECHANICAL OUTLINE (32 PIN TRIPLE DIP)

ORDERING INFORMATION

DRC-10520-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Accuracy:
- 3 = ±4 Minutes
- 4 = ±2 Minutes
- 5 = ±1 Minute

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C (Case)
- 2 = -40°C to +85°C (Case)
- 3 = 0°C to +70°C (Case)
- 4 = -55°C to +125°C (Case) with Variables Test Data
- 5 = -40°C to +85°C (Case) with Variables Test Data
- 8 = 0°C to +70°C (Case) with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

DDC™
©Data Device Corporation
105 Wilbur Place, Bohemia, New York 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7389 or 7413

Headquarters - Tel: (631) 567-5600 ext. 7389 or 7413, Fax: (631) 567-7358
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
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