m i c r o e l e c t r o n i c s g r o u p

Lucent Technologies
Bell Labs Innovations

Ambassador™ T8102
H.100/H.110 Interface and Time-Slot Interchanger

Features

- Complete solution for interfacing board-level circuitry to the H.100/H.110 telephony bus

- H.100/H.110 compliant interface; all mandatory signals

- Includes 2 CT_NETREF pins

- Programmable connections to any of the 4096 time slots on the H.100/H.110 bus

- Up to 16 local serial inputs and 16 local serial outputs, programmable for 2.048 Mbits/s, 4.096 Mbits/s, and 8.192 Mbits/s operation per CHI specifications

- Programmable switching between local time slots and H.100/H.110 bus, up to 512 connections

- Choice of frame integrity or minimum latency switching on a per-time-slot basis:
  — Frame integrity to ensure proper switching of wideband data
  — Minimum latency switching to reduce delay in voice channels

- On-chip phase-locked loop (PLL) for H.100/H.110, *MVIP**, or *Dialogic*'s† SC-bus clock operation in master or slave clock modes

- Serial TDM bus rate and format conversion between most standard buses

- Optional 8-bit parallel input and/or 8-bit parallel output for local TDM interfaces

- High-performance microprocessor interface:
  — Provides access to device configuration registers and to time-slot data
  — Supports both *Motorola*‡ nonmultiplexed and *Intel*§ multiplexed/nonmultiplexed modes

- Subrate switching of nibbles, dibits, or bits

- Programmable GPIO

- Local-to-local switching through the H-bus content addressable memories (CAMs)

- Two independently programmable groups of up to 12 framing signals each

- 3.3 V local I/O with 5 V tolerant inputs and TTL-compatible outputs

- Boundary-scan testing support

- 208-pin, plastic SQFP

- 217-pin BGA package

Applications

- Computer-telephony systems

- Enhanced service platforms

- WAN access devices

- PBXs

Description

The *Ambassador* T8102 is an H.100/H.110-compliant device that provides a complete interface between the H.100/H.110 bus and a wide variety of telephony interface components, processors, and other circuits. The bus interface provides all signals needed for the H.100/H.110 bus, the H-*MVIP* and *MVIP*-90 buses, or the SC-bus. Local interfaces include sixteen serial inputs and sixteen serial outputs based on the Lucent concentration highway interface (CHI). One built-in time-slot interchanger is included. It supports up to 512 programmable connections between any time slot on the H.100/H.110 bus and any time slot in the local switching domain. The *Ambassador* T8102 is configured via a microprocessor interface. This interface can also read and write time-slot and device data.

* *MVIP* is a trademark of Natural MicroSystems Corporation.
† *Dialogic* is a registered trademark of Dialogic Corporation.
‡ *Motorola* is a registered trademark of Motorola, Inc.
§ *Intel* is a registered trademark of Intel Corporation.

Description (continued)

Onboard clock circuitry, including a digital phase-locked loop, supports all H.100/H.110 clock modes including
MVIP and SC-bus compatibility clocks. The local CHI interfaces support PCM rates of 2.048 Mbits/s,
4.096 Mbits/s, and 8.192 Mbits/s. The *Ambassador* T8102 has internal circuitry to support either minimum latency
or multi-time-slot frame integrity. Frame integrity is a requisite feature for applications that switch wideband data
(ISDN H-channels). Minimum latency is advantageous in voice applications.
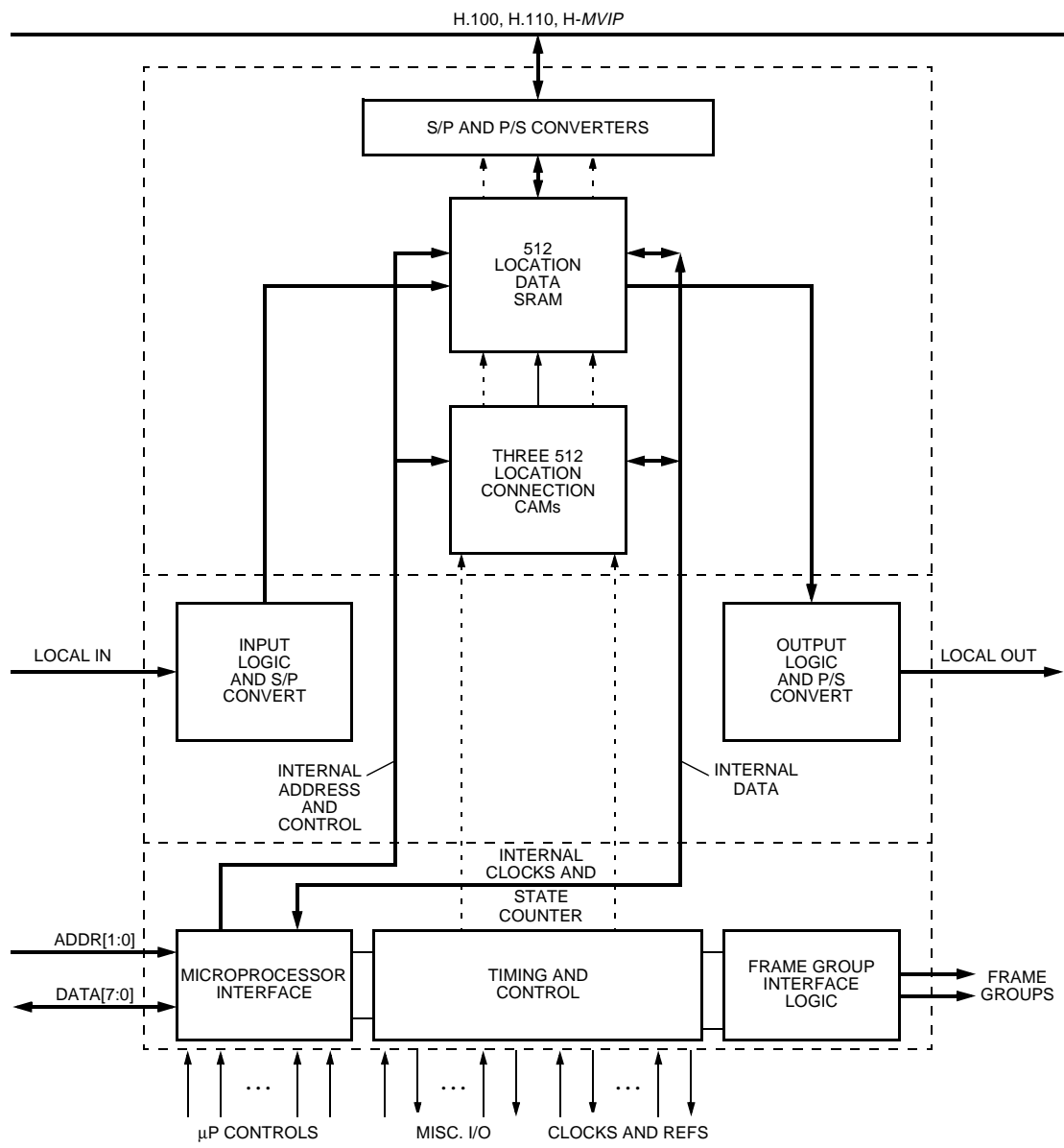
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Figure 1. Block Diagram of the *Ambassador*

Application Overview

The integration of computers and telecommunications has enabled a wide range of new communications applications and has fueled an enormous growth in communications markets. A key element in the development of computer-based communications equipment has been the addition of an auxiliary telecom bus to existing computer systems. Most manufacturers of high-capacity, computer-based telecommunications equipment have incorporated some such telecom bus in their systems. Typically, these buses and bus interfaces are designed to transport and switch Nx64 kbits/s low-latency telecom traffic between boards within the computer, independent of the computer's I/O and memory buses. At least a half dozen of these PC-based telecom buses emerged in the early 1990s for use within equipment based on ISA/EISA and MCA computers.

With the advent of the H.100/H.110 bus specification by the Enterprise Computer Telephony Forum, the computer-telephony industry has agreed on a single telecom bus for use with PCI and compact PCI computers. H.100/H.110 facilitates interoperation of components, thus providing maximum flexibility to equipment manufacturers, value-added resellers, system integrators, and others building computer-based telecommunications applications.

Subrate switching is the ability to switch part(s) of one byte from one stream/time slot to another stream/time slot. The parts are the following:

- Nibbles (4 bits)—representing a 32 kbits/s subrate

- Dibits (2 bits)—representing a 16 kbits/s subrate

- Bits—representing an 8 kbits/s subrate

H.100/H.110 data transfers are always bytes. If subrate switching is used, the T8100A constructs a byte consisting of the subrate samples. The constructed byte may contain any combination of nibbles, dibits, or bits. In addition, individual data bits can be placed within a byte along with don't care bits.
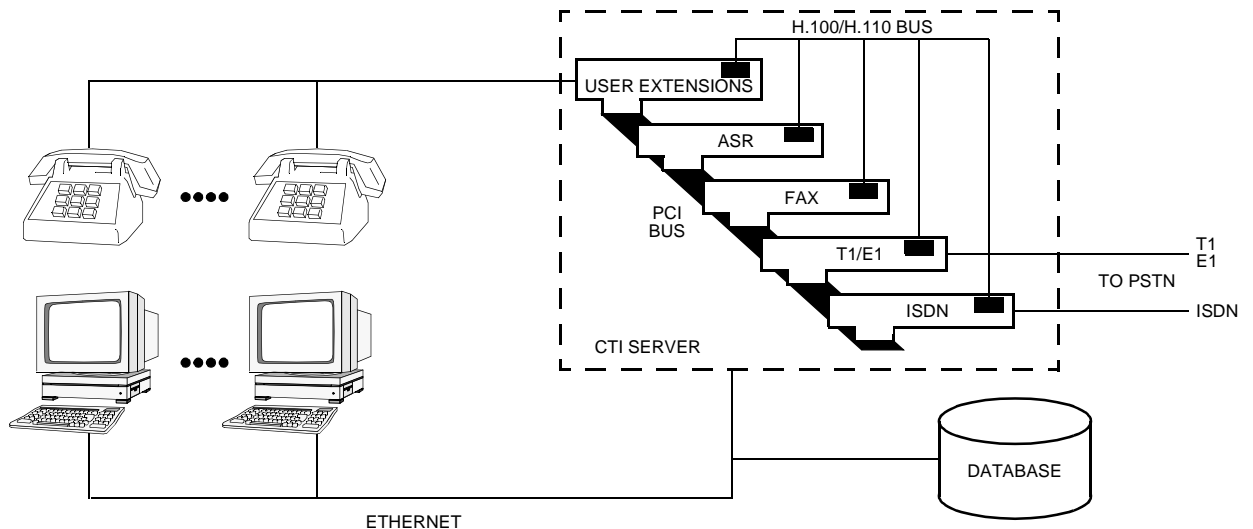

Figure 2. CTI Call Center Application

T8102 Selection Guide

Features	T8100	T8100A	T8102	T8105
Subrate switching	—	√	√	√
Local-to-local connections	1,024	1,024	—	1,024
Local-to-H.100 connections	256	256	512	512
CT_NETREFs	1	2	2	2

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