



T-46-13-27

NMC93C56/NMC93C66

## NMC93C56/C66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Memories

### General Description

The NMC93C56/NMC93C66 are 2048/4096 bits of CMOS electrically erasable memory divided into 128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 5V supply since  $V_{PP}$  is generated on-board. The serial organization allows the NMC93C56/66 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status come out on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The NMC93C56/66 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming capability with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

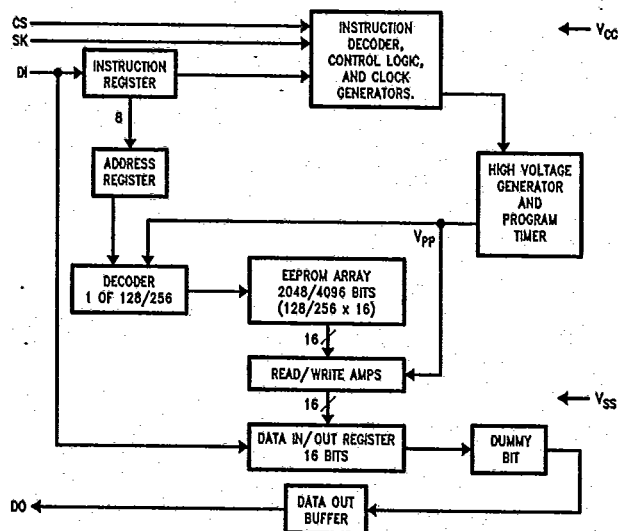
### Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346 and CMOS EEPROMs NMC93C06/46. The NMC93C56/66 are both pin and function compatible with the NMC93C06/46, 256/1024-bit EEPROM with the one exception that the NMC93C56/66 require 2 additional address bits.

### Features

- Typical active current 400  $\mu$ A; Typical standby current 25  $\mu$ A
- Reliable CMOS floating gate technology
- 5V only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 40 years data retention
- Designed for 100,000 write cycles

### Block Diagram



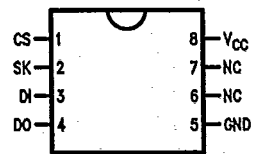
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Connection Diagrams

Dual-In-Line Package (N)



Top View

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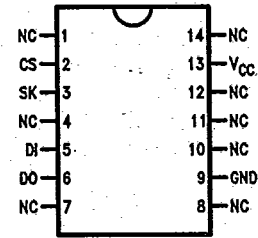
See NS Package Number N08E

Pin Names

|     |                    |
|-----|--------------------|
| CS  | Chip Select        |
| SK  | Serial Data Clock  |
| DI  | Serial Data Input  |
| DO  | Serial Data Output |
| GND | Ground             |
| VCC | Power Supply       |

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SO Package (M)



Top View

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See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

| Order Number        |
|---------------------|
| NMC93C56N/NMC93C66N |
| NMC93C56M/NMC93C66M |

Extended Temp. Range (-40°C to +85°C)

| Order Number          |
|-----------------------|
| NMC93C56EN/NMC93C66EN |
| NMC93C56EM/NMC93C66EM |

Military Temp. Range (-55°C to +125°C)

| Order Number          |
|-----------------------|
| NMC93C56MN/NMC93C66MN |
| NMC93C56MM/NMC93C66MM |

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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

All Input or Output Voltages with Respect to Ground  $+6.5\text{V}$  to  $-0.3\text{V}$

Lead Temp. (Soldering, 10 sec.)  $+300^{\circ}\text{C}$

ESD Rating 2000V

**Operating Conditions**

Ambient Operating Temperature

NMC93C56/NMC93C66  $0^{\circ}\text{C}$  to  $+10^{\circ}\text{C}$

NMC93C56E/NMC93C66E  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

NMC93C56M/NMC93C66M  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

(Mil. Temp.)

Positive Power Supply 4.5V to 5.5V

**DC and AC Electrical Characteristics**  $V_{CC} = 5\text{V} \pm 10\%$  (unless otherwise specified)

| Symbol                 | Parameter                                 | Part Number                                                      | Conditions                                                                       | Min                | Max                 | Units                          |
|------------------------|-------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------------------------|--------------------|---------------------|--------------------------------|
| $I_{CC1}$              | Operating Current<br>CMOS Input Levels    | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M* | CS = $V_{IH}$ , SK = 1 MHz<br>SK = 0.5 MHz<br>SK = 0.5 MHz                       |                    | 2<br>2<br>2         | mA                             |
| $I_{CC2}$              | Operating Current<br>TTL Input Levels     | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | CS = $V_{IH}$ , SK = 1 MHz<br>SK = 0.5 MHz<br>SK = 0.5 MHz                       |                    | 3<br>3<br>4         | mA                             |
| $I_{CC3}$              | Standby Current                           | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | CS = 0V                                                                          |                    | 50<br>100<br>100    | $\mu\text{A}$                  |
| $I_{IL}$               | Input Leakage                             | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | $V_{IN} = 0\text{V}$ to $V_{CC}$                                                 | -2.5<br>-10<br>-10 | 2.5<br>10<br>10     | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{OL}$               | Output Leakage                            | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | $V_{IN} = 0\text{V}$ to $V_{CC}$                                                 | -2.5<br>-10<br>-10 | 2.5<br>10<br>10     | $\mu\text{A}$<br>$\mu\text{A}$ |
| $V_{IL}$<br>$V_{IH}$   | Input Low Voltage<br>Input High Voltage   |                                                                  |                                                                                  | -0.1<br>2          | 0.8<br>$V_{CC} + 1$ | V<br>V                         |
| $V_{OL1}$              | Output Low Voltage                        | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | $I_{OL} = 2.1\text{ mA}$<br>$I_{OL} = 2.1\text{ mA}$<br>$I_{OL} = 1.8\text{ mA}$ |                    | 0.4<br>0.4<br>0.4   | V                              |
| $V_{OH1}$              | Output High Voltage                       |                                                                  | $I_{OH} = 400\text{ }\mu\text{A}$                                                | 2.4                |                     | V                              |
| $V_{OL2}$<br>$V_{OH2}$ | Output Low Voltage<br>Output High Voltage |                                                                  | $I_{OL} = 10\text{ }\mu\text{A}$<br>$I_{OH} = -10\text{ }\mu\text{A}$            | $V_{CC} - 0.2$     | 0.2                 | V<br>V                         |
| $f_{SK}$               | SK Clock Frequency                        | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  |                                                                                  | 0<br>0<br>0        | 1<br>0.5<br>0.5     | MHz                            |
| $t_{SKH}$              | SK High Time                              | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | (Note 2)<br>(Note 3)<br>(Note 3)                                                 | 250<br>500<br>500  |                     | ns                             |
| $t_{SKL}$              | SK Low Time                               | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | (Note 2)<br>(Note 3)<br>(Note 3)                                                 | 250<br>500<br>500  |                     | ns                             |
| $t_{CS}$               | Minimum CS Low Time                       | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | (Note 4)<br>(Note 5)<br>(Note 5)                                                 | 250<br>500<br>500  |                     | ns                             |
| $t_{CSS}$              | CS Setup Time                             | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M  | Relative to SK                                                                   | 50<br>100<br>100   |                     | ns                             |

\*Note: Throughout this table "M" refers to temperature range ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ), not package type.

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**DC and AC Electrical Characteristics**  $V_{CC} = 5V \pm 10\%$  (unless otherwise specified) (Continued)

| Symbol    | Parameter              | Part Number                                                     | Conditions               | Min               | Max                 | Units |
|-----------|------------------------|-----------------------------------------------------------------|--------------------------|-------------------|---------------------|-------|
| $t_{DIS}$ | DI Setup Time          | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | Relative to SK           | 100<br>200<br>200 |                     | ns    |
| $t_{CSH}$ | CS Hold Time           |                                                                 | Relative to SK           | 0                 |                     | ns    |
| $t_{DIH}$ | DI Hold Time           | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | Relative to SK           | 100<br>200<br>200 |                     | ns    |
| $t_{PD1}$ | Output Delay to "1"    | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | AC Test                  |                   | 500<br>1000<br>1000 | ns    |
| $t_{PD0}$ | Output Delay to "0"    | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | AC Test                  |                   | 500<br>1000<br>1000 | ns    |
| $t_{SV}$  | CS to Status Valid     | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | AC Test                  |                   | 500<br>1000<br>1000 | ns    |
| $t_{DF}$  | CS to DO in TRI-STATE® | NMC93C56/NMC93C66<br>NMC93C56E/NMC93C66E<br>NMC93C56M/NMC93C66M | AC Test<br>CS = $V_{IL}$ |                   | 100<br>200<br>200   | ns    |
| $t_{WP}$  | Write Cycle Time       |                                                                 |                          |                   | 10                  | ms    |

**Note 1:** Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1  $\mu s$ , therefore in an SK clock cycle  $t_{SKH} + t_{SKL}$  must be greater than or equal to 1  $\mu s$ . For example if  $t_{SKL} = 250$  ns then the minimum  $t_{SKH} = 750$  ns in order to meet the SK frequency specification.

**Note 3:** The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2  $\mu s$ , therefore in an SK clock cycle  $t_{SKH} + t_{SKL}$  must be greater than or equal to 2  $\mu s$ . For example, if the  $t_{SKL} = 500$  ns then the minimum  $t_{SKH} = 1.5$   $\mu s$  in order to meet the SK frequency specification.

**Note 4:** For Commercial parts CS must be brought low for a minimum of 250 ns ( $t_{CS}$ ) between consecutive instruction cycles.

**Note 5:** For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns ( $t_{CS}$ ) between consecutive instruction cycles.

**Note 6:** This parameter is periodically sampled and not 100% tested.

**Capacitance** (Note 6) $T_A = 25^\circ C$   $f = 1$  MHz

| Symbol    | Test               | Typ | Max | Units |
|-----------|--------------------|-----|-----|-------|
| $C_{OUT}$ | Output Capacitance |     | 5   | pF    |
| $C_{IN}$  | Input Capacitance  |     | 5   | pF    |

**AC Test Conditions**

|                                    |                               |
|------------------------------------|-------------------------------|
| Output Load                        | 1 TTL Gate and $C_L = 100$ pF |
| Input Pulse Levels                 | 0.4V to 2.4V                  |
| Timing Measurement Reference Level |                               |
| Input                              | 1V and 2V                     |
| Output                             | 0.8V and 2V                   |

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NMC93C56/NMC93C66

## Functional Description

The NMC93C56 and NMC93C66 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

### Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

### Erase/Write Enable (EWEN):

When  $V_{CC}$  is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or  $V_{CC}$  is removed from the part.

### Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ( $t_{CS}$ ). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

### Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ( $t_{CS}$ ). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

### Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ( $t_{CS}$ ).

### Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns ( $t_{CS}$ ).

### Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

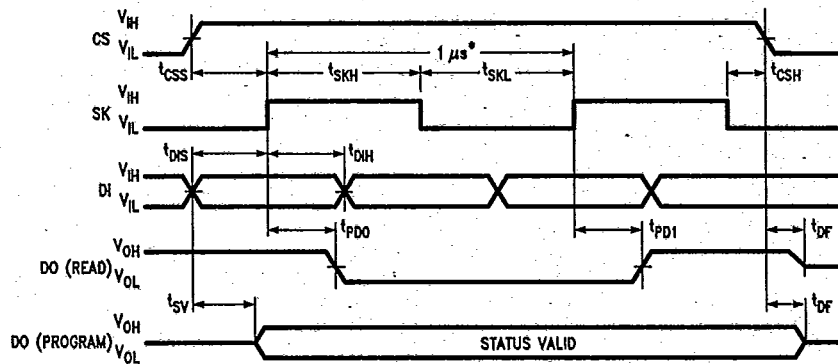
## Instruction Set for the NMC93C56 and NMC93C66

| Instruction | SB | Op Code | Address  | Data   | Comments                                                           |
|-------------|----|---------|----------|--------|--------------------------------------------------------------------|
| READ        | 1  | 10      | A7-A0    |        | Reads data stored in memory.                                       |
| EWEN        | 1  | 00      | 11XXXXXX |        | Write enable must precede all programming modes.                   |
| ERASE       | 1  | 11      | A7-A0    |        | Erase register A7A6A5A4A3A2A1A0.                                   |
| ERAL        | 1  | 00      | 10XXXXXX |        | Erases all registers.                                              |
| WRITE       | 1  | 01      | A7-A0    | D15-D0 | Writes register if address is unprotected.                         |
| WRAL        | 1  | 00      | 01XXXXXX | D15-D0 | Writes all registers. Valid only when Protect Register is cleared. |
| EWDS        | 1  | 00      | 00XXXXXX |        | Disables all programming instructions.                             |

## Timing Diagrams

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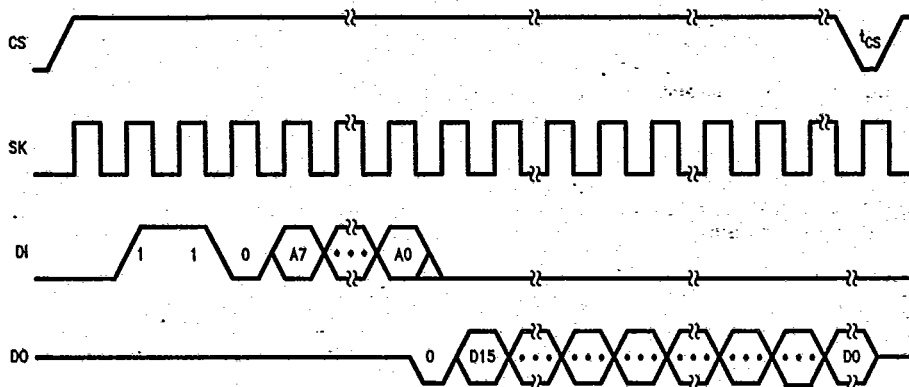
## Synchronous Data Timing



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\*This is the minimum SK period (Note 2).

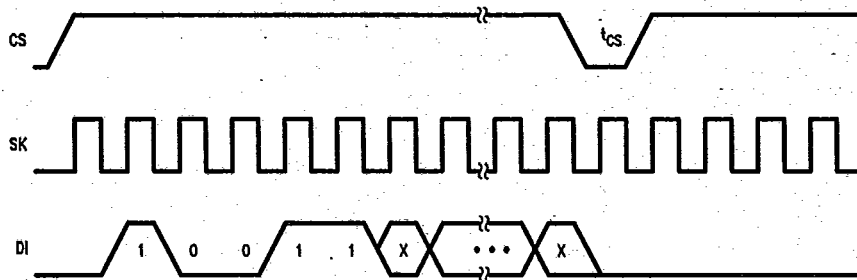
## READ:



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\*Address bit A7 becomes a "don't care" for NMC93C56.

## EWEN:

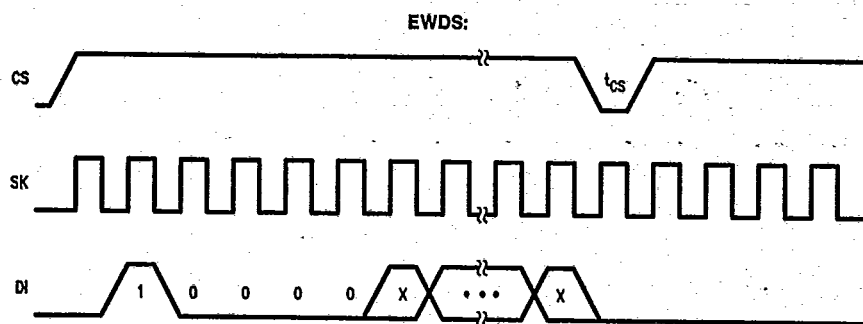


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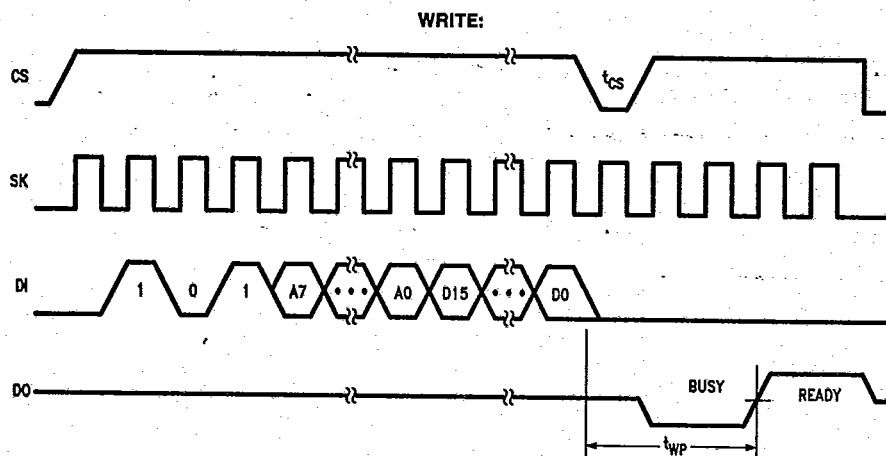
Timing Diagrams (Continued)

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NMC93C56/NMC93C66

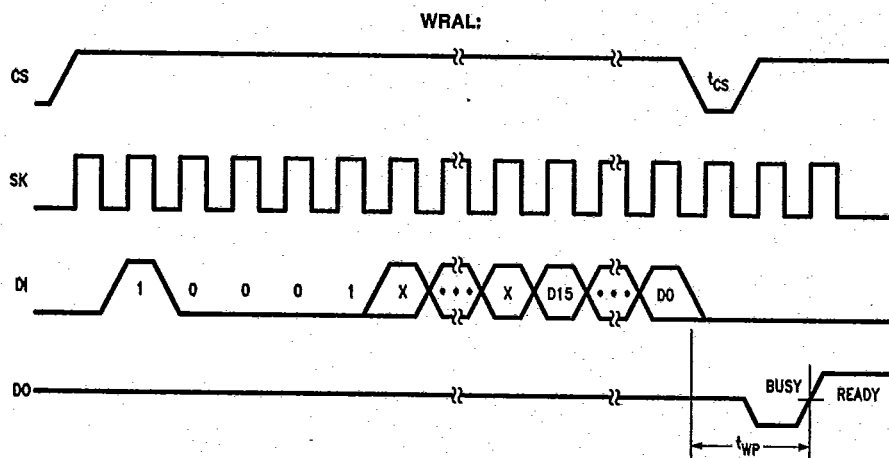


TL/D/9617-7



TL/D/9617-8

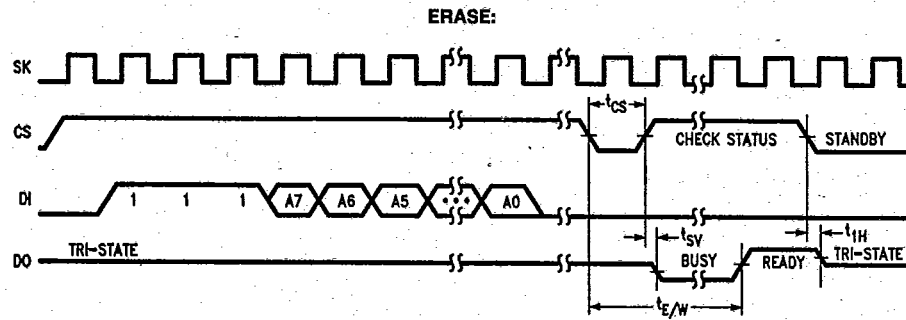
\*Address bit A7 becomes a "don't care" for NMC93C56.



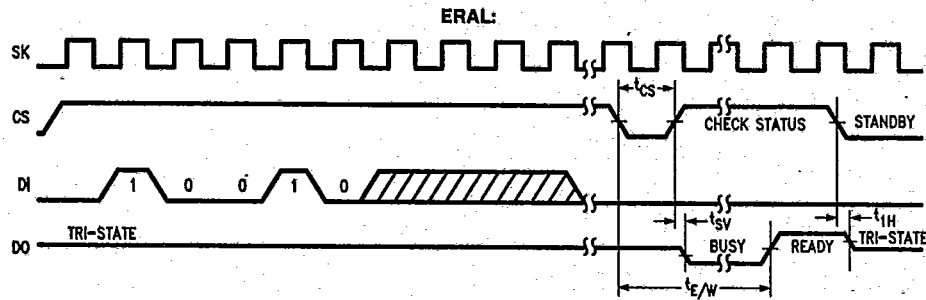
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Timing Diagrams (Continued)

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TL/D/9617-10



TL/D/9617-11