Migrating from LXT325 to LXT336 Quad Receiver

Application Note

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Order Number: 249173-002

As of January 15, 2001, this document replaces the Level One document known as *AN116*.

Application Note

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Revision History

Revision	Date	Description
-002	03/06/01	Modified Figures 2 & 4. Modified LXT336 QFP pin #18 description Tables 1, 3 & 5.

1.0 Introduction

This Application Note provides information to convert an existing LXT325 based design to the LXT336. The LXT325 was the first Intel Quad Receiver for both T1 and E1 applications. The LXT336 is a new quad T1/E1 receiver with some additional features that are not available on the LXT325.

Due to pin-out and functional differences between the LXT325 and LXT336, migration will require redesigning of the PCB

1.1 Major Differences

- The LXT336 offers both bipolar and unipolar mode, the LXT325 works in bipolar mode only.
- The LXT336 offers selectable AMI/HDB3 decoders, the LXT325 offers AMI decoding only.
- Both devices have a pin called MODE. However, the operation of this pin is different for each device. Refer to the data sheets for details.
- Receiver slicer ratio is selectable on the LXT325 (with MODE pin), on the LXT336 slicer ratio is fixed to 50% for E1 and to 70% for T1 applications.
- LOS criteria are different for the LXT336 and the LXT325. The LXT336 LOS complies with the most recent standards; the LXT325 does not.
- Package size is different for each device. The LXT325 comes in 28 pin DIP, 28pin PLCC and 44 pin QFP packages. The LXT336 is only available in a 64-pin QFP package.

1.2 Pin Comparisons

Table 1 provides a complete pin comparison between the LXT325 and the LXT336 to facilitate migration. It lists the signals available on the LXT325 and the corresponding (equivalent) signals on the LXT336. Due to its increased functionality, the LXT336 has more I/O pins than the LXT325.

1.3 Applications

Table 2 through Table 5 list the LXT336 pin configuration for each of its four major applications:

- T1 Receiver mode
- T1 Monitoring mode
- E1 Receiver mode
- E1 Monitoring mode

The LXT336 meets or exceeds the performance of the LXT325 when used in the recommended configurations. Figure 1 through Figure 4 show how to couple the device to the line and other details the designer should be aware of when converting from the LXT325 to the LXT336.

Note: There are significant differences in line coupling transformer requirements and other external components for both receiver and monitoring applications. Refer to the LXT325 and LXT336 data sheets for details.

Table 1. Pinout Cross-Mapping from the LXT325 to the LXT336

LXT325				LXT336		
Pin Number			Pin Name	Pin Number	Pin Name	Description/Comments
DIP	PLCC	QFP		QFP		
1	2	8	RPOS1	63	RPOS0/ RDATA0	Receiver 1, Receive Positive Data Output.
2	3	9	RNEG1	62	RNEG0/BPV0	Receiver 1, Receive Negative Data Output.
3	4	10	RCLK1	64	RCLK0	Receiver 1, Receive Clock Output.
4	5	13	RPOS2	60	RPOS1/ RDATA1	Receiver 2, Receive Positive Data Output.
5	6	14	RNEG2	59	RNEG1/BPV1	Receiver 2, Receive Negative Data Output.
6	7	15	RCLK2	61	RCLK1	Receiver 2, Receive Clock Output.
7	8	16	LOS3	27	LOS2	Receiver 3, Loss of Signal Output.
8	9	19	RPOS3	53	RPOS2/ RDATA2	Receiver 3, Receive Positive Data Output.
9	10	20	RNEG3	52	RNEG2/BPV2	Receiver 3, Receive Negative Data Output.
10	11	21	RCLK3	54	RCLK2	Receiver 3, Receive Clock Output.
11	12	24	RPOS4	50	RPOS3/ RDATA3	Receiver 4, Receive Positive Data Output.
12	13	25	RNEG4	49	RNEG3/BPV3	Receiver 4, Receive Negative Data Output.
13	14	26	RCLK4	51	RCLK3	Receiver 4, Recovered Clock Output.
14	15	27, 28	GND	3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	Ground.
15	16	30	MCLK	1	MCLK	Master Clock Input.
16	17	31	MODE	-	-	Mode Selection Input. This pin on LXT325 selects 50% or 70% slicer ratio. On the LXT336 the slicer ratio is set to 50% for E1 and 70% for T1 operation.
17	18	32	RTIP4	29	RTIP3	Receiver 4, Receive TIP Input.
18	19	35	RRING4	28	RRING3	Receiver 4, Receive RING Input.
19	20	36	LOS4	30	LOS3	Receiver 4, Loss of Signal Output
20	21	37	RTIP3	26	RTIP2	Receiver 3, Receive TIP Input.
21	22	38	RRING3	25	RRING2	Receiver 3, Receive RING Input.

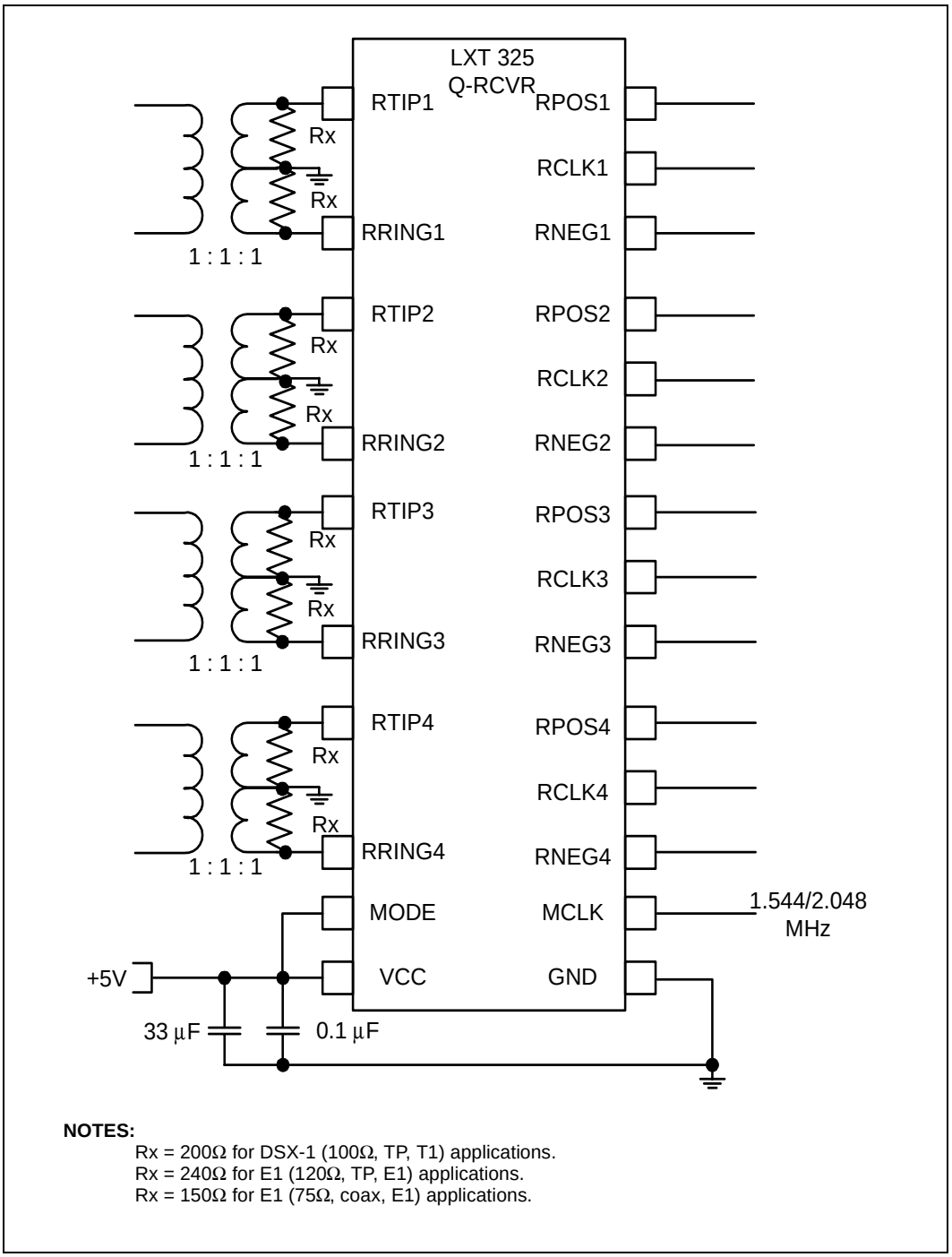
Table 1. Pinout Cross-Mapping from the LXT325 to the LXT336 (Continued)

LXT325				LXT336		
Pin Number			Pin Name	Pin Number	Pin Name	Description/Comments
DIP	PLCC	QFP		QFP		
22	23	40	LOS2	24	LOS1	Receiver 2, Loss of Signal Output.
23	24	41	RTIP2	23	RTIP1	Receiver 2, Receive TIP Input.
24	25	42	RRING2	22	RRING1	Receiver 2, Receive RING Input.
25	26	2	LOS1	21	LOS0	Receiver 1, Loss of Signal Output.
26	27	3	RTIP1	20	RTIP0	Receiver 1, Receive TIP Input.
27	28	4	RRING1	19	RRING0	Receiver 1, Receive RING Input.
28	1	5, 6	VCC	11, 15, 34, 38, 41	VCC	Positive (+5V) supply.
-	-	-	-	18	MODE	Mode Select Input. Refer to the LXT336 data sheet for details. Tie this pin to GND for E1 AMI operation, High for E1 - HDB3 operation or connect it to 2.5V for T1 operation.
-	-	-	-	4 7 42 45	UBS0 UBS1 UBS2 UBS3	Receiver 1, 2, 3, and 4 - Unipolar-Bipolar Select Input. These Inputs are available only on the LXT336. Connect to GND.
-	-	-	-	32	CLKE	Clock Edge Select Input. Tie pin to VCC through a 10 kΩ resistor.
-	-	-	-	2 5 44 47	CLKI0 CLKI1 CLKI2 CLKI3	CLOCK Input Receiver1, 2, 3, and 4. Connected to GND when migrating from LXT325 to LXT336.
-	-	1, 7, 11, 12,17, 18, 22, 23, 29, 33, 34, 39, 43, 44	NC-not connected	9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC-not connected	All NC pins must be left open (not connected).

1.3.1 Migrating to LXT336 Receiver Mode of Operation

Figure 1 and Figure 2 show the LXT325 and the LXT336 configured for receiver mode of operation. Note the differences between the LXT325 and the LXT336. The following signals are significant: MODE, CLKI, UBS and CLKE. Table 2 specifies the pin-out to configure the LXT336 for T1 receiver mode. Table 4 specifies the pin-out to configure the LXT336 for E1 receiver mode.

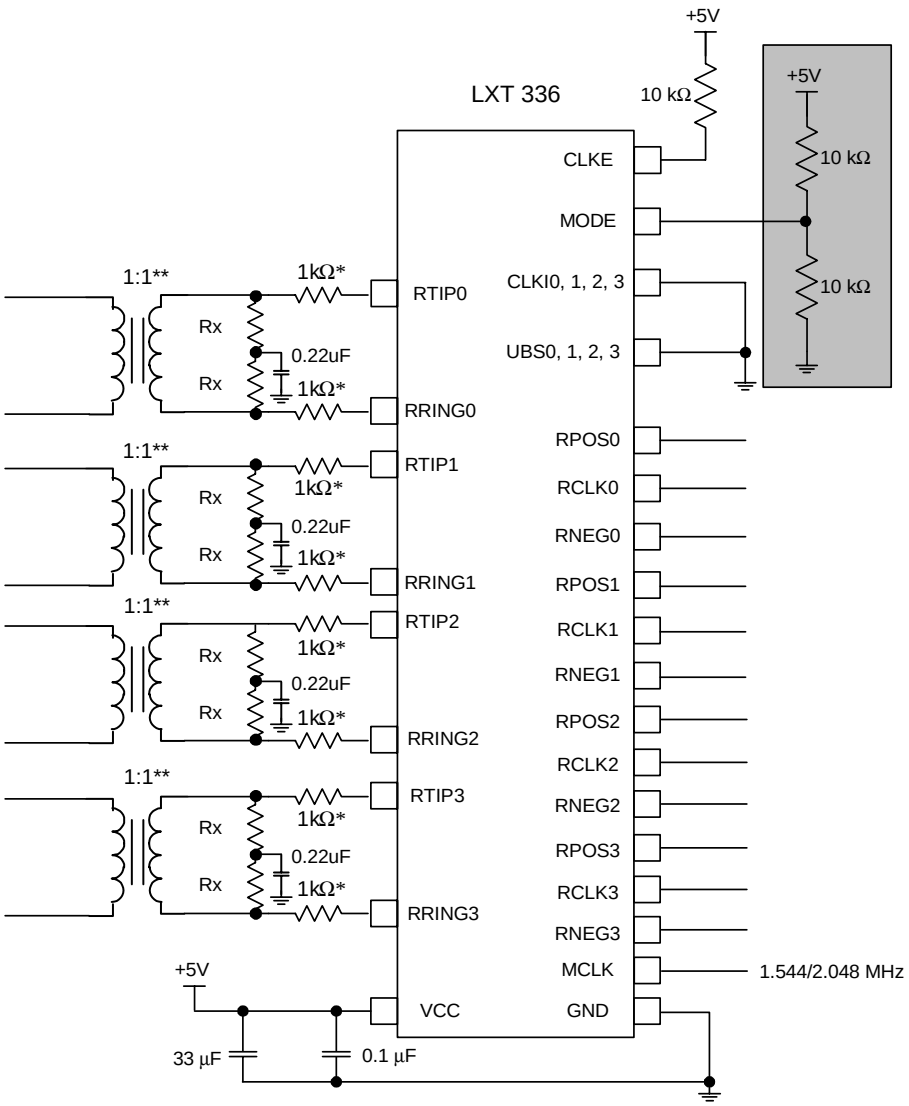
Figure 1. LXT325 Receiver Mode Applications



NOTES:

Rx = 200Ω for DSX-1 (100Ω, TP, T1) applications.
Rx = 240Ω for E1 (120Ω, TP, E1) applications.
Rx = 150Ω for E1 (75Ω, coax, E1) applications.

Figure 2. LXT336 Receiver Mode Applications



NOTES:

Rx = 50Ω ± 1% for T1 (100Ω, TP cable) applications.
Rx = 60Ω ± 1% for E1 (120Ω, TP cable) applications.
Rx = 37.5Ω ± 1% for E1 (75Ω, coax cable) applications.

* The 1 kΩ resistors on RTIP and RRING are optional and provide surge protection for the LXT336. The recommended value is between 100Ω and 1000Ω.

** Each 1:1 line transformer shown above may be substituted with the 1:1:1 transformer used on the LXT325 design. This is accomplished by using one-half of the 1:1:1 transformer's secondary winding.

Table 2. LXT336 Configuration in T1 Receiver Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 1.544 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to ground.
3, 6, 8,10, 14,17, 31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11, 15, 34, 38, 41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect this input to 2.5V signal. See Figure 2.
19 20 22 23 25 26 28 29	RRING0 RTIP0 RRING1 RTIP1 RRING2 RTIP2 RRING3 RTIP3	AI AI AI AI AI AI AI AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).
21 24 27 30	LOS0 LOS1 LOS2 LOS3	DO DO DO DO	Loss of Signal Port 0. Loss of Signal Port 1. Loss of Signal Port 2. Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63 62	RPOS0 RNEG0	DO DO	Receive Positive Data Port 0 (Port 1 per LXT325). Receive Negative Data Port 0 (Port 1 per LXT325).
60 59	RPOS1 RNEG1	DO DO	Receive Positive Data Port 1 (Port 2 per LXT325). Receive Negative Data Port 1 (Port 2 per LXT325).
53 52	RPOS2 RNEG2	DO DO	Receive Positive Data Port 2 (Port 3 per LXT325). Receive Negative Data Port 2 (Port 3 per LXT325).
50 49	RPOS3 RNEG3	DO DO	Receive Positive Data Port 3 (Port 4 per LXT325). Receive Negative Data Port 3 (Port 4 per LXT325).
64 61 54 51	RCLK0 RCLK1 RCLK2 RCLK3	DO DO DO DO	Receive Clock Output Port 0 (Port 1 on LXT325). Receive Clock Output Port 1 (Port 2 on LXT325). Receive Clock Output Port 2 (Port 3 on LXT325). Receive Clock Output Port 3 (Port 4 on LXT325).

Table 3. LXT336 Configuration in E1 Receiver Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 2.048 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11, 15, 34, 38, 41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect to Vcc or Gnd. See Figure 2.
19 20 22 23 25 26 28 29	RRING0 RTIP0 RRING1 RTIP1 RRING2 RTIP2 RRING3 RTIP3	AI AI AI AI AI AI AI AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).
21 24 27 30	LOS0 LOS1 LOS2 LOS3	DO DO DO DO	Loss of Signal Port 0. Loss of Signal Port 1. Loss of Signal Port 2. Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63 62	RPOS0 RNEG0	DO DO	Receive Positive Data Port 0 (Port 1 per LXT325). Receive Negative Data Port 0 (Port 1 per LXT325).
60 59	RPOS1 RNEG1	DO DO	Receive Positive Data Port 1 (Port 2 per LXT325). Receive Negative Data Port 1 (Port 2 per LXT325).
53 52	RPOS2 RNEG2	DO Do	Receive Positive Data Port 2 (Port 3 per LXT325). Receive Negative Data Port 2 (Port 3 per LXT325).
50 49	RPOS3 RNEG3	DO DO	Receive Positive Data Port 3 (Port 4 per LXT325). Receive Negative Data Port 3 (Port 4 per LXT325).
64 61 54 51	RCLK0 RCLK1 RCLK2 RCLK3	DO DO DO DO	Receive Clock Output Port 0 (Port 1 on LXT325). Receive Clock Output Port 1 (Port 2 on LXT325). Receive Clock Output Port 2 (Port 3 on LXT325). Receive Clock Output Port 3 (Port 4 on LXT325).

1.3.2 LXT336 Monitoring Mode of Operation

Figure 3 and Figure 4 show the LXT325 and the LXT336 configured for monitor mode of operation. Note the differences between the LXT325 and the LXT336. The following signals are significant: MODE, CLKI, UBS and CLKE. Table 4 specifies the pin-out to configure the LXT336 for T1 monitor mode. Table 5 specifies the pin-out to configure the LXT336 for E1 monitor mode.

Figure 3. LXT325 Monitor Application

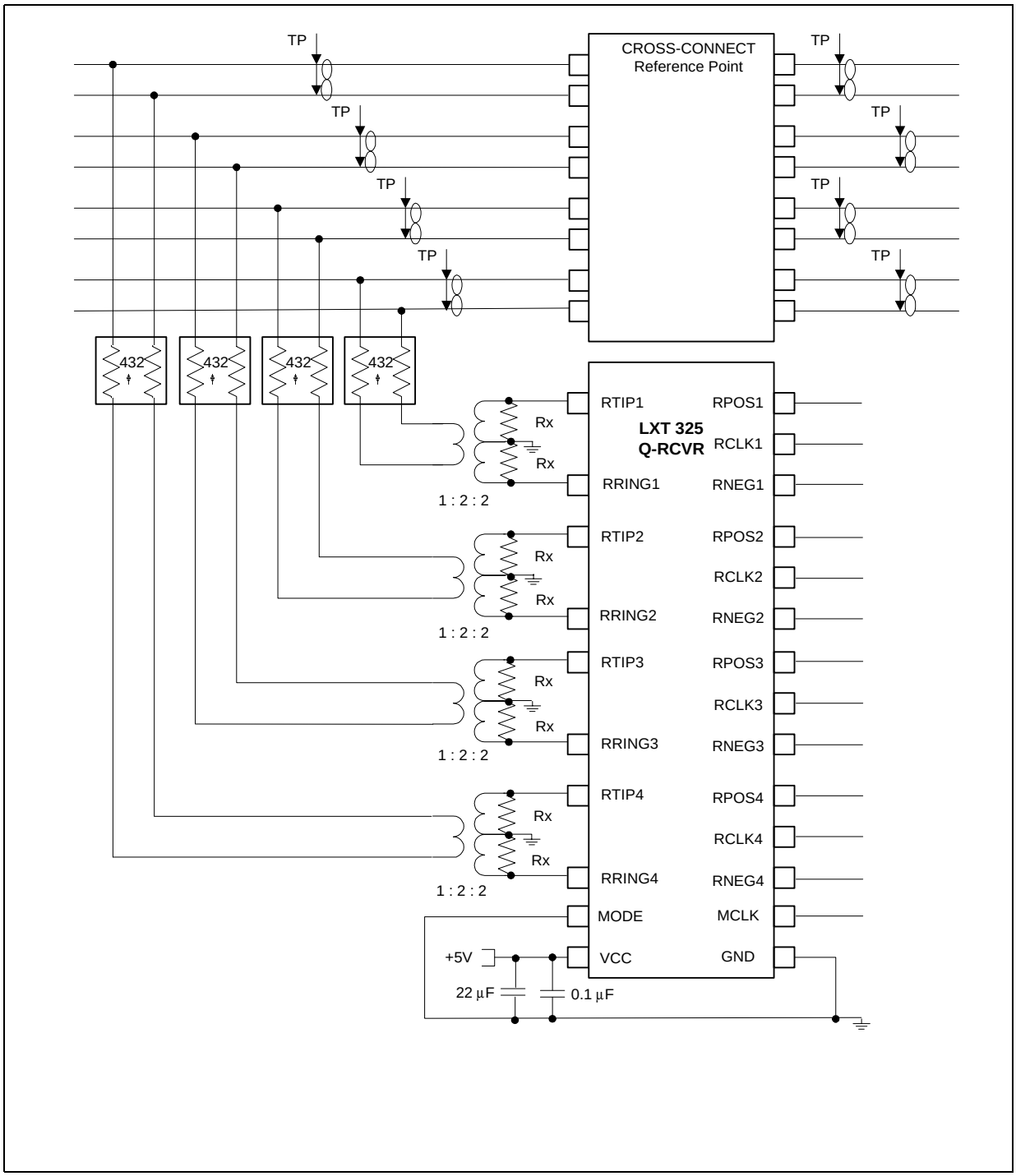
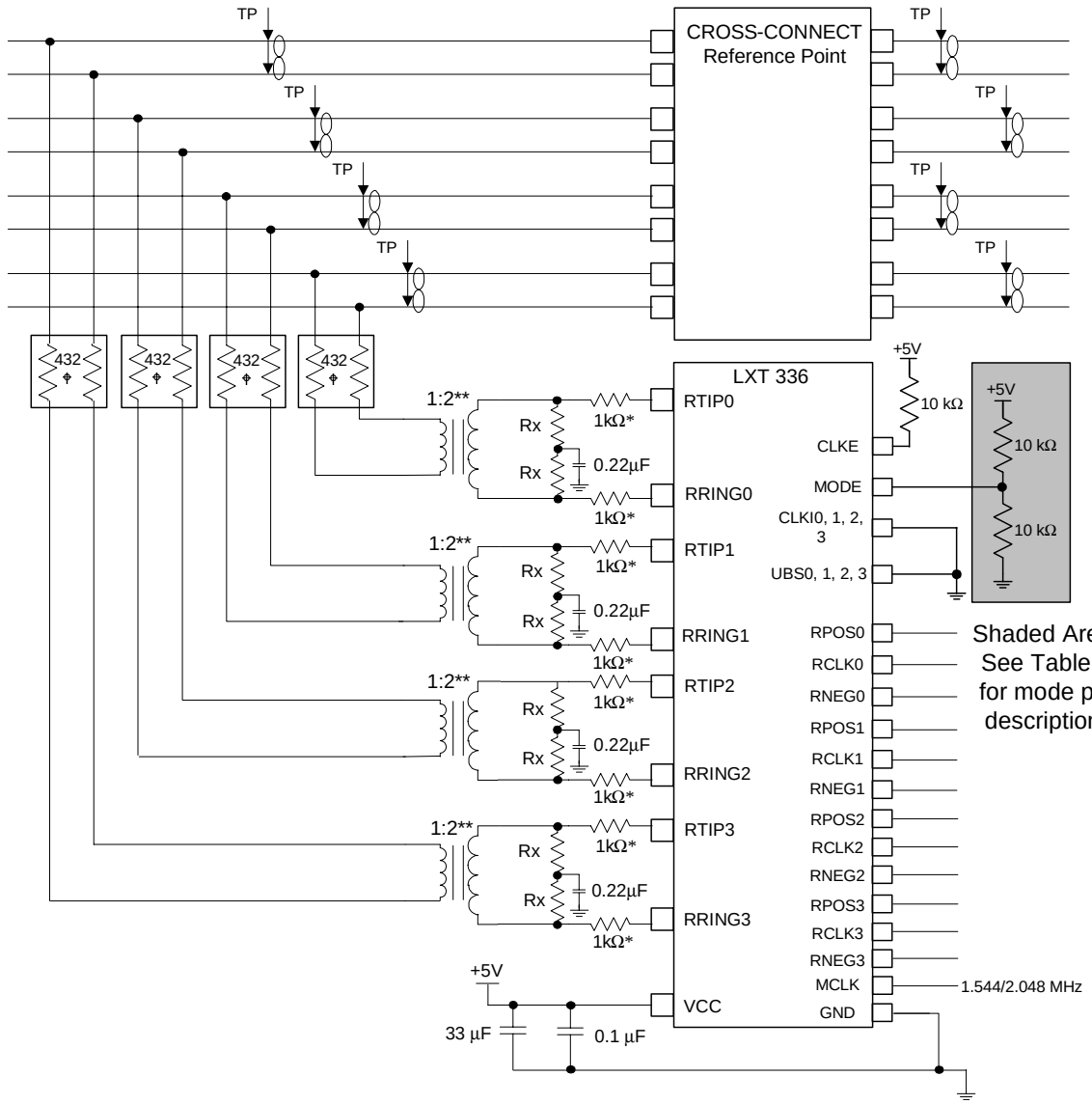


Figure 4. LXT336 Monitor Application



NOTES:

Rx = 200Ω ± 1% for T1 (100Ω, TP cable) applications.
Rx = 240Ω ± 1% for E1 (120Ω, TP cable) applications.
Rx = 150Ω ± 1% for E1 (75Ω, coax cable) applications.

* The 1 kΩ resistors on RTIP and RRING are optional and provide surge protection for the LXT336. The recommended value is between 100Ω and 1000Ω.

** Each 1:2 line transformer shown above may be substituted with the 1:2:2 transformer used on the LXT325 design. This i accomplished by using one-half of the 1:2:2 transformer's secondary winding.

Table 4. LXT336 Configuration In T1 Monitoring Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 1.544 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17,31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11,15,34, 38,41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect this input to 2.5V. See Figure 4.
19	RRING0	AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2, 3, and 4 per LXT325).
20	RTIP0	AI	
22	RRING1	AI	
23	RTIP1	AI	
25	RRING2	AI	
26	RTIP2	AI	
28	RRING3	AI	
29	RTIP3	AI	
21	LOS0	DO	Loss of Signal Port 0.
24	LOS1	DO	Loss of Signal Port 1.
27	LOS2	DO	Loss of Signal Port 2.
30	LOS3	DO	Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63	RPOS0	DO	Receive Positive Data Port 0 (Port 1 per LXT325).
62	RNEG0	DO	Receive Negative Data Port 0 (Port 1 per LXT325).
60	RPOS1	DO	Receive Positive Data Port 1 (Port 2 per LXT325).
59	RNEG1	DO	Receive Negative Data Port 1 (Port 2 per LXT325).
53	RPOS2	DO	Receive Positive Data Port 2 (Port 3 per LXT325).
52	RNEG2	DO	Receive Negative Data Port 2 (Port 3 per LXT325).
50	RPOS3	DO	Receive Positive Data Port 3 (Port 4 per LXT325).
49	RNEG3	DO	Receive Negative Data Port 3 (Port 4 per LXT325).
64	RCLK0	DO	Receive Clock Output Port 0 (Port 1 on LXT325).
61	RCLK1	DO	Receive Clock Output Port 1 (Port 2 on LXT325).
54	RCLK2	DO	Receive Clock Output Port 2 (Port 3 on LXT325).
51	RCLK3	DO	Receive Clock Output Port 3 (Port 4 on LXT325).

Table 5. LXT336 Configuration in E1 Monitoring Mode of Operation

Pin#	Symbol	I/O	Description
1	MCLK	DI	Master Clock. Supply 2.048 MHz clock.
2, 5, 44, 47	CLKI0, 1, 2, 3	DI	Connect to Ground.
3, 6, 8, 10, 14, 17, 31, 35, 39, 43, 46	GND	S	Connect to power supply Ground.
4, 7, 42, 45	UBS0, 1, 2, 3	DI	Connect to Ground.
9, 12, 13, 16, 33, 36, 37, 40, 48, 55, 56, 57, 58	NC	-	Not Connected.
11, 15, 34, 38, 41,	VCC	S	+5V power supply.
18	MODE	DI	Mode Select Input. Connect this input to Vcc or Gnd. See Figure 4.
19 20 22 23 25 26 28 29	RRING0 RTIP0 RRING1 RTIP1 RRING2 RTIP2 RRING3 RTIP3	AI AI AI AI AI AI AI AI	Receive Ring/Tip Inputs for Port 0, 1, 2, and 3 (Port 1, 2,3, and 4 per LXT325).
21 24 27 30	LOS0 LOS1 LOS2 LOS3	DO DO DO DO	Loss of Signal Port 0. Loss of Signal Port 1. Loss of Signal Port 2. Loss of Signal Port 3.
32	CLKE	DI	Clock Edge Select Input. Pull this pin High using a 10k Ω resistor.
63 62	RPOS0 RNEG0	DO DO	Receive Positive Data Port 0 (Port 1 per LXT325). Receive Negative Data Port 0 (Port 1 per LXT325).
60 59	RPOS1 RNEG1	DO DO	Receive Positive Data Port 1 (Port 2 per LXT325). Receive Negative Data Port 1 (Port 2 per LXT325).
53 52	RPOS2 RNEG2	DO DO	Receive Positive Data Port 2 (Port 3 per LXT325). Receive Negative Data Port 2 (Port 3 per LXT325).
50 49	RPOS3 RNEG3	DO DO	Receive Positive Data Port 3 (Port 4 per LXT325). Receive Negative Data Port 3 (Port 4 per LXT325).
64 61 54 51	RCLK0 RCLK1 RCLK2 RCLK3	DO DO DO DO	Receive Clock Output Port 0 (Port 1 on LXT325). Receive Clock Output Port 1 (Port 2 on LXT325). Receive Clock Output Port 2 (Port 3 on LXT325). Receive Clock Output Port 3 (Port 4 on LXT325).