Features

- TTL logic level inputs for 3.3V logic interfaces
- Smart logic for power up / hot plug state control
- Monolithic IC reliability
- Low matched R_{ON}
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting and thermal shutdown for SLIC protection
- +12.5V operation with power consumption ≤25mW
- Latched logic level inputs, no external drive circuitry required
- Small 16-pin SOIC

Applications

- Fiber to the Home (FTTH)
- Fiber in the Loop (FITL)
- VoIP Gateways
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)

Description

The CPC7508 is a member of Clare's next generation Line Card Access Switch family. When used with ringing SLICs it provides the necessary functions to replace the two 2-Form-C electromechanical test relays used in contemporary Fiber To The Home (FTTH) and Optical Network Unit (ONU) deployments as well as Voice over IP (VoIP) telephony terminals.

Solid state switches provide the mechanism for tip and ring line break, drop test, and channel test while requiring only a single +12V supply for operation. Interface compatibility with 3.3V or 5V logic for switch state control is provided by the TTL logic level inputs.
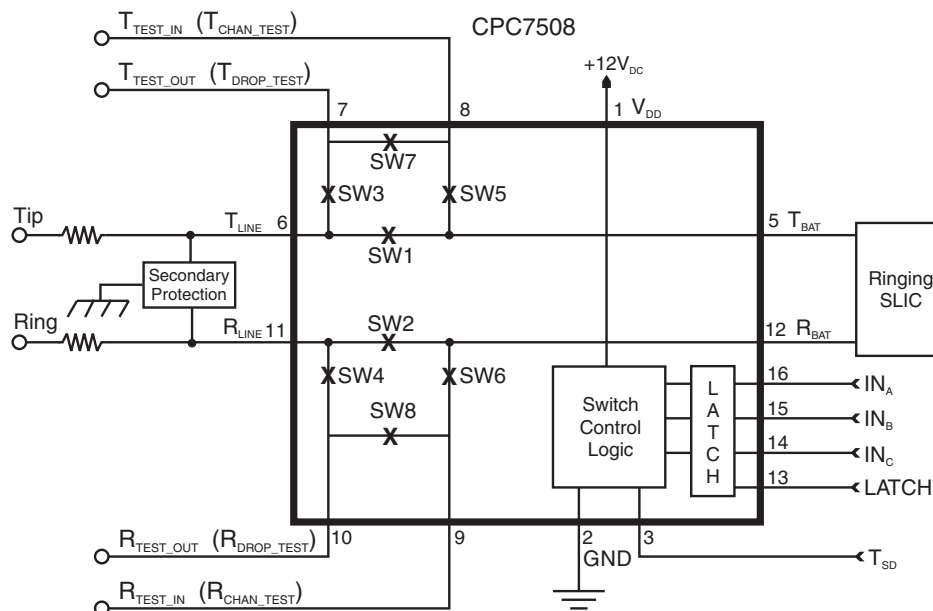
The CPC7508 is designed for fiber access units where EMR's are used for test access and line monitoring functions but solid-state switches are desired due to reduced operating noise, lower power consumption and longer lifetimes.

This monolithic 8-pole solid-state switch is available in a 16-pin SOIC package.

Ordering Information

Part Number	Description
CPC7508B	8-pole LCAS, 16-pin SOIC in tubes (50/tube)
CPC7508BTR	8-pole LCAS, 16-pin SOIC in reels (1000/reel)

Figure 1. CPC7508 Block Diagram

1. Specifications

1.1 Package Pinout

CPC7508

V_{DD}	1	16	IN_A
GND	2	15	IN_B
T_{SD}	3	14	IN_C
N/C	4	13	LATCH
T_{BAT}	5	12	R_{BAT}
T_{LINE}	6	11	R_{LINE}
T_{TEST_OUT}	7	10	R_{TEST_OUT}
T_{TEST_IN}	8	9	R_{TEST_IN}

1.2 Pin Description

Pin	Name	Description
1	V_{DD}	+12.5V_{DC} supply
2	GND	Ground
3	T_{SD}	I/O, All Off control, Thermal shutdown flag
4	N/C	No Connect - Do not use
5	T_{BAT}	Tip lead to the SLIC
6	T_{LINE}	Tip lead of the line side
7	T_{TEST_OUT}	Tip lead of the Test Out (Drop Test) bus
8	T_{TEST_IN}	Tip lead of the Test In (Channel Test) bus
9	R_{TEST_IN}	Ring lead of the Test In (Channel Test) bus
10	R_{TEST_OUT}	Ring lead of the Test Out (Drop Test) bus
11	R_{LINE}	Ring lead of the line side
12	R_{BAT}	Ring lead to the SLIC
13	LATCH	Input, Data latch enable
14	IN_C	Input, Logic control
15	IN_B	Input, Logic control
16	IN_A	Input, Logic control

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+12 V power supply (V_{DD})	-0.3	15	V
Logic input voltage	-0.3	6	V
Logic input to switch output isolation	-	225	V
Switch open-contact to ground isolation	-	225	V
Switch open, contact to contact isolation	-	320	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)
1000 V

1.5 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements.

Typical values are characteristic of the device at 25° C and are the result of engineering evaluations. They are provided for information purposes only and are not part of the testing requirements.

Specifications cover the operating temperature range T_A = -40° C to +85° C. Also, unless otherwise specified all testing is performed with V_{DD} = 12.5 V_{dc}, logic low input voltage is 0 V_{dc} and logic high voltage is 3.3 V_{dc}.

1.6 Switch Specifications

1.6.1 Break Switches, SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{LINE} to T_{BAT} V_{SW2} (differential) = R_{LINE} to R_{BAT} Applied voltage maximum ±225 V to ground All-Off state.					
	+25° C, V_{SW} (differential) = ±320 V	I_{SW}	-	0.1	1	μA
	+85° C, V_{SW} (differential) = ±330 V			0.3		
	-40° C, V_{SW} (differential) = ±310 V			0.1		
On Resistance	I_{SW}(on) = ±10 mA, ±40 mA					
	+25° C	R_{ON}		14.7	-	Ω
	+85° C			21.1	28	
	-40° C		8	10.7	-	
On Resistance Matching	Per SW1 & SW2 On Resistance test conditions.	ΔR_{ON}	-	0.15	0.8	Ω
DC current limit	V_{SW} (on) = ±10 V, +25° C	I_{SW}	-	300	-	mA
	V_{SW} (on) = ±10 V, +85° C		80	160		
	V_{SW} (on) = ±10 V, -40° C		-	400	425	
Dynamic current limit ($t \leq 0.5$ μs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 μs pulse with appropriate protection in place.	I_{SW}	-	1.0	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±225 V V_{SW} (T_{BAT}, R_{BAT}) = ±225 V	I_{SW}	-	0.1	1	μA
	+85° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±225 V V_{SW} (T_{BAT}, R_{BAT}) = ±225 V		-	0.3		
	-40° C, Logic inputs = gnd, V_{SW} (T_{LINE}, R_{LINE}) = ±225 V V_{SW} (T_{BAT}, R_{BAT}) = ±225 V		-	0.1		
dv/dt sensitivity	-	-	-	500	-	V/μs

1.6.2   TEST_OUT Switches SW3 & SW4 and TEST BRIDGE Switches SW7 & SW8

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW3} (differential) = T_{LINE} to T_{TEST_OUT} V_{SW4} (differential) = R_{LINE} to R_{TEST_OUT} V_{SW7} (differential) = T_{TEST_OUT} to T_{TEST_IN} V_{SW8} (differential) = R_{TEST_OUT} to R_{TEST_IN} Applied voltage maximum ±225 V to ground All-Off state.					
	+25° C, V_{SW} (differential) = ±320 V	I_{SW}	-	0.1	1	µA
	+85° C, V_{SW} (differential) = ±330 V			0.3		
	-40° C, V_{SW} (differential) = ±310 V			0.1		
On Resistance	I_{SW}(on) = ±0 mA, ±10 mA,	R_{ON}				Ω
	+25° C			60	-	
	+85° C			85	110	
	-40° C		30	50	-	
On Resistance Matching	Per On Resistance test conditions.	ΔR_{ON}	-	0.5	2	Ω
	SW3 & SW4					
	SW7 & SW8					
DC current limit	V_{SW} (on) = ± 10 V, +25° C	I_{SW}	-	135	-	mA
	V_{SW} (on) = ± 10 V, +85° C		70	85		
	V_{SW} (on) = ± 10 V, -40° C		-	210	250	
Dynamic current limit (t ≤ 0.5 µs)	Test_OUT switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	0.7	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW3} (T_{TEST_OUT}) = ±225 V V_{SW4} (R_{TEST_OUT}) = ±225 V	I_{SW}	-	0.1	1	µA
	+85° C, Logic inputs = gnd, V_{SW3} (T_{TEST_OUT}) = ±225 V V_{SW4} (R_{TEST_OUT}) = ±225 V			0.3		
	-40° C, Logic inputs = gnd, V_{SW3} (T_{TEST_OUT}) = ±225 V V_{SW4} (R_{TEST_OUT}) = ±225 V			0.1		
dv/dt sensitivity	-	-	-	500	-	V/µs

1.6.3   TEST_IN Switches, SW5 and SW6

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW5} (differential) = T_{TEST_IN} to T_{BAT} V_{SW6} (differential) = R_{TEST_IN} to R_{BAT} Applied voltage maximum ±225 V to ground All-Off state.					
	+25° C, V_{SW} (differential) = ±320 V	I_{SW}	-	0.1	1	μA
	+85° C, V_{SW} (differential) = ±330 V			0.2		
	-40° C, V_{SW} (differential) = ±310 V			0.1		
On Resistance	I_{SW}(on) = ±10 mA, ±40 mA					
	+25° C	R_{ON}		38	-	Ω
	+85° C			46	70	
	-40° C		20	28	-	
On Resistance Matching	Per SW5 & SW6 On Resistance test conditions.	ΔR_{ON}	-	0.35	1.4	Ω
DC current limit	V_{SW} (on) = ±10 V, +25° C	I_{SW}	-	125	-	mA
	V_{SW} (on) = ±10 V, +85° C		80	95		
	V_{SW} (on) = ±10 V, -40° C		-	165	250	
Dynamic current limit (t ≤ 0.5 μs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 μs pulse with appropriate protection in place.	I_{SW}	-	1	-	A
Logic input to switch output isolation	+25° C, Logic inputs = gnd, V_{SW5} (T_{TEST_IN}) = ±225 V V_{SW6} (R_{TEST_IN}) = ±225 V	I_{SW}	-	0.1	1	μA
	+85° C, Logic inputs = gnd, V_{SW5} (T_{TEST_IN}) = ±225 V V_{SW6} (R_{TEST_IN}) = ±225 V		-	0.3		
	-40° C, Logic inputs = gnd, V_{SW5} (T_{TEST_IN}) = ±225 V V_{SW6} (R_{TEST_IN}) = ±225 V		-	0.1		
dv/dt sensitivity	-	-	-	500	-	V/μs

1.7 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input voltage, Logic low	Input voltage falling	V_{IL}	0.8	1.0	-	V
Input voltage, Logic high	Input voltage rising	V_{IH}	-	1.7	2.0	
Input leakage current, Logic high	V_{DD} = 13.4 V, V_{HI} = 2.4 V	I_{IH}	-	0.1	1	μA
Input leakage current, Logic low	V_{DD} = 13.4 V, V_{IL} = 0.4 V	I_{IL}	-	0.1	1	μA
Output Characteristics						
Output voltage, T_{SD} Logic low	V_{DD} = 13.4 V, I_{TSD} = 1mA	V_{TSD_on}	-	0	0.4	V

1.8 Voltage and Power Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
V_{DD}	-	V_{DD}	11.4	12.5	13.4	V
Power Specifications						
V_{DD} current	V_{DD} = 12.5 V, All states	I_{DD}	-	1.67	2	mA
Power consumption	V_{DD} = 12.5 V, All states, Measure I_{DD}	P	-	20	25	mW

1.9 Protection Circuitry Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Thermal Shutdown Specifications						
Shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits.	T_{TSD_on}	110	125	150	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C

1.10 Truth Table

State	IN_A	IN_B	IN_C	LATCH	T_{SD}	Break Switches	TEST_OUT Switches	TEST BRIDGE Switches	TEST_IN Switches
Talk	0	0	0			On	Off	Off	Off
TEST_IN	0	0	1			Off	Off	Off	On
TEST_OUT	0	1	0			Off	On	Off	Off
TEST_IN Monitor	0	1	1	0	Z^1	On	Off	Off	On
TEST_OUT Monitor	1	0	0			On	On	Off	Off
TEST_IN & OUT	1	0	1			Off	On	Off	On
All-Off	1	1	0			Off	Off	Off	Off
TEST_IN Bridge	1	1	1			Off	Off	On	On
Latched	X	X	X	1		Unchanged			
All-Off	X	X	X	X	0	Off	Off	Off	Off

[1] Z = High Impedance. Because T_{SD} has a high impedance output for a logic high it needs to be pulled up to the logic supply through an external resistor.

Break Switches: SW1 and SW2
TEST_OUT Switches: SW3 and SW4
TEST_IN Switches: SW5 and SW6
TEST BRIDGE Switches: SW7 and SW8

2. Functional Description

2.1 Introduction

The CPC7508 LCAS provides the necessary test access functions for line card interfaces supported by ringing SLICs in contemporary Fiber In The Loop (FITL), Fiber To The Home (FTTH) applications and Voice over Internet Protocol (VoIP).

These applications have a different working environment than standard traditional Digital Loop Carrier (DLC) equipment and therefore have unique requirements. Two significant differences are the diverse supply voltages and the interface to ringing SLICs.

The once common 5V supply is generally not available in the modern short loop products made feasible with the advent of broadband services. To support applications where a 5V supply is not available but a 12V supply is, the V_{DD} input power specification for the CPC7508 has been set accordingly.

Ringing SLICs have replaced the customary standard SLIC and ringing relay configuration and for the LCAS to be compatible with a ringing SLIC. the LCAS internal protection circuits have been removed. This was essential so as not to clip the ringing waveform output from the ringing SLIC.

Traditional test access is provided by two pair of test access switches, TEST_IN and TEST_OUT, employing the TEST_IN & OUT state. Supplementing the traditional test access switches is the TEST BRIDGE switch pair capable of cross connecting the test busses thereby providing the means to validate the status of SW1 and SW2, the Break Switches.

2.2 Description

2.2.1 Overview

Because the CPC7508 LCAS utilizes solid-state switch construction to implement the switching functions this means no impulse noise is generated when switching large line potentials. To ensure proper voice performance the linear break switches SW1 and SW2 have exceptionally low R_{ON} and excellent matching characteristics. The switches have a

minimum open contact breakdown voltage of 320 V and a minimum contact to ground breakdown voltage of 225 V at +25°C, sufficiently high with proper protection to prevent breakdown in the presence of a transient fault condition.

Integrated into the CPC7508 is a dynamic active current limit, a DC current limit and a thermal shutdown mechanism to provide protection for the SLIC during a fault condition. Positive and negative lightning surge currents are reduced by the dynamic current limiting circuitry and excess power-cross potentials are restricted by the DC current limit and thermal shutdown circuits.

To protect the CPC7508 from an over-voltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at it's tip and ring line terminals to a level below the maximum breakdown voltage of the switches. With proper selection of the secondary protector, a line interface circuit using the CPC7508 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7508 operates from a single +12.5 V supply giving the device extremely low power consumption in any state.

State control is via TTL logic-level compatible inputs so no additional driver circuitry or level translators are required. TTL compatible inputs make state control of the CPC7508 with low voltage logic devices possible.

2.2.2 Logic States

The CPC7508 provides eight distinct states enabling sufficient configurations to satisfy most design requirements. They are defined below.

- **Talk**. Break switches SW1 and SW2 closed, all other switches open. This provides a path between the ringing SLIC and the drop allowing communication and signalling to pass between the subscriber and the network.
- **Test_IN**. Test switches SW5 and SW6 closed, all other switches open. In this state the SLIC, CODEC and digital carrier performance can be tested via the Test In or Channel Test bus
- **Test_OUT**. Test switches SW3 and SW4 closed and all other switches open. This state provides the

means to test the drop without the loading effects of the line feed circuitry.

- **Test_IN Monitor**. Break switches SW1 and SW2 plus the TEST_IN switches SW5 and SW6 closed, all other switches open. With this state it is possible to monitor the SLIC output while the SLIC is driving the line.
- **Test_OUT Monitor**. Break switches SW1 and SW2 plus the TEST_OUT switches SW3 and SW4 closed, all other switches open. With this state it is possible to monitor the LCAS output while the SLIC is driving the line.
- **Test_IN & OUT**. TEST_IN switches SW5 and SW6 plus the TEST_OUT switches SW3 and SW4 closed, all other switches open. This state allows simultaneous testing of the transmission channel and the drop.
- **Test_IN BRIDGE**. TEST_IN switches SW5 and SW6 plus TEST BRIDGE switches SW7 and SW8 closed, all other switches open. This state allows connecting the SLIC output to the Test Out bus to compare the on-hook TEST_OUT Monitor evaluation. This makes it possible to determine if there is a failure with the Break Switches.
- **All-Off**. All switches open. Activation of this state can be accomplished by setting the appropriate IN_X pattern or by pulling the T_{SD} input/output low.

2.3 Switch Logic and Control

2.3.1 Introduction

The CPC7508 uses a three input transparent latch as the interface between the externally controlled inputs, IN_A, IN_B and IN_C and the switch logic. Control of the transparent latch is by means of the LATCH input.

Data output from the latch is fed into the switch control logic which decodes the inputs and drives the appropriate switches. To prevent undesirable switch activity during both start-up and power down the switch control logic also contains under voltage lock out detection circuitry to manage the behavior of the CPC7508. The under voltage lock out release threshold is internally set to ensure all internal logic is properly biased before accepting external switch commands from the INx inputs to control the switch states. Prior to release of the under voltage lock out, the switch control logic is conditioned to the All-Off state

2.3.2 Under Voltage Detection and Switch Lock Out

Under voltage detection circuitry in the CPC7508 consists of an internal detector to evaluate the V_{DD} supply and smart logic to provide for switch state control during both power up and power loss transitions.

Any time an unsatisfactory condition causes the V_{DD} supply to fall below the internally set under voltage lockout threshold, the smart logic overrides user switch control by blocking the information at the INx input pins and conditions the switch control logic to place the switches into the All-Off state.

2.3.2.1 Power Up Sequence

Upon power up, the under voltage detector and smart logic become active before the switch driver circuits and the switch control logic can activate any of the switches. As the V_{DD} supply starts up, the rising supply voltage is evaluated by the under voltage detector to determine when to de-assert the under voltage switch lock out command. Prior to release of the lock out command, the smart logic preconditions the switch control logic for the All-Off state.

The All_Off state is sustained by holding the LATCH input at a logic high level. This is accomplished by an external resistor at the LATCH pin which pulls the input to the supply voltage used by the on-board logic. The LATCH logic high secures the switch control logic and the CPC7508 remains in the All-Off state until the LATCH input is pulled down to a logic low. Prior to the assertion of a logic low at the LATCH pin, the control inputs IN_A, IN_B and IN_C must be properly conditioned.

2.3.2.2 Hot Plug and Power Up Circuit Design Considerations

To facilitate hot plug insertion and power up control the LATCH pin has an external pull up resistor to the local logic power rail that will hold a non-driven LATCH pin at a logic high state. This enables board designers to use the CPC7508 with FPGAs and other devices that provide high impedance outputs during power up and configuration.

There are six possible start up scenarios that can occur during power up. They are:

1. All inputs defined at power up & LATCH = 0
2. All inputs defined at power up & LATCH = 1
3. All inputs defined at power up & LATCH = Z
4. All inputs not defined at power up & LATCH = 0
5. All inputs not defined at power up & LATCH = 1
6. All inputs not defined at power up & LATCH = Z

Under all of the start up situations listed above the CPC7508 will hold all of it's switches in the all-off state during power up. When V_{DD} requirements have been satisfied the LCAS will complete it's start up procedure in one of three conditions.

For start up scenario 1 the CPC7508 will transition from the all-off state to the state defined by the inputs when V_{DD} is valid.

For start up scenarios 2, 3, 5, and 6 the CPC7508 will power up in the all-off state and remain there until the LATCH pin is pulled low. This allows for an indefinite all-off state for boards inserted into a powered system but are not configured for service or boards that need to wait for other devices to be configured first.

Start up scenario 4 will start up with all switches in the all-off state but upon the acceptance of a valid V_{DD} the LCAS will revert to one of the legitimate states listed in the truth tables and there after may randomly change states based on input pin leakage currents and loading. Because the LCAS state after power up can not be predicted with this start up condition it should never be utilized.

On designs that do not wish to individually control the LATCH pins of multi-port cards it is possible to bus many (or all) of the LATCH pins together to create a single board level input enable control.

2.3.2.3 Power Loss Sequence
For a falling V_{DD} event, the under voltage lock out detector monitors the supply voltage and upon reaching the internally set threshold point asserts the under voltage lock out command. This feature protects the integrity of the application during power dropouts by assuring proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed. Upon assertion of the under voltage lock out command the switch control logic is conditioned into the All_Off state where it will remain until V_{DD} recovers and the LATCH input is pulled low.

2.3.3 Data Latch
The CPC7508 has an integrated transparent data latch controlled by the LATCH input which can be used as an enable or a chip select function when the INx inputs of multiple LCAS devices are connected to common busses. The latch enable operation is controlled by TTL input logic levels at the LATCH pin. Control data is input to the latch via the input pins IN_A, IN_B and IN_C while the output of the data latch are internal nodes used for state control. When the LATCH enable input control pin is a logic 0 (low) the data latch is transparent and any change to the inputs will flow directly through the latch to the state control circuitry and be reflected by a change in the switches status.

Whenever the LATCH enable control pin is at logic 1, the data latch is active and data is locked. Subsequent changes to the input controls IN_A, IN_B and IN_C will not result in a change to the control logic or affect the existing switch state.

2.4 T_{SD} Pin Description
The T_{SD} pin is a bi-directional I/O structure used as an output to indicate a thermal shutdown event is in effect and as an input to condition the device into the All-Off state.

As an output, this pin indicates the status of the thermal shutdown circuitry. During normal operation the output will be pulled up to a logic high by an external resistor tied to the local logic supply voltage. Under a line fault situation that creates excess thermal loading, the CPC7508 will enter thermal shutdown and a logic low will be output.

As an input, the T_{SD} pin is utilized to place the CPC7508 into the "All-Off" state by simply pulling the input to a logic low. Clare recommends the use of an open-collector or an open-drain type output from the control logic to manage the All-Off state using the T_{SD} pin.

Forcing T_{SD} to a logic 1 or tying this pin to V_{CC} will not prevent normal operation of the thermal shutdown circuitry inside the CPC7508. It will however prevent the user from detecting a thermal shutdown condition and is therefore not recommended.

Neither the T_{SD} input control nor the T_{SD} output functions are affected by the latch function. Since internal thermal shutdown control and external "All-off" control is not affected by the state of the LATCH enable input, T_{SD} will override state control.

2.5 Power Supplies

Only a +12 V supply and ground are connected to the CPC7508. Switch state control is powered exclusively by the +12 V supply while internal level shifters provide the necessary translation from the low voltage inputs to the switch driver circuitry.

2.6 Protection

The CPC7508 uses a combination of current limiting and a thermal shutdown mechanism to protect the SLIC device and itself from damage during transient line faults such as lightning.

For power induction or power-cross fault conditions the DC current limit function restricts the maximum current through the switches. Excess power dissipation during current limiting events will trigger the thermal shutdown circuit to shut down all of the switches.

2.6.1 Current Limiting function

If a lightning strike transient occurs when any of the devices switches are operating, the current will be restricted by the dynamic current limit response of the active switches. For instance, during the talk state, when a 1000V 10x1000 μs lightning pulse (GR-1089-CORE) is applied to the line though a properly clamped external protector, the current seen at T_{LINE} and R_{LINE} will be a pulse with a typical magnitude of 2.5 A and a duration less than 0.5 μs.

If a power-cross fault occurs with the device in the talk state, the current is passed though the break switches SW1 and SW2 but is limited by the DC current limit response of the two break switches. The DC current limit specified over temperature is between 80 mA and 425 mA and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a power cross fault condition, the measured current at T_{LINE} and R_{LINE} will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will enter the all-off state.

2.6.2 Thermal Shutdown

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown events the T_{SD} pin will output a logic low with a nominal 0 V level. A logic high is output from the T_{SD} pin during normal operation with a typical output level equal to V_{DD}.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, the device temperature will rise and the thermal shutdown mechanism will activate forcing the switches to the all-off state. At this point the current measured into T_{LINE} or R_{LINE} will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the de-activation level of the thermal shutdown circuit. This permits the device to autonomously return to normal operation. If the transient has not passed, current will again flow up to the value allowed by the dynamic DC current limiting of the switches and heating will resume, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector will activate shunting the fault current to ground.
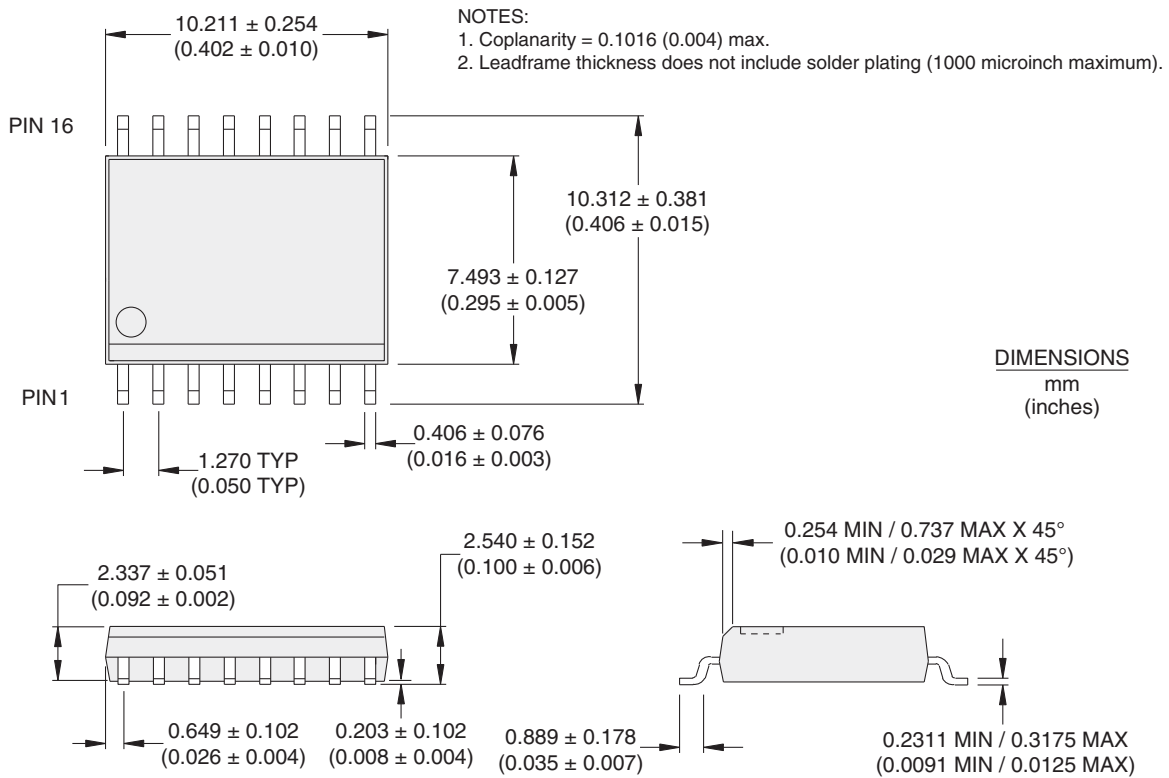
2.7 External Protection Elements

The CPC7508 requires only the over voltage secondary protector normally used to protect the ringing SLIC placed on the line side of the LCAS. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7508. Use of a foldback or crowbar type protector is recommended to minimize stresses on the LCAS.
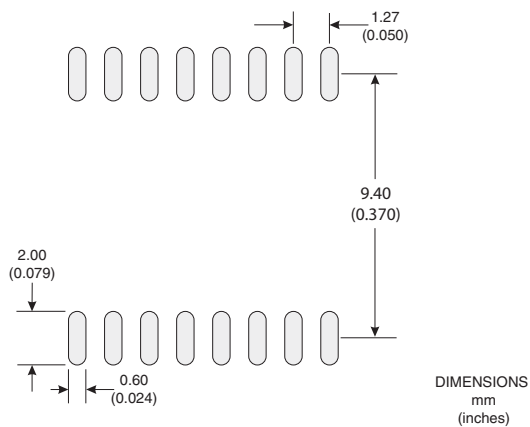
Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.
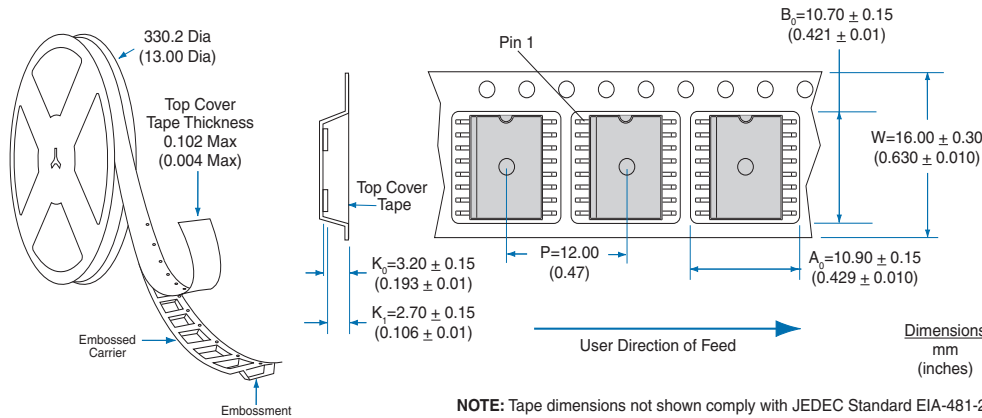
3. Manufacturing Information

3.1 Mechanical Dimensions

10.211 ± 0.254
(0.402 ± 0.010)

PIN 16

PIN 1

NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).

10.312 ± 0.381
(0.406 ± 0.015)

7.493 ± 0.127
(0.295 ± 0.005)

DIMENSIONS
mm
(inches)

0.406 ± 0.076
(0.016 ± 0.003)

1.270 TYP
(0.050 TYP)

2.337 ± 0.051
(0.092 ± 0.002)

2.540 ± 0.152
(0.100 ± 0.006)

0.649 ± 0.102
(0.026 ± 0.004)

0.203 ± 0.102
(0.008 ± 0.004)

0.889 ± 0.178
(0.035 ± 0.007)

0.254 MIN / 0.737 MAX X 45°
(0.010 MIN / 0.029 MAX X 45°)

0.2311 MIN / 0.3175 MAX
(0.0091 MIN / 0.0125 MAX)

3.2 Printed-Circuit Board Land Pattern

1.27
(0.050)

9.40
(0.370)

2.00
(0.079)

0.60
(0.024)

DIMENSIONS
mm
(inches)

3.3 Tape and Reel Packaging

NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

3.4 Soldering

3.4.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity for this package using IPC/JEDEC standard J-STD-020. The CPC7508B 16-pin SOIC package conforms to with the IPC/JEDEC standard J-STD-033 moisture sensitivity level (MSL) level 1.

3.4.2 Reflow Profile

For proper assembly, this component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

3.5 Washing

Clare does not recommend ultrasonic cleaning of this part.

For additional information please visit www.clare.com