

# MOS INTEGRATED CIRCUIT $\mu PD23C64040AL$

### 64M-BIT MASK-PROGRAMMABLE ROM 8M-WORD BY 8-BIT(BYTE MODE) / 4M-WORD BY 16-BIT(WORD MODE) PAGE ACCESS MODE

#### **Description**

The  $\mu$ PD23C64040AL is a 67,108,864 bits mask-programmable ROM. The word organization is selectable (BYTE mode: 8,388,608 words by 8 bits, WORD mode: 4,194,304 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The  $\mu$ PD23C64040AL are packed in 44-pin plastic SOP and 48-pin plastic TSOP (I).

#### **Features**

• Word organization

8,388,608 words by 8 bits (BYTE mode)

4,194,304 words by 16 bits (WORD mode)

• Page access mode

BYTE mode: 8-byte random page access WORD mode: 4-word random page access

• Operating supply voltage: 2.7 to 3.6 V

	Operating supply voltage Vcc	Access time / Page access time ns (MAX.)	Power supply current  (Active mode)	Standby current (CMOS level input)
ŀ	3.3 V ± 0.3 V	85 / 25	mA (MAX.) 60	μΑ (MAX.) 30
	3.0 V ± 0.3 V	100 / 30	55	30

#### **Ordering Information**

Part Number	Package
μPD23C64040ALGX-xxx	44-pin Plastic SOP (600 mil)
$\mu$ PD23C64040ALGY-xxx-MJH	48-pin Plastic TSOP (I) (12 x 18 mm)(Normal bent)
$\mu$ PD23C64040ALGY-xxx-MKH	48-pin Plastic TSOP (I) (12 x 18 mm)(Reverse bent)

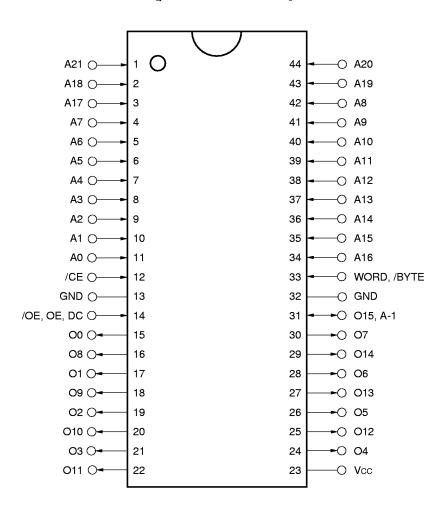
(xxx: ROM code suffix)

The information in this document is subject to change without notice.

#### Pin Configuration (Marking Side)

/xxx indicates active low signal.

# 44-pin plastic SOP (600 mil) [μPD23C64040AGX-xxx]



A0 - A21 : Address inputs
O0 - O7, O8 - O14 : Data outputs

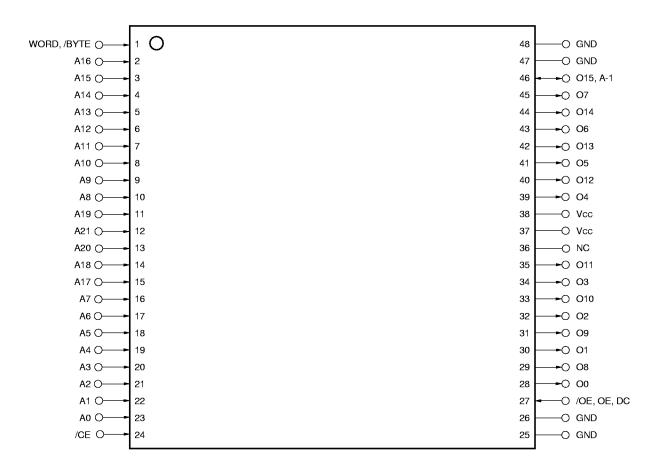
O15, A-1 : Data 15 output (WORD mode),

LSB address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE, OE : Output Enable
Vcc : Supply voltage

GND : Ground DC : Don't Care

# 48-pin plastic TSOP (I) (12 x 18 mm) (Normal bent) [μPD23C64040ALGY-xxx-MJH]



A0 - A21 : Address inputs

O0 - O7, O8 - O14 : Data outputs

O15, A-1 : Data 15 output (WORD mode),

LSB address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE, OE : Output Enable
Vcc : Supply voltage

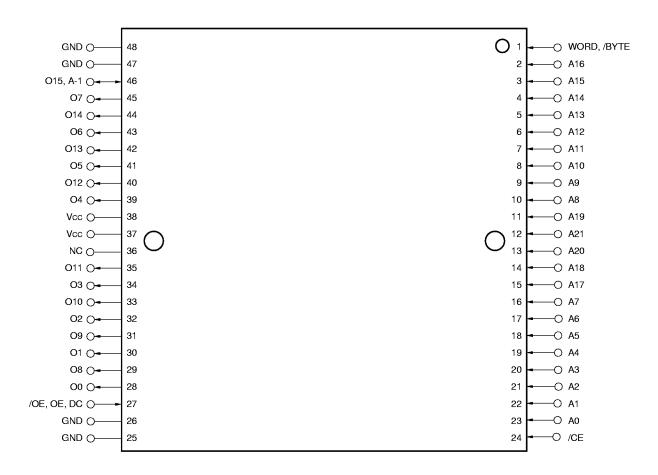
GND : Ground

NC No Connection

DC : Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

# 48-pin plastic TSOP (I) (12 x 18 mm) (Reverse bent) $[\mu PD23C64040ALGY-xxx-MKH]$



A0 - A21 : Address inputs

O0 - O7, O8 - O14 : Data outputs

O15, A-1 : Data 15 output (WORD mode),

LSB address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE, OE : Output Enable
Vcc : Supply voltage

GND : Ground

NC No Connection
DC : Don't Care

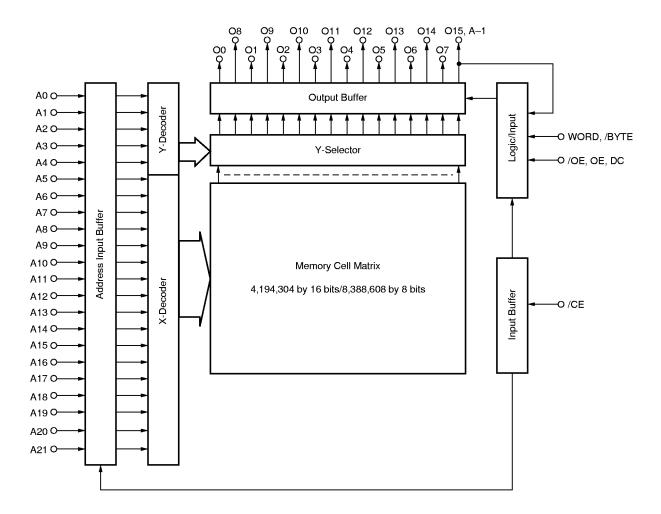
Note Some signals can be applied because this pin is not connected to the inside of the chip.



# **Input / Output Pin Functions**

Pin name	Input / Output	Function				
WORD, /BYTE	Input	The pin for switching BYTE mode and WORD mode.				
		High level: WORD mode (4M-word by 16-bit)				
		Low level : BYTE mode (8M-word by 8-bit)				
A0 to A21		Address bus.				
(Address inputs)		A0 to A21 are used differently in the WORD mode and the BYTE mode.				
		WORD mode (4M-word by 16-bit)				
		A0 to A21 are used as 22 bits address signals.				
		BYTE mode (8M-word by 8-bit)				
		A0 to A21 are used as the upper 22 bits of total 23 bits of address signal.				
		(The least significant bit (A-1) is combined to O15.)				
O0 to O7,	Output	Output data bus.				
O8 to O14		O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE n				
(Data output)		WORD mode (4M-word by 16-bit)				
		The lower 15 bits of 16 bits data outputs to O0 to O14.  (The most significant bit (O15) combined to A-1.)				
		· ·				
		BYTE mode (8M-word by 8-bit)				
		8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.				
O15, A–1	Input , Output	O15, A-1 are used differently in the WORD mode and the BYTE mode.				
(Data output 15),		WORD mode (4M-word by 16-bit)				
(LSB Address input)		The most significant output data bus (O15).				
		BYTE mode (8M-word by 8-bit)				
		The least significant address bus (A-1).				
/CE	Input	Chip activating signal.				
(Chip Enable)		When the OE is active, output states are following.				
		High level : High impedance				
		Low level : Data out				
/OE, OE, DC	Input	Output enable signal. The active level of OE is mask option. The active level of				
(Output Enable)		OE can be selected from high active, low active and Don't care at order.				
Vcc	-	Supply voltage				
GND	_	Ground				
NC	_	Not internally connected. (The signal can be connected.)				

#### **Block Diagram**





#### **Mask Option**

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among "0" "1" "x" shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	Н
х	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option: 0)

/CE	/OE	Mode	Output state
	L		Data out
L	Н	Active	High impedance
Н	H or L	Standby	High impedance

Operation mode (Option: 1)

/CE	OE	Mode	Output state
	L		High impedance
L	Н	Active	Data out
Н	H or L	Standby	High impedance

Operation mode (Option: x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
Н	H or L	Standby	High impedance

Remark L: Low level input

H: High level input



#### **Electrical Specifications**

#### **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	Vcc		-0.3 to +4.6	٧
Input voltage	Vı		-0.3 to Vcc+0.3	٧
Output voltage	Vo		-0.3 to Vcc +0.3	٧
Operating ambient temperature	Та		-10 to +70	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

#### Capacitance ( $T_A = 25 °C$ )

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Cī	f = 1 MHz			10	pF
Output capacitance	Со				12	рF

#### DC Characteristics (T<sub>A</sub> = -10 to +70 °C, Vcc = 2.7 to 3.6 V)

Parameter	Symbol	Test conditions			TYP.	MAX.	Unit
High level input voltage	ViH			2.0		Vcc + 0.3	٧
Low level input voltage	VIL	Vcc = 3.0 V ± 0.3 V		-0.3		+0.5	٧
		Vcc = 3.3 V ± 0.3 V		-0.3		+0.8	
High level output voltage	Vон	Іон = −100 μА	oн = -100 μA				٧
Low level output voltage	Vol	loL = 2.1 mA			0.4	٧	
Input leakage current	lш	VI = 0 V to Vcc		-10		+10	μΑ
Output leakage current	Іьо	Vo = 0 V to Vcc, Chip desele	cted	-10		+10	μΑ
Power supply current	Icc <sub>1</sub>	/CE = VIL(Active mode),	/CE = $V_{IL}$ (Active mode), $V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$			55	mA
		lo = 0 mA				60	
Standby current	Іссз	/CE = Vcc - 0.2 V (Standby I			30	μΑ	

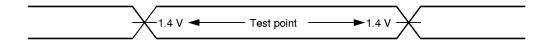
#### ★ AC Characteristics ( $T_A = -10 \text{ to } +70 \text{ °C}$ , $V_{CC} = 2.7 \text{ to } 3.6 \text{ V}$ )

Parameter	Symbol	Test condition	Vcc :	$Vcc = 3.0 V \pm 0.3 V$		Vcc = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	tacc				100			85	ns
Page access time	<b>t</b> PAC				30			25	ns
Chip enable access time	<b>t</b> ce				100			85	ns
Output enable access time	toe				30			25	ns
Output hold time	tон		0			0			ns
Output disable time	<b>t</b> DF		0		30	0		25	ns
WORD, /BYTE access time	twв				100			100	ns

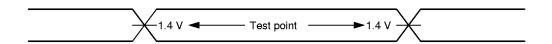
**Remark** toF is the time from inactivation of /CE or /OE, OE to high-impedance state output.

#### **AC Test Conditions**

#### Input waveform (Rise / Fall time ≤ 5 ns)



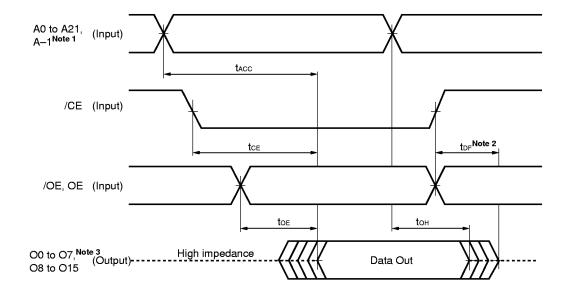
#### Output waveform



#### **Output load**

1TTL + 100 pF

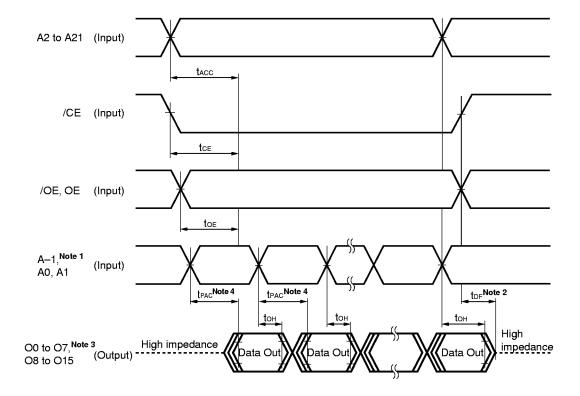
#### **Read Cycle Timing Chart 1**



Notes 1. During WORD mode, A-1 is O15.

- 2. tor is specified when one of /CE, /OE, OE is inactivated.
- 3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

#### ★ Read Cycle Timing Chart 2 (Page Access Mode)

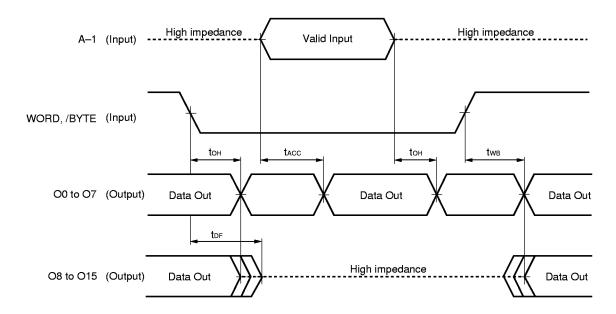


Notes 1. During WORD mode, A-1 is O15.

- 2. toF is specified when one of /CE, /OE, OE is inactivated.
- 3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.
- 4. The definition of page access time is as follows.

Page access time	Upper address (A2 to A21)	/OE, OE input condition		
tpac	Before tacc — tpac	Before tce — tpac	Before stabilizing of page address (A -1, A0, A1)	

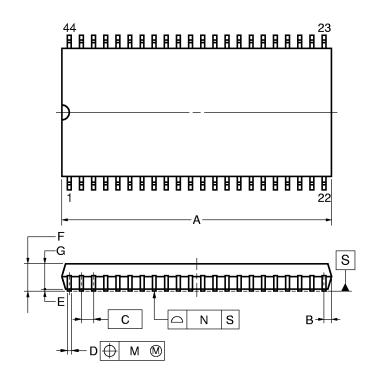
#### **★** WORD, /BYTE Switch Timing Chart



Remark /OE, OE and /CE: Active.

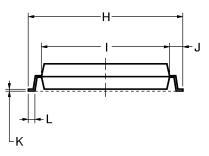
#### **Package Drawings**

## 44 PIN PLASTIC SOP (600 mil)



detail of lead end





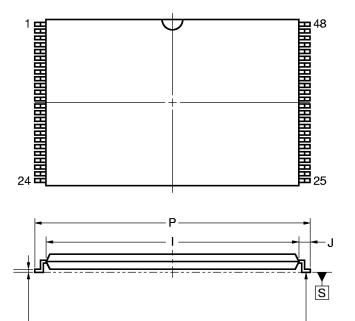
#### NOTE

- 1. Controlling dimension millimeter.
- 2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
Α	$27.83^{+0.4}_{-0.05}$	$1.096^{+0.016}_{-0.003}$
В	0.78 MAX.	0.031 MAX.
С	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.15±0.1	0.006±0.004
F	3.0 MAX.	0.119 MAX.
G	2.7±0.05	$0.106^{+0.003}_{-0.002}$
Н	16.04±0.3	$0.631^{+0.013}_{-0.012}$
I	13.24±0.1	$0.521^{+0.005}_{-0.004}$
J	1.4±0.2	0.055±0.008
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
М	0.12	0.005
N	0.10	0.004
Р	3° +7° -3°	3° +7° -3°

P44GX-50-600A-3

# **48 PIN PLASTIC TSOP (I) (12×18)**





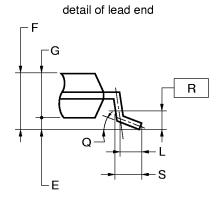
-K

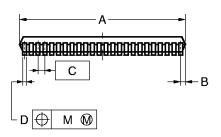
- $1. \ Controlling \ dimension --- \ Millimeter.$
- Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

Ν

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3. "A" excludes mold flash. (Includes mold flash: 12.4 mm MAX. <0.489 inch MAX.>)

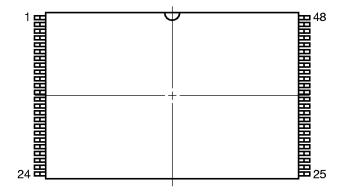


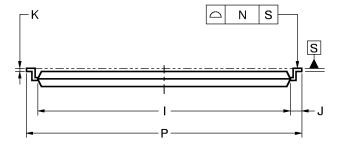


ITEM	MILLIMETERS	INCHES
Α	12.0±0.1	$0.472^{+0.005}_{-0.004}$
В	0.45 MAX.	0.018 MAX.
С	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
1	16.4±0.1	$0.646^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
К	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
М	0.10	0.004
N	0.10	0.004
Р	18.0±0.2	$0.709^{+0.008}_{-0.009}$
Q	3° +5° -3°	3° +5° -3°
R	0.25	0.010
s	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MJH1

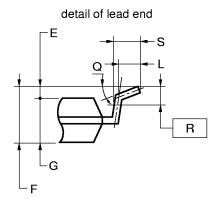
## 48 PIN PLASTIC TSOP (I) (12×18)

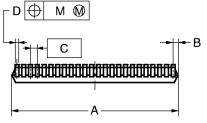






- 1. Controlling dimension Millimeter.
- 2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
- 3. "A" excludes mold flash. (Includes mold flash: 12.4 mm MAX. <0.489 inch MAX.>)





ITEM	MILLIMETERS	INCHES
Α	12.0±0.1	$0.472^{+0.005}_{-0.004}$
В	0.45 MAX.	0.018 MAX.
С	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
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R	0.25	0.010
s	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MKH1



#### **Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD23C64040AL.

#### Types of Surface Mount Device

 $\mu$ PD23C64040ALGX : 44-pin plastic SOP (600 mil)

 $\mu$ PD23C64040ALGY-MJH : 48-pin plastic TSOP (I) (12 x 18 mm) (Normal bent)  $\mu$ PD23C64040ALGY-MKH : 48-pin plastic TSOP (I) (12 x 18 mm) (Reverse bent) [MEMO]

[MEMO]

#### NOTES FOR CMOS DEVICES —

#### 1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

#### (2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

#### (3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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NEC devices are classified into the following three quality grades:

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.