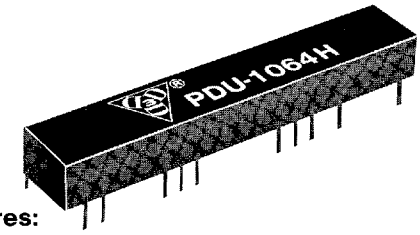
Digitally Programmable Delay Units

SERIES: PDU-1064H
(6-Bit) ECL Interfaced

data delay devices, inc.



Features:

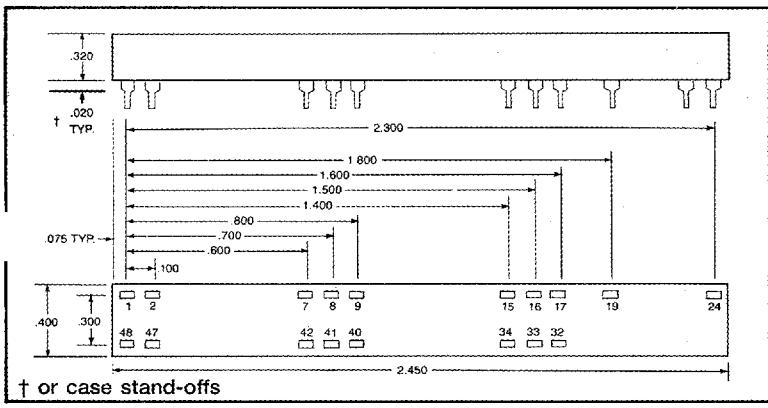
- Low propagation delay
- Input & output ECL buffered
- 6-BIT ECL programmable delay line
- Output same polarity of input
- Completely interfaced
- Compact & low profile

Specifications:

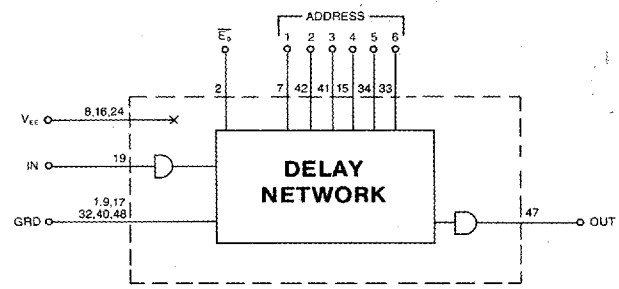
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: + 5% or 2 ns whichever is greater.
- Inherent delay (T_{DD}): 12 ns typ.
- Propagation delay:
  Address to output (T_{SUA}) = 3.6 ns typ.
  Enable to output (T_{SUE}) = 1.7 ns typ.
- Power dissipation: 925 mw typ.
- Supply voltage: −5 Vdc ± 5%.
- Operating Temperature: 0-70°C.
- Temperature Coefficient: 100 PPM/°C.
- DC parameters: See ECL-10KH Logic Table on Page 6.

Test Conditions

- **Input pulse-width:** ≥150% of Max. delay.
- **Input pulse spacing:** ≥3 times of Max. delay.
- **Input pulse voltage:** ECL logic.
- **Measurements taken @** T_a = 25°C, V_{EE} = −5V.



† or case stand-offs



TRUTH TABLE

Enable ($\overline{E_0}$)	Address 6	5	4	3	2	1	Delay Out
0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	1	T_1
0	0	0	0	0	1	0	T_2
0	0	0	0	0	1	1	T_3
0	0	0	0	1	0	0	T_4
0	0	0	0	1	0	1	T_5
0	0	0	0	1	1	0	T_6
0	0	0	0	1	1	1	T_7
0	0	0	1	0	0	0	T_8
0	0	0	1	1	1	1	T_{15}
0	0	1	0	0	0	0	T_{16}
0	0	1	1	1	1	1	T_{31}
0	1	0	0	0	0	0	T_{32}
0	1	1	1	1	1	1	T_{63}
1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{63}$ Multiplier of incremental delay.

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1064H-0.5	0.5 ± 0.3	31.5
PDU-1064H-1	1 ± 0.5	63
PDU-1064H-2	2 ± 0.5	126
PDU-1064H-3	3 ± 1.0	189
PDU-1064H-4	4 ± 1.0	252
PDU-1064H-5	5 ± 1.0	315
PDU-1064H-6	6 ± 1.0	378
PDU-1064H-8	8 ± 1.0	504
PDU-1064H-10	10 ± 1.5	630

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